

# Behavioral Simulation of an Optical-Electrical Sub-Sampling Down Conversion Receiver and CT Delta-Sigma ADC

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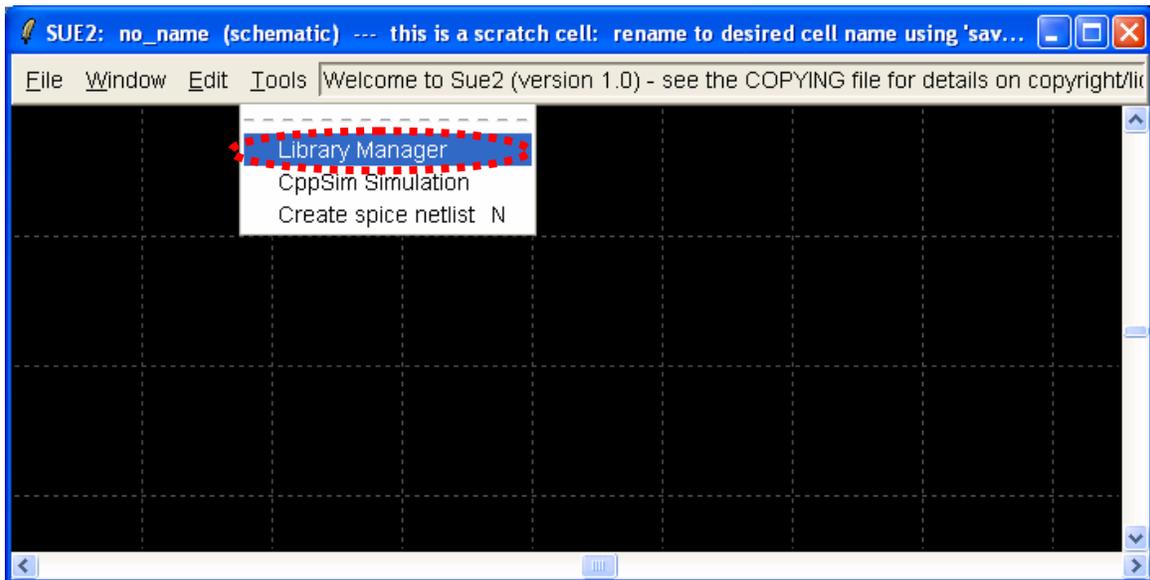
## Setup

Download and install the CppSim Version 3 package (i.e., download and run the self-extracting file named **setup\_cppsim3.exe**) located at:

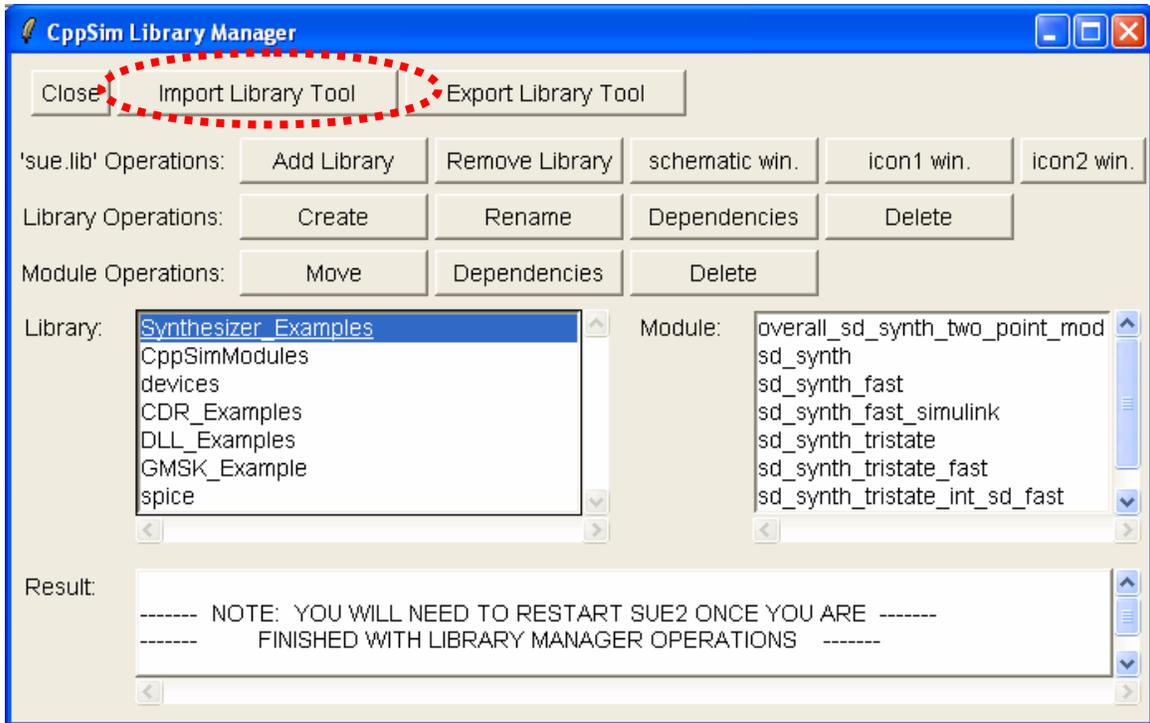
<http://www.cppsim.com>

Upon completion of the installation, you will see icons on the Windows desktop corresponding to the PLL Design Assistant, CppSimView, and Sue2. Please read the “**CppSim (Version 3) Primer**” document, which is also at the same web address, to become acquainted with CppSim and its various components. You should also read the manual “**PLL Design Using the PLL Design Assistant Program**”, which is located at <http://www.cppsim.com>, to obtain more information about the PLL Design Assistant as it is briefly used in this document.

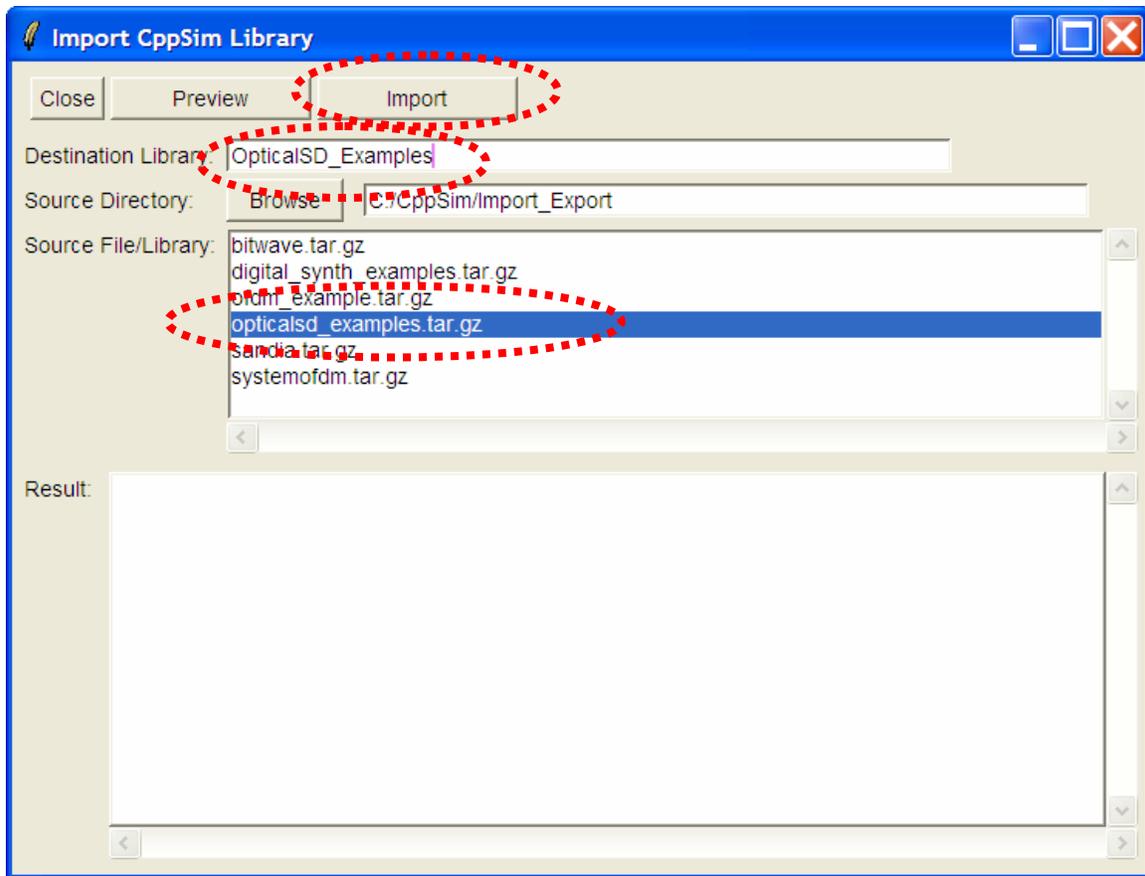
To run this tutorial, you will also need to download the file **opticalsd\_examples.tar.gz** available at <http://www.cppsim.com>, and place it in the **Import\_Export** directory of CppSim (assumed to be **c:/CppSim/Import\_Export**). Once you do so, start up **Sue2** by clicking on its icon, and then click on **Tools->Library Manager** as shown in the figure below.



In the **CppSim Library Manager** window that appears, click on the **Import Library Tool** button as shown in the figure below.



In the **Import CppSim Library** window that appears, change the **Destination Library** to **OpticalSD\_Examples**, click on the **Source File/Library** labeled as **opticalsd\_examples.tar.gz**, and then press the **Import** button as shown in the figure below. Note that if **opticalsd\_examples.tar.gz** does not appear as an option in the **Source File/Library** selection listbox, then you need to place this file (downloaded from <http://www.cppsim.com>) in the **c:/CppSim/Import\_Export** directory.

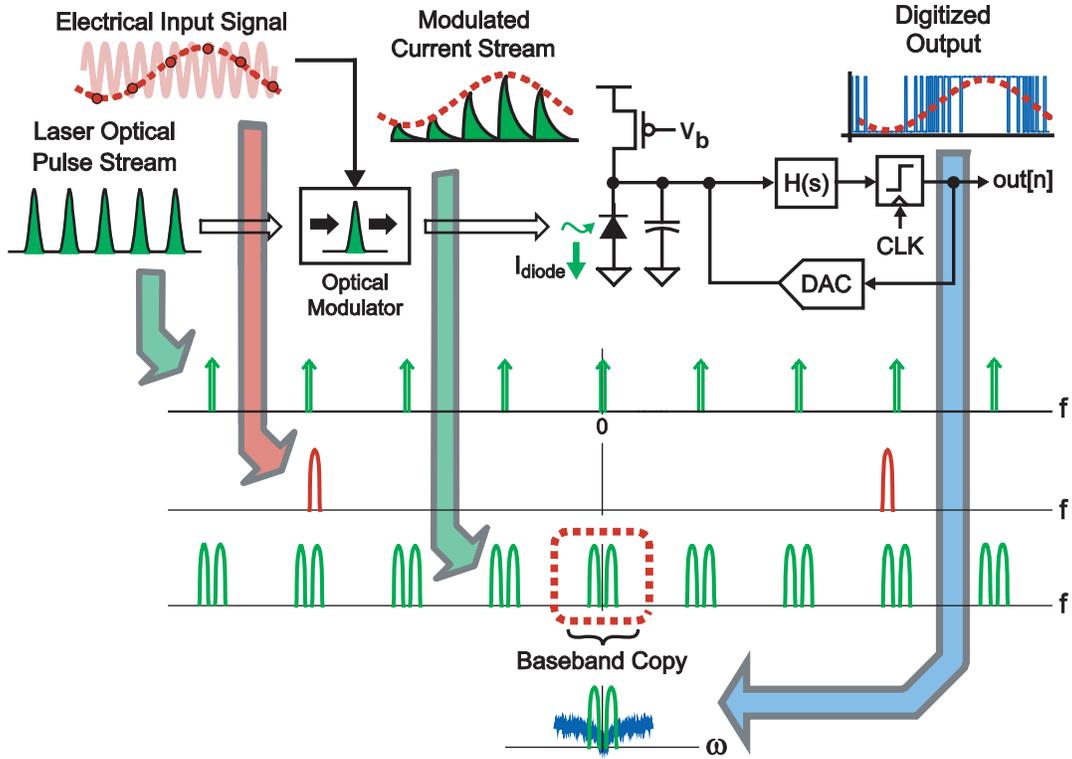


Once you have completed the above steps, restart **Sue2** as directed in the above figure.

## **Introduction**

Most significant improvements in performance in increasingly complex communications systems will arise from architectural innovations. These innovations are only possible when you can quickly and accurately model and simulate the system under consideration. CppSim is a free behavioral simulation package that leverages the C++ language to allow very fast simulation of a wide array of system types. The goal of this tutorial is to expose the reader to a novel optical-electrical sub-sampling down-conversion receiver and ADC.

As shown in Figure 1, a low-jitter pulsed laser is leveraged to perform precise sub-sampling of a narrowband RF signal. Information travels between the optical and electrical domains by connecting a photodiode to an on-chip current source and capacitor. The resulting photodiode-based integrator serves as the input stage to a continuous-time (CT) 2nd order  $\Delta\Sigma$  ADC, which digitizes the down-converted signal. The entire architecture is modeled in CppSim, enabling the exploration of key design issues, and providing crucial insights on how optical devices could be improved to yield better system-level performance.



**Figure 1:** Mode-locked-laser sub-samples a narrowband RF signal, and CT  $\Delta\Sigma$  ADC digitizes baseband signal while filtering out images with its inherent anti-aliasing filter.

### A. Background

Sub-sampling down-conversion provides an alternative to conventional down-conversion architectures, but is usually limited by aperture jitter. Indeed, prior work employing narrowband electronic sub-sampling architectures suffered lower SNR than other conversion techniques due to noise-folding from aliasing, and noise skirts arising from local oscillator aperture jitter [1-3]. Noise folding can be minimized through band-pass filtering of the RF prior to mixing, as was done in previous work. However, due to the limit of aperture jitter in electronics (0.5-2 ps rms [4]) and its impact on SNR, sub-sampling architectures have seldom operated above a few GHz.

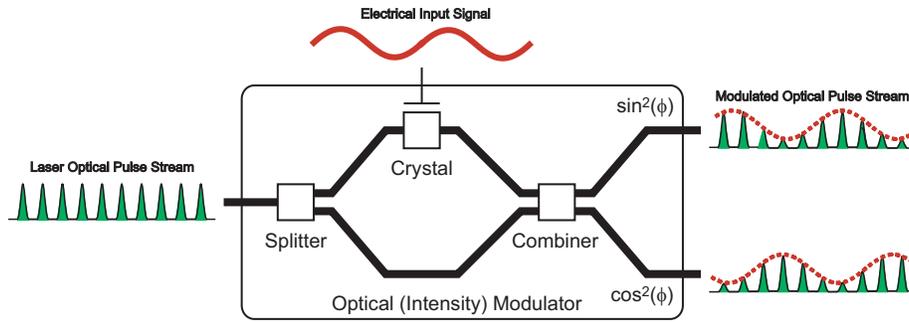
<i>Harmonic (GHz)</i>	<i>SNR (dB)</i>	<i># of Bits</i>
1	84	14.0
5	70	11.7
10	64	10.7
20	58	9.7
40	52	8.7

**Table 1:** SNR and ENOB at different harmonic frequencies assuming a 200 MHz repetition-rate mode-locked laser with 10 fs RMS jitter in a 2 MHz bandwidth

The SNR for a given aperture jitter and carrier frequency is described by [5]:

$$SNR = 20 \log \left( \frac{1}{2\pi f_o \Delta t} \right) \quad (1)$$

where  $f_o$  is the carrier frequency and  $\Delta t$  is the rms jitter of the local oscillator in the bandwidth of interest. Aperture jitter of mode-locked lasers have been shown to be extremely low ( $< 10$  fs in a 1 kHz-20MHz bandwidth [6]), which facilitates the sub-sampling of RF signals in the 10's of GHz range with close to 8 bit precision. Table 1 lists the calculated SNR values for various RF carrier frequencies assuming 10 fs rms aperture jitter in a 2 MHz BW. Indeed, with a mode-locked laser with 10 fs of rms jitter, close to 9 bits of resolution is possible even at an RF frequency of 40 GHz.



**Figure 2:** differential power modulation using a dual output intensity modulator

The optical-electrical sampler shown in Figure 2 comprises a mode-locked laser and an optical modulator. An optical modulator (also called an intensity modulator) uses an applied voltage to vary the refractive index of one optical axis of a crystal, thereby creating a phase shift between two polarization states. When the two optical paths are recombined with an optical combiner, the phase shift from the crystal effectively results in an intensity modulation of the optical power. The relationship between optical power ( $P_{in}(t)$ ) and applied voltage ( $v_{in}(t)$ ) is then described by:

$$P_{out+}(t) = P_{in}(t) \sin^2 \left( \frac{\pi}{2} \cdot \frac{v_{in}(t)}{v_{\pi}} \right) \quad (2a)$$

$$P_{out-}(t) = P_{in}(t) \cos^2 \left( \frac{\pi}{2} \cdot \frac{v_{in}(t)}{v_{\pi}} \right) \quad (2b)$$

Where  $P_{out+}(t)$  and  $P_{out-}(t)$  are the differentially modulated optical powers leaving the device,  $P_{in}(t)$  is the applied optical signal power,  $v_{in}(t)$  is the applied electronic signal, and  $v_{\pi}$  is the modulator voltage-to-phase gain.

When biased at its most linear point ( $V_{IN,DC} = v_{\pi}/2$ ), the modulator and its non-linearity can be approximated by a 3<sup>rd</sup> order polynomial of the form:

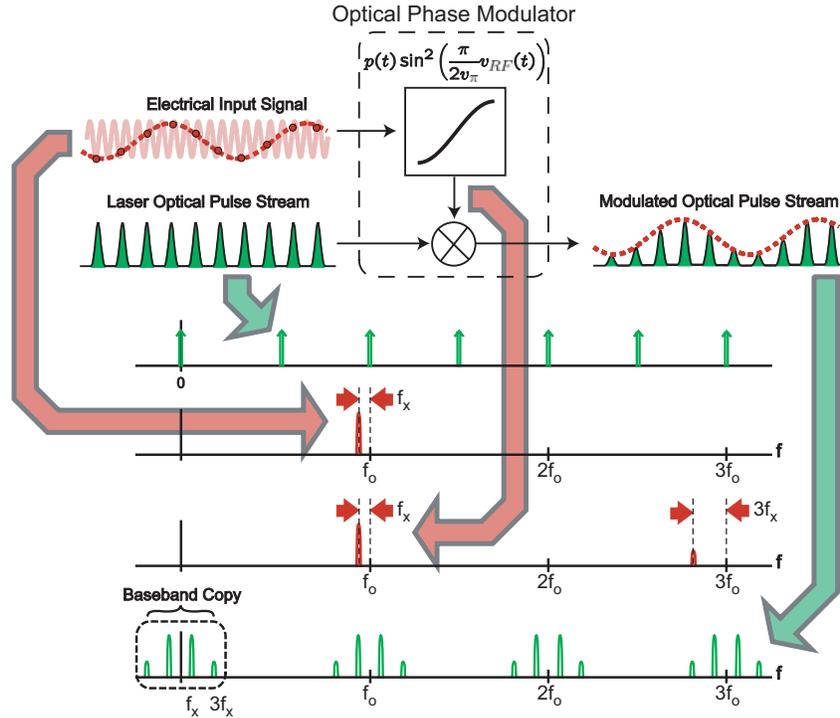
$$P_{out}(t) = \alpha_0 + \alpha_1 v_{in}(t) + \alpha_2 v_{in}(t)^2 + \alpha_3 v_{in}(t)^3 \quad (3)$$

with coefficients:

$$\begin{aligned} \alpha_0 &= \frac{1}{2} P_{avg} \\ \alpha_1 &= \frac{1}{2} P_{avg} \cdot \frac{\pi}{v_\pi} \\ \alpha_2 &= 0 \\ \alpha_3 &= -\frac{1}{24} P_{avg} \cdot \left( \frac{\pi}{v_\pi} \right)^3 \end{aligned} \quad (4)$$

where  $P_{avg}$  is the average optical power applied to the optical modulator. The impact of modulator non-linearity can be understood with the aid of Figure 3. Here, the RF signal is a sinusoid of amplitude  $A$  offset by an amount  $f_x$  from a carrier frequency  $f_o$ , with  $f_o$  chosen to be an integer multiple of the pulse repetition frequency ( $f_o = N/T$ ):

$$v_{RF}(t) = A \cos(2\pi[f_o - f_x]t) \quad (5)$$



**Figure 3:** Aliasing of harmonics from 3<sup>rd</sup> order non-linearity down to baseband due to sub-sampling.

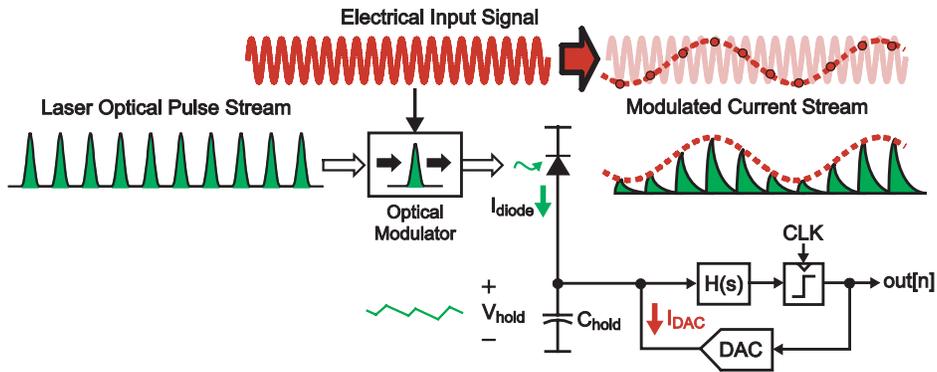
Due to differential power modulation, the even-order terms in the polynomial of Equation (3) should ideally be zero. The 3<sup>rd</sup> order non-linearity can then be studied in isolation:

$$(v_{RF}(t))^3 = \frac{A^3}{4} (3 \cos(2\pi[f_o - f_x]t) + \cos(2\pi[3f_o - 3f_x]t)) \quad (6)$$

Sub-sampling will alias the signals in equations (5) and (6) to baseband, resulting in the desired signal at  $f_x$ , and a harmonic at  $3f_x$ . Therefore, harmonics can still appear at baseband even in the absence of any interferers. Intermodulation can cause out-of-band interferers to alias down to baseband as well, but this effect can be potentially suppressed by using resonant optical modulators, which can have very high Q ( $> 300$ ). However, as is the case in any classical RF system, intermodulation can cause a weak signal of interest to be completely masked by a strong interferer if proper system design is not performed.

After the electronic signal has been sampled by the optical phase modulator, the resulting optical signal needs to be converted to the electronic domain. A photodiode is used to convert the optical sample information (photons) into an equivalent electronic signal (charge) that can be digitized using electronics. Modulated optical pulses are now converted to modulated current pulses, and the question now becomes how to efficiently capture this information for digitization.

## B. System Architecture



**Figure 4:** photodiode charge is continuously integrated onto a capacitor, and a comparator and DAC used to discharge the capacitor to prevent unbounded integration.

By limiting our application space to narrowband down-conversion, optical information can be easily captured by directly integrating the photodiode charge onto a capacitor. This approach is particularly attractive because it precludes the implementation of a S/H network, thus bypassing many of the non-idealities associated with MOS switches. Indeed, these switch non-idealities (finite resistance, charge injection, signal feed-through) severely limited the performance of prior broadband optical-electrical ADC implementations [4,7,8]. Furthermore, since charge is continuously integrated as opposed to compartmentalized as in a S/H network, the system is not as sensitive to current pulse transients arising from slow minority-carrier recombination time constants of the photodiode (which may not necessarily settle within a sample period). However, note that some mechanism is needed to counteract the unbounded integration of charge onto the capacitor so that saturation does not occur.

As shown in Figure 4, negative feedback offers a straightforward solution. Here, a level sensitive comparator (or quantizer) senses when the capacitor voltage exceeds a certain threshold, and then drives a current digital-to-analog converter (DAC) to discharge the capacitor. As long as the total charge supplied by the DAC is greater than or equal to that from the photodiode, the capacitor voltage will remain bounded. Indeed, the voltage at the photodiode output will be held constant on average, although there will be high frequency ripple due to the pulsed nature of the optical stream and feedback of the comparator's quantization noise.

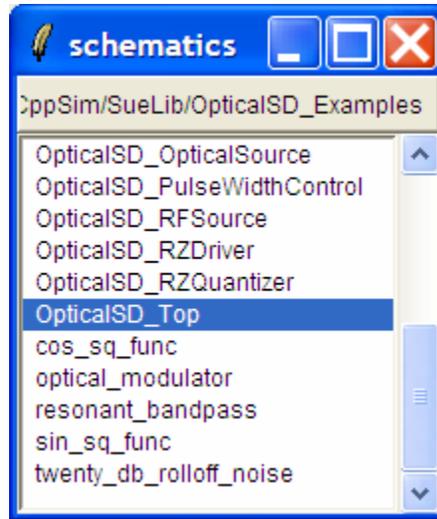
Structurally, the feedback loop in Figure 4 is identical to that of a conventional continuous-time (CT)  $\Delta\Sigma$  ADC, except that the voltage-to-current conversion is accomplished by the optical modulator and photodiode pair, as opposed to a transconductance-C amplifier or an op-amp RC integrator. When the quantizer oversamples the input signal, the loop operates identically to a CT  $\Delta\Sigma$  ADC, and achieves the benefits associated with the topology: noise shaping, higher SNR and DR, and potentially lower power for a given precision.

Note that the use of a  $\Delta\Sigma$  ADC architecture limits the application space of the down-converter to a narrowband signal in order to achieve a high over-sampling ratio (OSR) and SNR. This tradeoff is acceptable in our application since we are trying to digitize sub-sampled signals, which must be sufficiently narrowband to prevent aliasing. A salient feature of the CT  $\Delta\Sigma$  architecture is that it provides free anti-aliasing filtering since such filtering is inherent in the topology itself [9]. This unique property could not be exploited in earlier sub-sampling architectures that employed discrete-time (DT)  $\Delta\Sigma$  topologies which required a separate anti-alias filter.

## **Preliminaries**

### **A. Opening Sue2 Schematic**

Click on the Sue2 icon to start Sue2, and then select the **OpticalSD\_Examples** library from the **schematic listbox**. The **schematic listbox** should now look as follows:



Select the **OpticalSD\_Top** cell from the above **schematic listbox**. The Sue2 schematic window should now appear as shown below. Key signals for this schematic include:

**sd\_out**: 1-bit output of the Sigma-Delta Quantizer

**optmod\_out\_accum**: output of the optical modulator filtered by the accumulate and dump filter

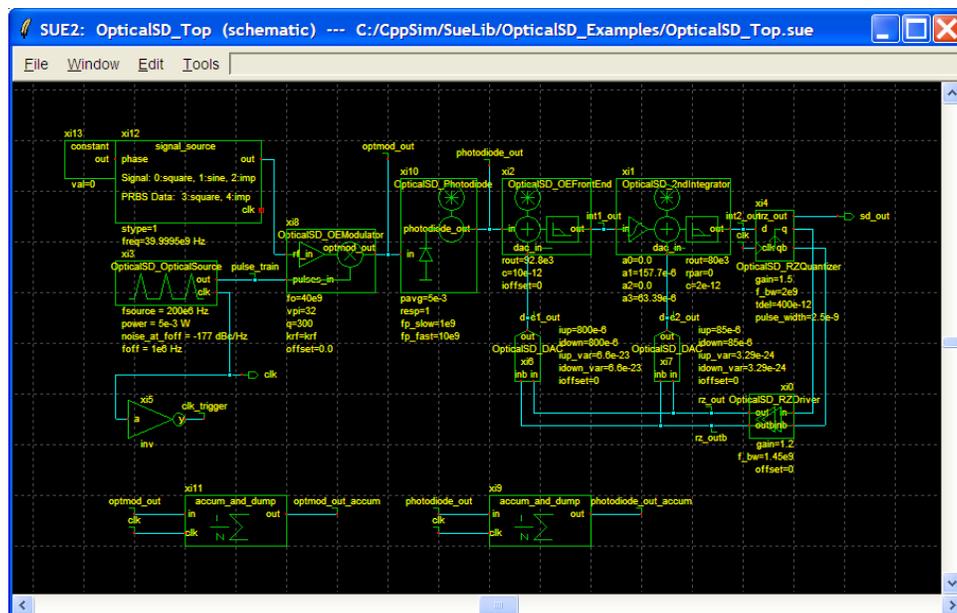
**photodiode\_out\_accum**: output of the photodiode filtered by the accumulate and dump filter

**pulse\_train**: pulse output of the mode-locked-laser

**int1\_out, int2\_out**: outputs of the 1<sup>st</sup> and 2<sup>nd</sup> stage integrators

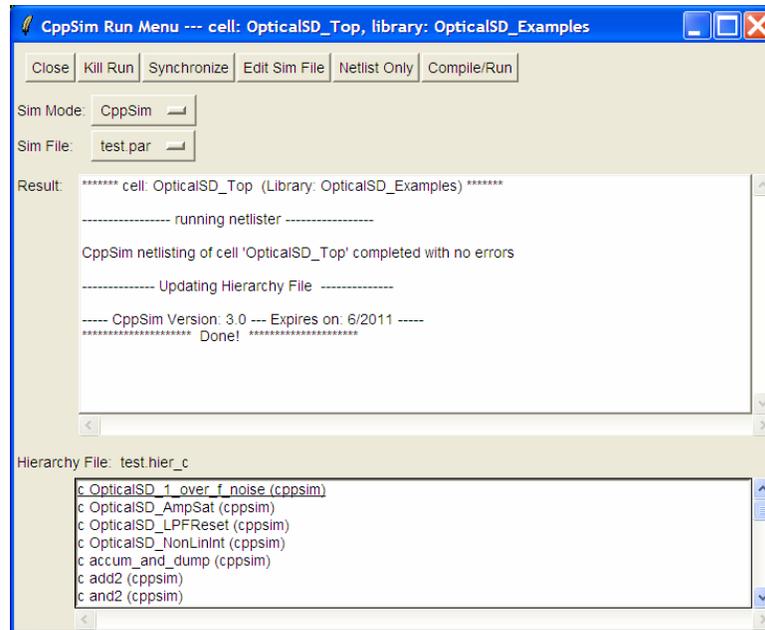
**dac1\_out, dac2\_out**: output current signals of the 1<sup>st</sup> and 2<sup>nd</sup> DAC's

**clk\_trigger**: clock signal used to sub-sample ADC output



## B. Running CppSim Simulations

In the Sue2 schematic window, click on the **Tools** text box in the menubar, and then select **CppSim Simulation**. A Run Menu window similar to the one shown below should open automatically. Note that the Run Menu is already synchronized to the schematic that you will be simulating (**OpticalSD\_Top**). If for whatever reason this is not the case, click on the Synchronize button in the menu bar, the Run Menu will be synchronized to the schematic in your Sue2 window.



To establish the simulation parameters, click on the **Edit Sim File** button in the menu. An Emacs window should appear displaying the contents of the simulation parameters file (**test.par**). The contents of your **test.par** file should look something like what is shown below:

```
//////////////////////////////////////
// CppSim Sim File: test.par
// Cell: OpticalSD_Top
// Library: OpticalSD_Examples
//////////////////////////////////////

// Number of simulation time steps
// Example: num_sim_steps: 10e3
num_sim_steps: 1e6

// Time step of simulator (in seconds)
// Example: Ts: 1/10e9
Ts: 1/100e9

// Output File name
// Example: name below produces test.tr0, test.tr1, ...
// Note: you can decimate, start saving at a given time offset, etc.
// -> See pages 34-35 of CppSim manual (i.e., output: section)
output: test_tran
```

```

// Nodes to be included in Output File
// Example: probe: n0 n1 xi12.n3 xi14.xi12.n0
probe: sd_out int1_out int2_out dacl_out dac2_out optmod_out
optmod_out_accum photodiode_out photodiode_out_accum

////////////////////////////////////
// Note: Items below can be kept blank if desired
////////////////////////////////////

// Values for global parameters used in schematic
// Example: global_param: in_gl=92.1 delta_gl=0.0 step_time_gl=100e3*Ts
global_param: ts=Ts

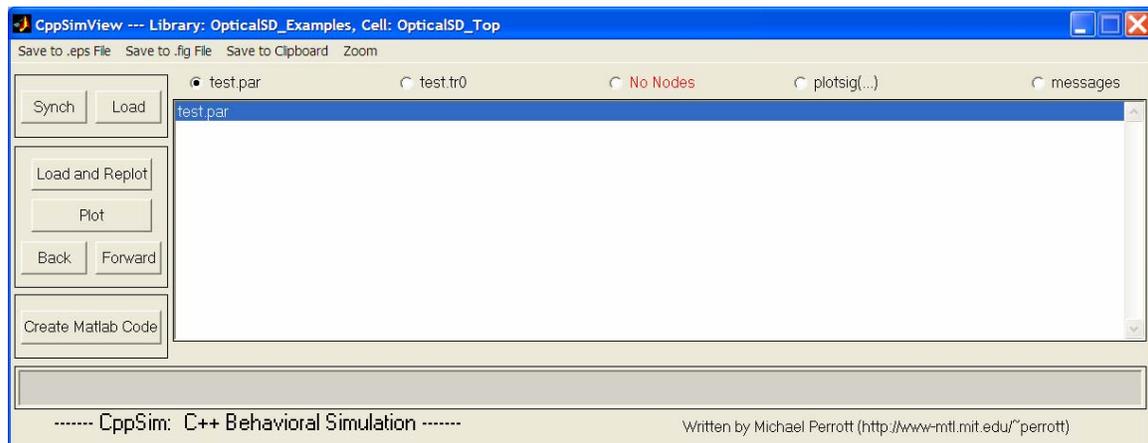
// Rerun simulation with different global parameter values
// Example: alter: in_gl = 90:2:98
// See pages 37-38 of CppSim manual (i.e., alter: section)
alter:

```

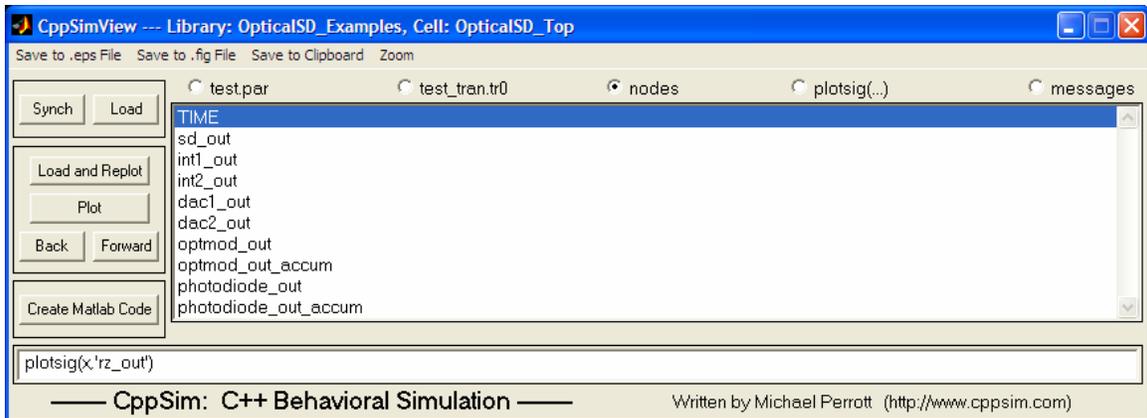
When you are finished, you can close the Emacs window by pressing **Ctrl-x Ctrl-c**. To launch the simulation, click on the menu bar button labeled **Compile/Run**.

## Plotting Time-Domain Results

Double-click on the CppSimView icon to start the CppSim viewer. The viewer should appear as shown below – notice that the banner indicates that it is currently synchronized to the **OpticalSD\_Top** cellview. If this is not the case, Sue2 and CppSimView can be synchronized by clicking the **Synch** button on the left-hand side of the CppSimView window.



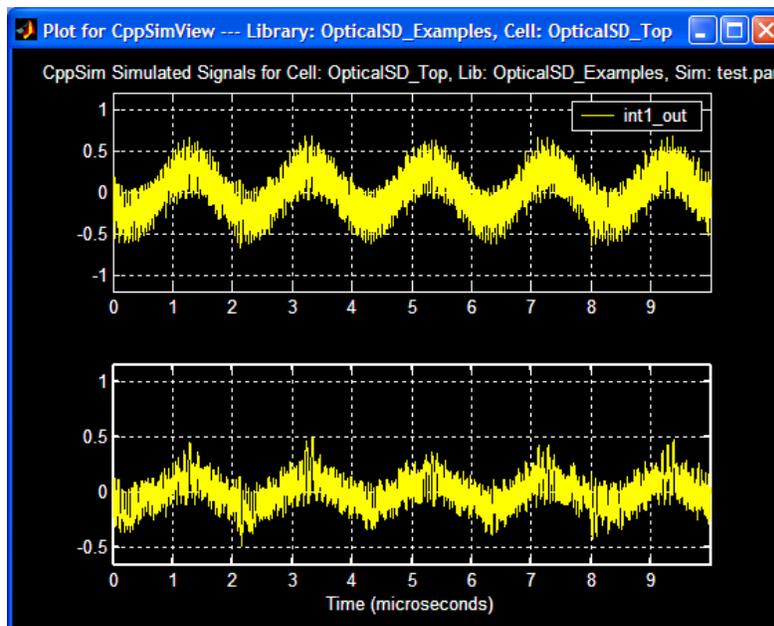
To view the simulation results, first click on the radio button titled **No Output File**. Immediately after this button is clicked, the radio button will instead display the output file's name, **test\_tran.tr0**. Next, click on the Load button on the left-hand side of the CppSimView window. Once this button is pressed, the **Nodes** radio button will be filled in, and the probed nodes will be listed, as shown below.

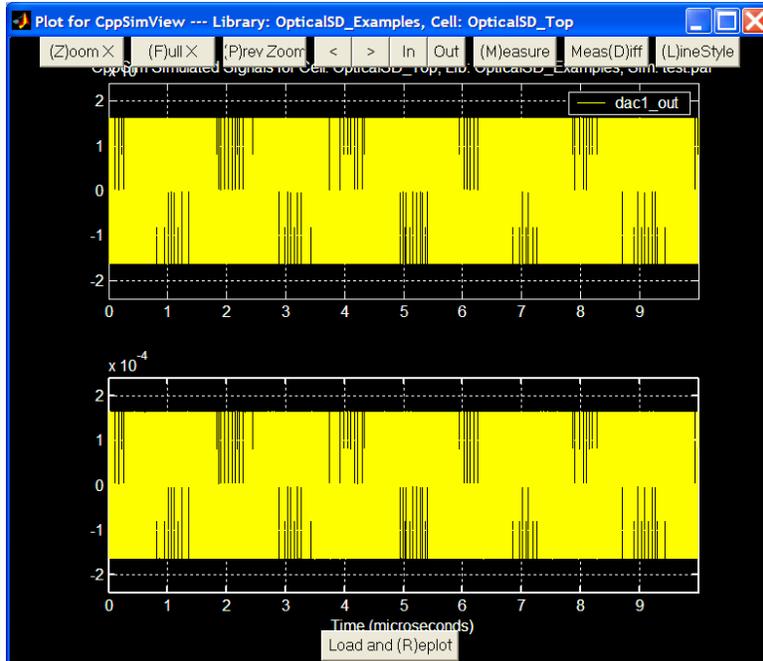


## A. Output Signal Plots

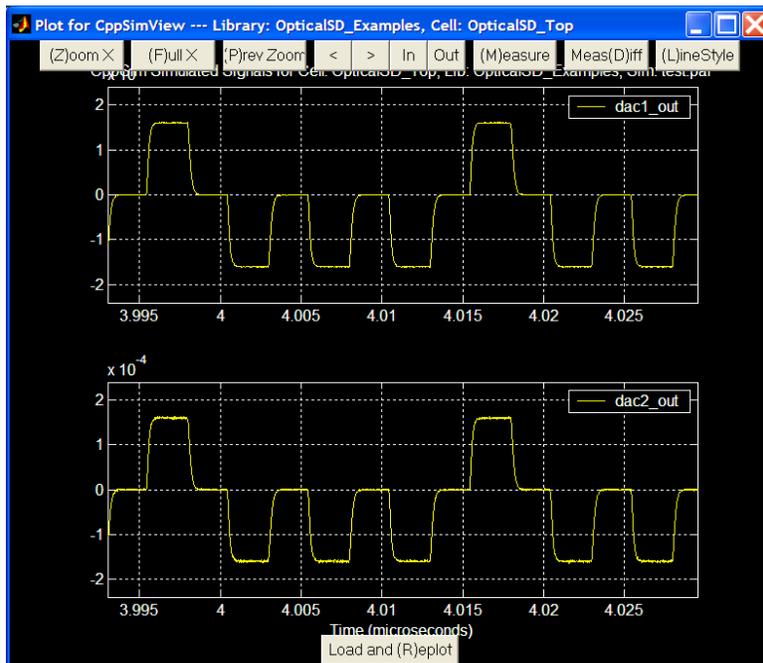
In the CppSimView window, double-click on signals **int\_out1** and **int\_out2**. You should see plots of the integrator output voltages, as shown below. These transient simulation plots can be used in the design of the Sigma-Delta ADC to determine if the output voltage swings may saturate the subsequent integration or quantization stage.

Now click on the Reset Node List button in the CppSimView window, and then double-click on the **dac1\_out** and **dac2\_out** nodes. You should see plots of the DAC output currents, but due to the large number of samples, you may have trouble viewing the waveforms clearly. To change the x-axis of the figure (the y-axis automatically scales), hit the Zoom radio button on the CppSimView menu-bar. This will cause a series of buttons to appear on the top and bottom of the plot window, as shown below.





Next click the **(Z)oom X** push-button located at the top of the plot window. Select the desired x-axis range by clicking at the beginning and ending location in any of the plotted signals. The figure will look similar to the figure below. Additionally, you can zoom in and out and pan left and right using the **In** and **Out** and the **<** and **>** push-buttons, respectively, located at the top of the plot figure. For example, expanding the x-axis around 4ns produces the plot shown below:



As can be seen from the plot, the RZ DAC output current exhibits rising and falling transients, which ultimately determine the upper limit of the DAC switching speed.

## Plotting Frequency-Domain Results

While viewing transient waveforms offer some intuition concerning the operation of the sub-sampling receiver and ADC, analyzing the frequency-domain results are essential in order to evaluate the performance of the overall architecture. To that end, longer simulations must be performed so that FFT's with sufficient resolution can be generated. MATLAB is used to load in the CppSim simulation data, and to calculate and plot the resulting FFT. The MATLAB script used to generate the subsequent FFT plots (`snr_plot.m`) is included in the **OpticalSD\_Examples** library.

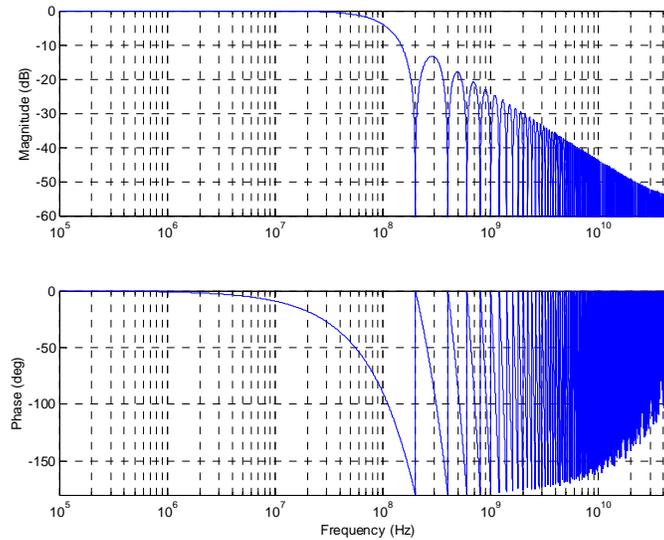
### **A. Triggering Output Data Storage**

Since the output of the optical-electrical ADC is a 200 Ms/s 1-bit code, it is not necessary to store this information at every CppSim time step  $T_s$ . Rather, the ADC output need only be stored at every ADC sample period  $T = 5\text{ns}$ , which results in a significantly smaller output file size. This can be accomplished by modifying the output statement in the `test.par` file:

```
output: test_fft trigger=clk_trigger start_sample=1e5
probe: sd_out optmod_out_accum
```

The above output statement will generate an output file called **test\_fft.tr0**, and will only write to the file when the trigger function detects a rising edge in the clock signal **clk\_trigger**. The **clk\_trigger** signal can be seen in the **OpticalSD\_Top** schematic, and simply corresponds to the inverted ADC clock signal **clk**. The **start\_sample** statement prevents the **test\_fft.tr0** output file from being written until the 100,000<sup>th</sup> simulation time step has completed. This statement is necessary since initial transients in the ADC will corrupt the FFT, and should not be recorded.

A second node of interest is the output of the optical modulator (**optmod\_out**). This signal effectively has infinite bandwidth, and must be filtered in order to extract the baseband signal, which is of primary interest. This can be easily accomplished using the **accum\_and\_dump** module, which averages the optical modulator output over one laser repetition period (or equivalently, over one ADC clock period) before dumping the result to the output, and resetting its internal state. A frequency domain view of this filter is shown in Figure 5.



**Figure 5:** Bode plot of an accumulate and dump filter assuming a CppSim internal time step of  $1/100e9$  and a laser repetition rate of 200 MHz.

Finally, it is necessary to set the number of simulation points. As previously mentioned, the number of simulation points will effectively determine the resolution of the FFT. For the sake of this tutorial, we pick ten million points:

```
num_sim_steps: 10.1e6
```

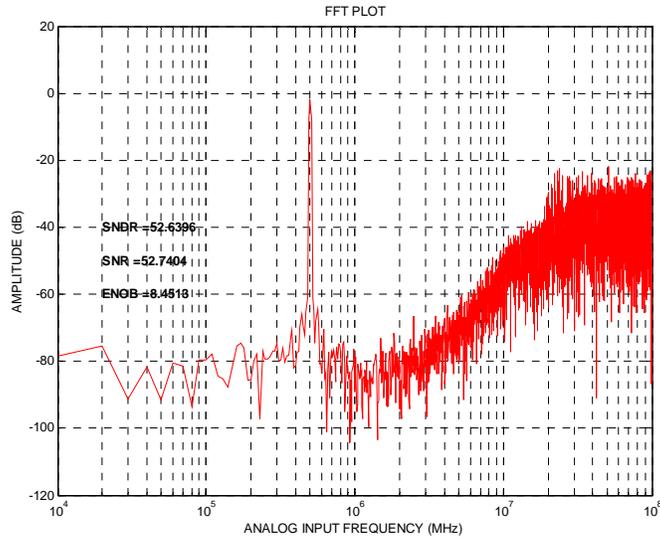
Save the changes to the **test.par** file, and start the CppSim simulation by clicking on the **Compile/Run** button in the CppSim run menu.

## B. Plotting the FFT

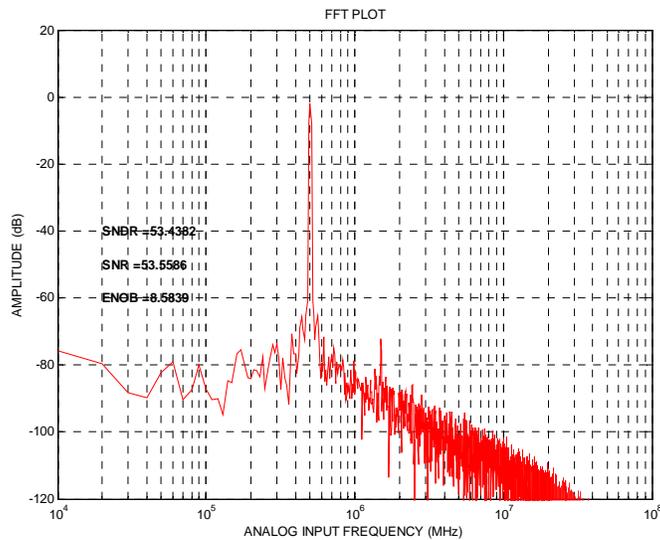
Once the CppSim simulation has completed, FFT's of the ADC output (Figure 6) and the optical modulator output (Figure 7) can be generated with the help of MATLAB. The plots shown below were generated using the script (**snr\_plot.m**) included in the distribution of the **OpticalSD\_Examples** library. The script is executed by typing:

```
[SNR, SNDR, ENOB] = snr_plot('test_fft.tr0','sd_out',1)
[SNR, SNDR, ENOB] = snr_plot('test_fft.tr0','optmod_out_accum',1)
```

Here, a 39.9995 GHz RF carrier is sub-sampled by a 200 MHz repetition rate mode-locked-laser with less than 10 fs of RMS timing jitter in the 2 MHz bandwidth of interest. The baseband signal resulting from the sub-sampling operation should then ideally look like a 500 kHz tone. By studying the FFT of the optical modulator output, it is clear that the optically down-converted signal incurs 3<sup>rd</sup> harmonic distortion and a noise skirt due to the jitter of the sub-sampling laser source. Similarly perusing the FFT of the ADC output reveals that the SNDR is degraded by 1-2 dB due to photodiode shot noise and shaped quantization noise at the edge of the 2 MHz bandwidth.



**Figure 6:** 10-million point FFT of the optical-electrical CT Sigma-Delta ADC output



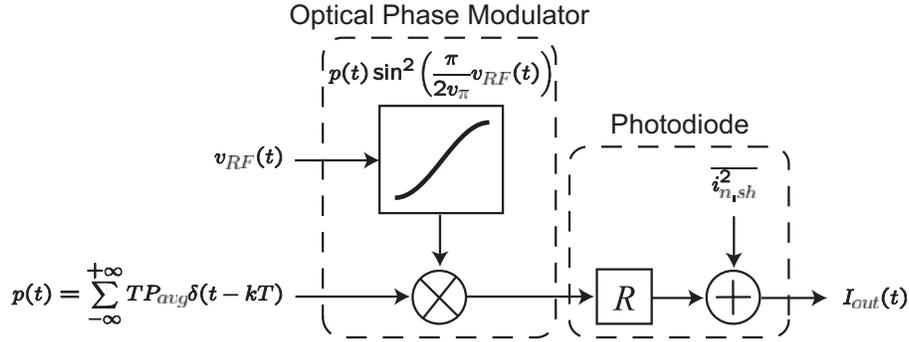
**Figure 7:** 10 million point FFT of the optical modulator output after being processed by the accumulate and dump filter

## Examining Non-Idealities

### A. Optical-Electrical Front-End Noise and Non-Linearity

In this section, a simple analytical model for noise analysis of the optical-electrical front-end is derived. As shown in Figure 8, the model includes non-linearity from the optical modulator and shot noise from the photodiode. Behavioral simulation results from

CppSim are used to verify the analytical model as well as to determine the impact of system non-idealities that cannot easily be described or evaluated analytically.



**Figure 8:** Model for noise analysis, which includes modulator non-linearity, photodiode shot noise, and aperture jitter of mode-locked laser.

Using the 3<sup>rd</sup> order polynomial (see Equation 3) that characterized the optical phase modulator non-linearity, the ratio of the signal power to the 3<sup>rd</sup> harmonic power, or spurious-free dynamic range (SFDR), can be described as:

$$SFDR = \frac{\left( \alpha_1 A + \frac{3\alpha_3 A^3}{4} \right)^2}{\left( \frac{\alpha_3 A^3}{4} \right)^2} \quad (8)$$

where  $A$  is the amplitude of the signal, and  $\alpha_1$  and  $\alpha_3$  are the first and third order polynomial coefficients from Equation (4). Note the optical modulator does not have any active components and should not contribute significant noise for a well designed modulator.

The photodiode is characterized by its responsivity,  $R$  (a power-to-current conversion gain), and a summing stage for the inclusion of shot noise. Shot noise is characterized by the average photodiode current, which can be calculated as:

$$I_{avg} = R \cdot \left[ \frac{1}{T} \int_T p(t) \right] = RP_{avg} \quad (9)$$

Since shot noise is a white, wide-sense-stationary process, its power spectral density can be described as:

$$\overline{i_{n,sh}^2} = 2qI_{avg} = 2qRP_{avg} \quad (10)$$

The jitter power can be calculated using the relationship from Equation (1), which relates the SNR to the rms jitter in a given bandwidth ( $\Delta t$ ) at the carrier frequency ( $f_o$ ). Measurement of the mode-locked laser in the prototype revealed a laser jitter of

approximately 10 fs rms in a 1 kHz to 10 MHz BW. When scaled by modulator gain and signal amplitude, the total jitter power is described by:

$$P_{jitter} = \frac{1}{2}(A\alpha_1)^2(2\pi f_o \Delta t)^2 \quad (11)$$

The power spectrum of the impulse train can be determined in two different ways. Ostensibly, the most straightforward approach is to determine the autocorrelation function and then take the Fourier Transform to obtain the power spectrum. In this case, the autocorrelation function of an impulse train is also an impulse train with period  $T$ :

$$R_{pp}(t + \tau, t) = \int_{-\infty}^{+\infty} p(\tau)p(t - \tau)d\tau = (TP_{avg})^2 \sum_{k=-\infty}^{+\infty} \delta(\tau - kT) \quad (12)$$

However, the power spectrum of an impulse train is not simply the Fourier Transform of its autocorrelation function because the process is cyclostationary. In order to calculate the power spectrum of a cyclostationary process, the average autocorrelation must first be calculated [15]:

$$\overline{R_{pp}(\tau)} = \frac{1}{T} \int_T R_{pp}(t + \tau, t)d\tau = T(P_{avg})^2 \sum_{k=-\infty}^{+\infty} \delta(\tau - kT) \quad (13)$$

The impulse train power spectrum is then the Fourier Transform of the average autocorrelation function:

$$S_{pp}(f) = (P_{avg})^2 \sum_{k=-\infty}^{+\infty} \delta\left(f - \frac{k}{T}\right) \quad (14)$$

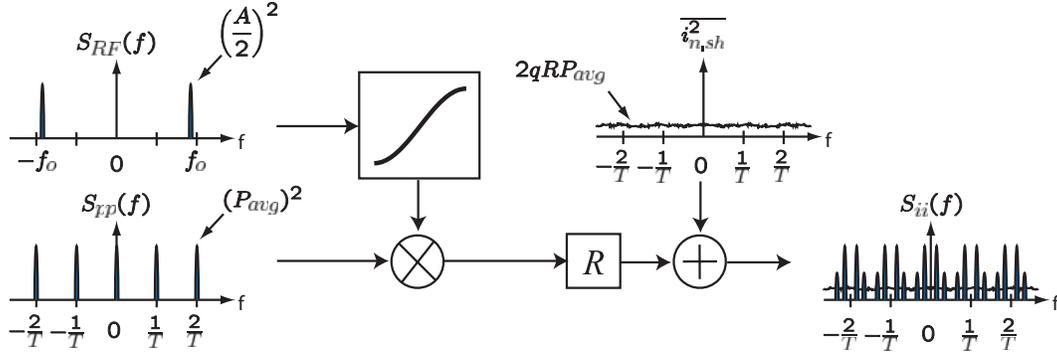
A second and more straightforward derivation of the above result makes use of Parseval's relation for total signal energy [16]:

$$\frac{1}{T} \int_T |p(t)|^2 dt = \sum_{k=-\infty}^{+\infty} |a_k|^2 \quad (15)$$

Since the impulse train is periodic, the total energy is infinite, but the power (energy per unit period) is finite:

$$S_{pp}(f) = \frac{1}{T} \sum_{k=-\infty}^{+\infty} |a_k|^2 = (P_{avg})^2 \sum_{k=-\infty}^{+\infty} \delta\left(f - \frac{k}{T}\right) \quad (16)$$

Using the power-spectral density expressions from Equations (10) and (14), a frequency domain picture of the optical-electrical front-end can be derived, and is shown in Figure 9.



**Figure 9:** Frequency-domain view of the optical-electrical front end

Using the results from the above derivations, the SNDR of the optical sub-sampling receiver is calculated to be:

$$SNDR = \frac{P_{signal}}{P_{noise}} = \frac{\left( \alpha_1 A + \frac{3\alpha_3 A^3}{4} \right)^2}{P_{jitter} + 2qRP_{avg} \cdot f_{BW} + \left( \frac{\alpha_3 A^3}{4} \right)^2} \quad (17)$$

where

$$\alpha_1 = \frac{1}{2} P_{avg} \cdot \frac{\pi}{v_\pi}$$

$$\alpha_3 = -\frac{1}{24} P_{avg} \cdot \left( \frac{\pi}{v_\pi} \right)^3$$

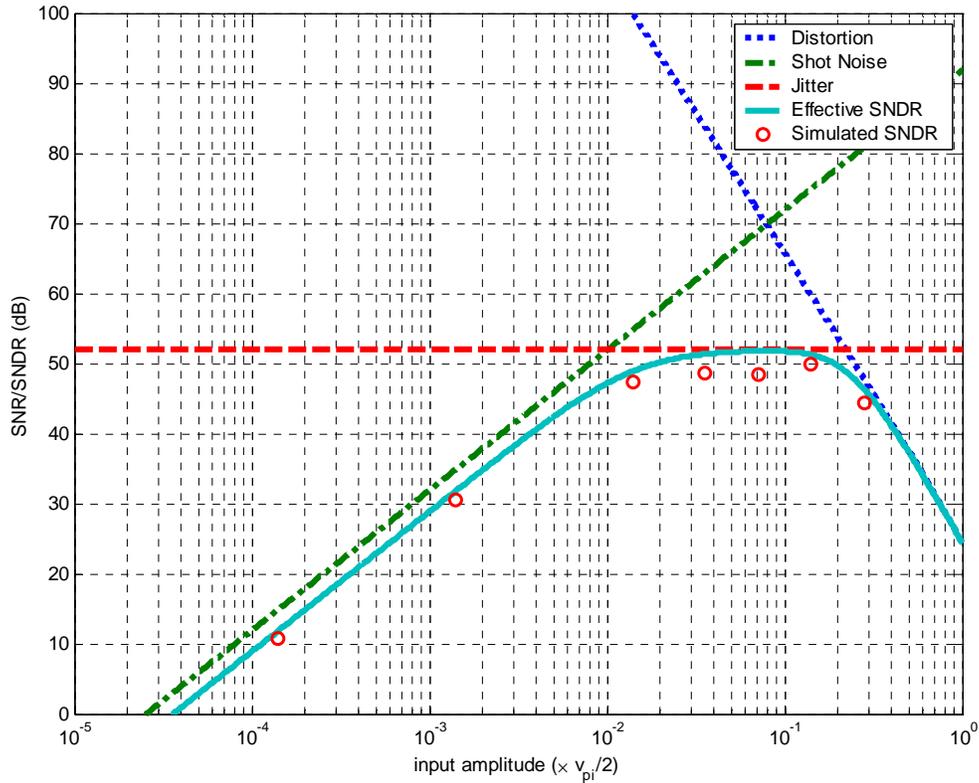
$$P_{jitter} = \frac{1}{2} (A \alpha_1)^2 (2\pi f_o \Delta t)^2$$

and  $f_{BW}$  is the signal bandwidth. The above equation enables three observations to be made:

1. The SNDR improves with increasing optical power,  $P_{avg}$ , until the aperture jitter limit is hit
2. The SNDR of an optically sampled signal is *independent* of the laser repetition rate,  $1/T$
3. The optimal SNDR can be achieved by reducing signal amplitude,  $A$ , until the 3<sup>rd</sup> harmonic distortion equals the inband shot-noise and jitter power

The SNDR limit stated in the first observation comes straight from Equation (17). Until the aperture jitter limit is reached, the SNDR is improved by increasing the optical power such that the signal is boosted relative to the shot noise. The second and third observations require closer inspection. Oversampling confers an improved SNR only when it is followed by filtering and down-sampling, which effectively reduces the noise power in the signal bandwidth. In this case, while the mode-locked laser is oversampling the

narrowband component, there is neither filtering nor down-sampling, and hence no change in SNR. The spurious-free dynamic range (SFDR) of the receiver can be improved by reducing signal power since the fundamental,  $\alpha_1$ , is proportional to the signal amplitude  $A$  while the third-harmonic,  $\alpha_3$ , is proportional to  $A^3$ . However, signal power cannot be arbitrarily reduced due to the presence of photodiode shot noise and aperture jitter.



**Figure 10:** effective optical front-end SNDR for varying input signal amplitude (normalized by  $v_{\pi}/2$ ) assuming 5mW of optical power, a 40 GHz RF carrier frequency, and laser jitter of 10 fs in a 2 MHz bandwidth.

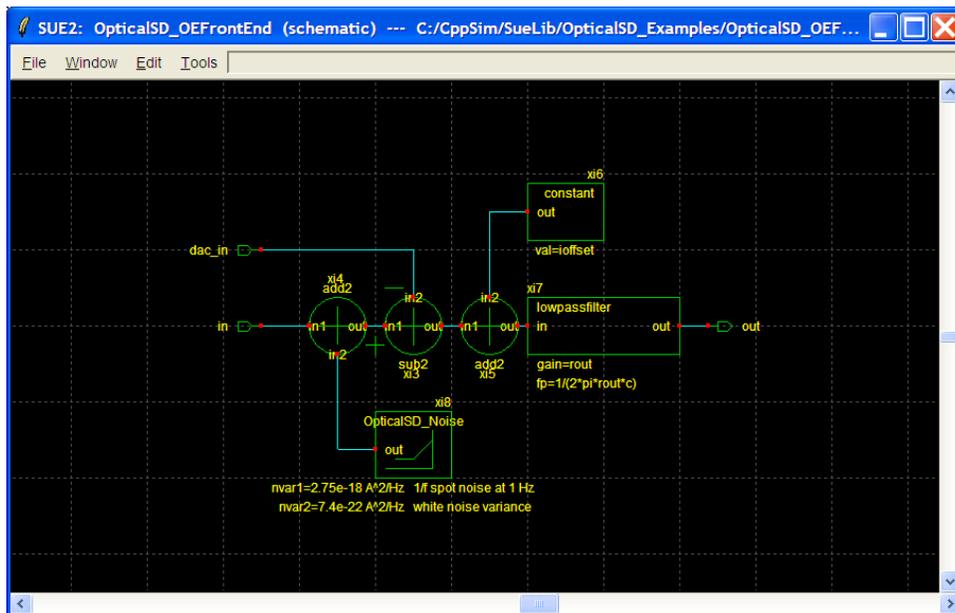
Figure 10 illustrates the tradeoffs between signal amplitude, SNDR, and jitter, and clearly shows that an optimal SNDR for a given optical power (5 mW) can be achieved when the power of the third harmonic is roughly equal to the total inband shot noise, or equivalently, when the SFDR is equal to the SNR. In this case, the optimal SNDR is approximately 52 dB over a 2 MHz BW when the input amplitude is approximately equal to  $v_{\pi}/20$ . Note that a more linear modulator would effectively remove the SNDR limitation arising from non linearity, but that the peak SNDR is still limited by the aperture jitter limit.

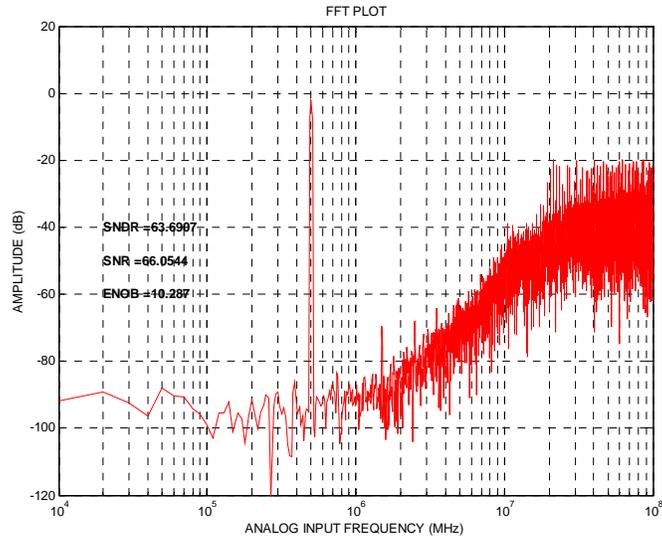
CppSim generally confirms this analysis. As indicated by the red circles in Figure 10, the simulated ADC SNR/SNDR follows the trends predicted by the analytical model, with the peak SNR/SNDR occurring near  $v_{\pi}/20$ .

## B. ADC Non-Idealities

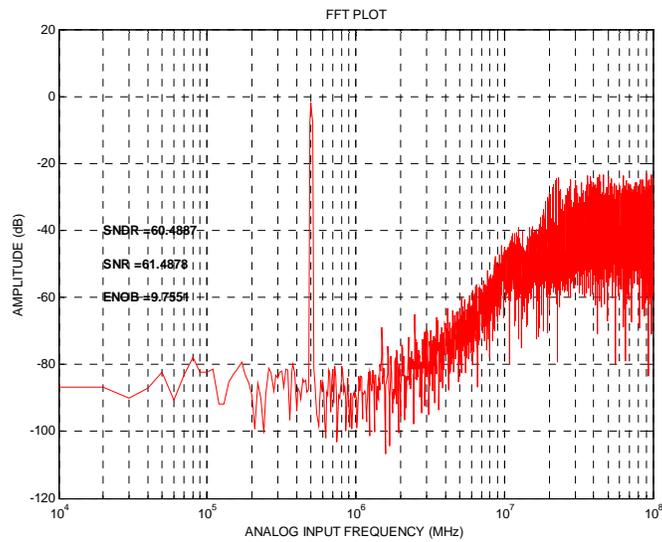
In CT  $\Delta\Sigma$  ADC's, thermal and flicker noise from the first feedback DAC and the first stage integrator have as great an impact on SNDR as the noise from the optical-electrical front end. Noise from the second feedback DAC and the second stage integrator are shaped by the gain of the preceding stage, and therefore have a smaller impact on the overall ADC performance.

The device thermal and flicker noise sources are modeled in CppSim using the **OpticalSD\_Noise** module, an example of which is shown below. The key parameters to the module are the output current spot flicker noise evaluated at 1 Hz and thermal noise density [ $A^2/Hz$ ]. As can be seen from the FFT's of the ADC output shown in Figure 11 (laser jitter eliminated for clarity), the inclusion of ADC device noise degrades the SNDR by approximately 4.5 dB. Of course, the device and photodiode shot noise floors are masked by the aperture jitter for near full-scale ADC inputs.





(a)



(b)

**Figure 11:** ADC output FFT with photodiode shot noise and device thermal and 1/f noise (a) excluded, and (b) included. Laser aperture jitter is set to zero to see the noise floor clearly.

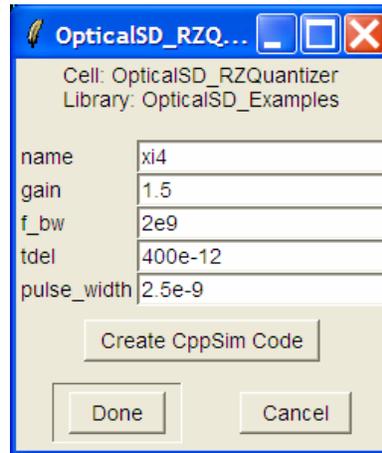
SNR and DR degradation arising from finite loop delay in 2nd order CT  $\Delta\Sigma$  ADCs have been well documented and various methods for compensating for it have been proposed [11,12]. The method of using RZ DAC pulses proposed in [11] was chosen since it enabled easy adjustment of the DAC gains for loop delay compensation. A script to calculate these DAC gains (**dac\_calc.m**) is also included in the **OpticalSD\_Examples** library. RZ DAC implementations are more sensitive to DAC jitter than NRZ implementations, but

calculations from [12] showed that the SNR for signal to clock jitter was not the limiting factor:

$$SNR_{RZ} = \left( \frac{OSR}{8} \frac{T_s^2}{\sigma_{jitter}^2} \right) \quad (7)$$

For instance, given a 1 ps rms clock jitter for the sigma-delta clock source, an OSR of 50, and clock period ( $T_s$ ) of 5 ns, a theoretically maximum  $SNR_{RZ}$  of 82 dB can be achieved. In practice, the SNR is limited to 52 dB in the prototype system due to photodiode shot noise and optical modulator distortion. Consequently, jitter from the ADC clock source is not included in the behavioral model, though it can be easily added in the same manner that the mode-locked laser jitter is modeled.

Feedback loop delay is also modeled explicitly in CppSim, and can be modified by double clicking on the **OpticalSD\_RZQuantizer** module (see below), and specifying a value for the delay variable **tdel**. The delay is also implicitly modeled through the finite gain bandwidths of the regenerative latch modules (**regen\_latch**) inside the quantizer module, and the DAC buffer module, **OpticalSD\_RZDriver**. Finally, the RZ pulse width can also be specified by entering in a value for the variable **pulse\_width**. As shown below, the pulse width is set to half an ADC clock period, or 2.5 ns.



While it is suppressed by the gain of the first integrator stage, non-linearity in the second stage integrator can nevertheless cause distortion, the severity of which depends on the output voltage swing of the first integrator. Non-linearity and offset in the second stage integrator are modeled in the module **OpticalSD\_2ndIntegrator** by using a third-order polynomial to describe the transconductance:

$$i_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3$$

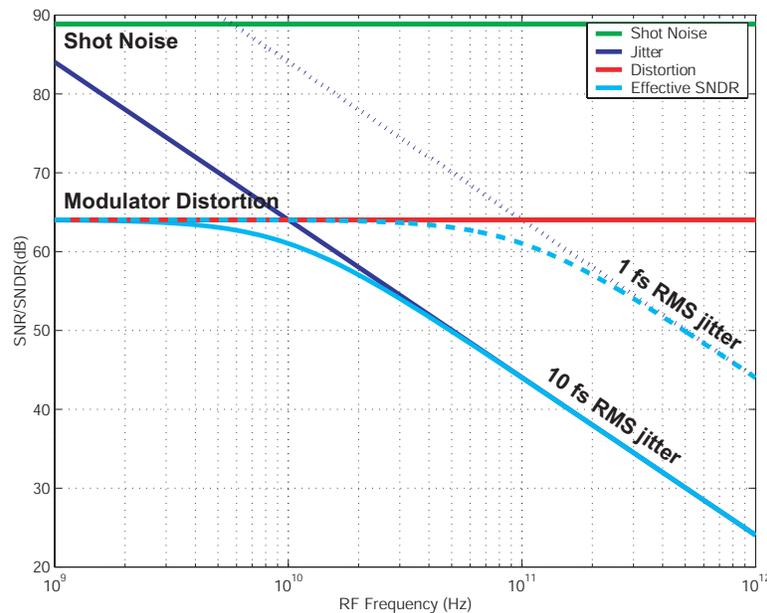
The ideal transconductance of the integrator is expressed by the  $a_1$  term, offset is characterized by the  $a_0$  term, and nonlinearity by the  $a_2$  and  $a_3$  terms. These coefficients can be obtained from a regression analysis of the DC transfer characteristics of the

summing amplifier in HSPICE or SPECTRE. The finite gain of these first and second integrators are then modeled by specifying a value for the small-signal output resistance, **ROUT**.

Other non-idealities (DAC current offsets, gain mismatches, etc.) are also included in the CppSim model. As they are self explanatory in nature, the interested reader can investigate their effect at his leisure.

## Conclusion

In this tutorial, we have explored the use of high precision optical sub-sampling to achieve a high resolution down conversion of very high frequency (>10 GHz) narrowband signals. Analysis showed that the resolution of the entire system was largely determined by the aperture jitter of the mode-locked laser, the linearity of the optical modulator, and the shot noise of the photodiodes. This result was further confirmed through behavioral simulation, which showed that ADC noise, non-linearity, and other non-idealities had a negligible impact on the overall architecture resolution. We now close with a brief discussion of future optical-electrical down-conversion receivers.



**Figure 12:** effective SNDR versus down converted frequency assuming a 200 MHz repetition rate mode-locked laser with 10 fs and 1 fs RMS jitter, 5 mW optical power, and an RF input amplitude of  $v_{\pi}/20$ .

As shown in Figure 10, the maximum theoretically achievable SNDR of the receiver was largely limited by the aperture jitter of the laser and the modulator non-linearity. Early theoretical analysis of mode-locked lasers [17] has suggested that sub-femtosecond timing jitter should be attainable. With the optical community widely reporting lasers with less

than 10 fs rms jitter, sub-femtosecond precision may soon be a reality. Superimposed on Figure 12 are the SNDR tradeoff curves for 1 fs rms aperture jitter. Now, the maximally achievable SNDR of approximately 60 dB is possible even up to 100 GHz. The use of more linear optical modulators can enable this scheme to potentially achieve close to 14 bit precision at 10 GHz. However, to achieve higher resolution or to sub-sample narrowband signals at higher than 10 GHz, the aperture jitter limit will still set the maximum achievable SNDR, so that the use of a more linear modulator would offer less benefit.

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