Linearization of a Pulse Width Modulated Power Amplifier

by

Shawn Kuo

B.S., Electrical Engineering (2002)
University of Illinois Urbana-Champaign

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Masters of Science in Computer Science and Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2004

© Massachusetts Institute of Technology 2004. All rights reserved.

Author .....
Department of Electrical Engineering and Computer Science
May 24, 2004

Certified by .....
Michael H. Perrott
Assistant Professor
Thesis Supervisor

Accepted by .....
Arthur C. Smith
Chairman, Department Committee on Graduate Students

Linearization of a Pulse Width Modulated Power Amplifier

by

Shawn Kuo

Submitted to the Department of Electrical Engineering and Computer Science
on May 24, 2004, in partial fulfillment of the
requirements for the degree of
Masters of Science in Computer Science and Engineering

Abstract

Currently, the cellphone industry is moving towards an integrated CMOS solution for power amplifiers. Cheaper phones for consumers and better bottom lines for companies are the result of this. The goal of this thesis is to investigate the use of pulse width modulation in a high efficiency integrated CMOS power amplifier for a wireless application. Though high efficiency CMOS power amplifiers exist in academia, the goal of this project is to explore pulse width modulation as a method of adjusting power. Pulse width modulation can potentially be used to create a higher bandwidth system. The challenge of this architecture is creating linear dynamic range. In simulations, feedback improved the pulse width modulated power amplifier linear dynamic range to 23dB.

Thesis Supervisor: Michael H. Perrott
Title: Assistant Professor

Acknowledgments

The research presented in this thesis was made possible by the help of many people in the MIT community. I would like to thank my advisor Mike Perrott who made this research opportunity at MIT possible. Ethan Crain and Scott Meninger taught me much about research and work from their industry experience. Charlotte Lau always let me know when I should go home. I would like to thank Belal Helal, Matt Park, and Min Park for accompanying me through the journey that is graduate school. Not to be forgotten from the group are Sam, Muyi, Sataporn, and Isaac. I would especially like to thank Roxann Blanchard of Analog Devices, Inc. who got me jump started on my research. I would also like to thank MIT and MARCO for funding my research.

I would like to thank my colleagues and peers around Microsystem Technology Lab (MTL). Alexandra Kern for teaching me the importance of being through. Julia Cline and Johnna Powell for being supportive. John Fiorenza, Micah O'Halloran, Andy Wang, and Albert Jerng, and the rest of μ-amp's ball for showing me the other side of circuits. I especially would like to thank Lunal Khuon for being patient when I was struggling with my 6.301/6.775/6.976 crash course. I would also like to thank Debb Hodges-Pabon for making my MTL experience absolutely wonderful in every way imaginable.

I would like to thank the crew. If it were not for you guys, I don't think I would have enjoyed my experience at MIT. Kate "Call me Kaity" Ryan who always brought spontaneity and subtle caustic humor everywhere. Amil Patel was the archrival Duke to my Illinois. Janelle was cool until that one fated trip to Puerto Rico. You're still cool, but no longer around. Hong Ma showed me what it truely means to be connected. Natalija Jovanovic was the Wendy to us Lost Boys. Karen Lee took pictures to document our journey through the firehose known as MIT. Song-Hee Paik, you are a wonderful TA and a true friend. Ming Tang, with you around there were never leftovers =). Despite everything you've shown me, Vikas, I still dont know Jack. Vivacious, thanks for sharing the Taiwan/Hunan connection with me. Most importantly, I would like to thank the man of innumerable talents, Tony Lau. Thanks for sticking by me through the times. You're ability to bend space on the basketball court never ceases to amaze me.

I would especially like to thank the members of the Men's and Women's Ultimate team. You guys provided me an outlet for frustration and success. I would especially like to thank (in alphabetical order) John Bicket, Benjie Chen, Dobson's (Jen, Kathy, and Chrissy), Dave Hoel, Tom Liptay, Peter Mayer, and Nancy Sun.

I would like to thank Paul Youn, Yuriy Brun, and Olivia Cheo for helping edit my thesis in a time of need. If you guys didn't help me in my last minute of need, I wouldn't have graduated on time. I would like to especially thank my housemates Tyrone Hill, Stephen Kohen, and Chris H. Rycroft. You guys made it fun to live there. I really appreciated how we would help each other out in the best interest of everyone. I think that made ClubUK special.

Finally, I would like to thank my parents, Shih-Yee and Chi-Jye, for their loving support. I would not have made it this far if I had not been brought up under their supervision. I would also like to thank my older brother, Peter, for constantly challenging me to be ambitious.

Contents

List of Figures

Chapter 1

Introduction

In recent years, wireless communications devices such as cellular phones have propagated to every phase of modern day life. In past years, children would have to call from a phone booth to tell their parents they need a ride home. Today, kids can call from their cell phone in the bus so that their parents will be there when the bus pulls in. As cellular phones become more readily available, solutions will become cheaper and their batteries will last longer. One significant contribution to both these factors is the power amplifier. The cost can be reduced by building an integrated chip. The battery life can be increased by designing a more efficient power amplifier.

One way to reduce cost is by building an integrated power amplifier. If any off-chip components must be used, the assembling cost will increase. The cost can be further reduced by laying out the chip carefully. By minimizing the area of the chip, the mask cost to create the chip will be reduced.

The battery life of a cellular phone is heavily influenced by the power amplifier. Since power amplifiers consume a significant proportion of the transmitter power, any efficiency improvement in the power amplifier will improve the battery life.

1.1 Background Information

There are two general types of power amplifiers (PA)– linear PAs and switch mode PAs. Linear PAs output scaled versions of the input at the expense of efficiency. In contrast,

switch mode PAs offer better efficiency but are constrained to a constant amplitude. In practical designs, efficiency enhancing techniques are used on linear PAs to meet the requisite efficiency while maintaining its linearity. Similarly, switch mode PAs vary their power supply to meet the necessary linearity requirement while keeping its efficiency high. Since one of the goals of this design is high efficiency, a switch mode PA will be used.

Switch mode PAs run on one general principle- minimizing the power dissipated in the transistor. The ideal case would be if the transistor behaved as a switch. When the switch is open, no power is dissipated since there is no current is flowing. When the switch is closed, no power is dissipated since there is no voltage across the switch. Since transistors are not perfect switches, the power can be minimized by making sure current and voltage are never high simultaneously. Traditionally, there are three classes of high efficiency power amplifiers that try to accomplish this goal. These are class D, E, and F power amplifiers.

1.1.1 Switch Mode Power Amplifiers

The class D power amplifier is built on a push-pull pair driving a matching network. This network is efficient for low frequencies where the switching time is small compared to the operating period. At high frequencies, the transition times become a large enough part of the entire period that the efficiency decreases drastically. Class D amplifier is only efficient up to the tens of megahertz range[2].

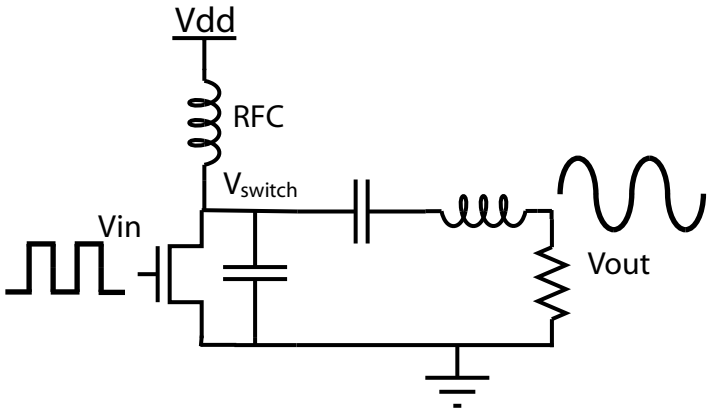

Figure 1-1 Standard class E power amplifier topology.

The class E power amplifier, shown in Figure 1-1, has the standard one transistor switch

connected to a radio frequency choke (RFC). The inductor is called a RFC since it is large enough relative to the switching period that it behaves as a constant current source. Together, the RFC and the transistor drive the class E network that is designed to create a high efficiency condition. The conditions are that the switch voltage and slope must be zero when the switch turns on. This makes sure there is never high voltage and current at the same time. Zero slope turn on permits the power amplifier to run efficiently even when the rise and fall times of the input take up to 30% of the switching period. The disadvantage with this switching technique is that the switch voltage waveform peaks at about three times the supply voltage[9]. For a given breakdown voltage, a class E design will not generate as much output power as other topologies.

The class F power amplifier exploits the properties of quarter-wavelength transmission lines. A quarter-wavelength transmission line has the following property:

$$Z_{Left} = \frac{Z_o^2}{Z_{Right}} \tag{1.1}$$

The impedance looking into the left of the transmission line is the characteristic impedance squared divided by the impedance to the right of the transmission line. This property is exploited using a parallel RLC tank as shown in Figure 1-2. At the fundamental frequency, the impedance will be at the designer's specification. At odd harmonics, the tank will be a short so the drain will see infinite impedance. At the even harmonics, the transmission line will look like a half-wavelength transmission line, or virtually a short. Therefore, even harmonics will not contribute to the drain voltage waveform. Since the odd harmonics see infinite impedance, the drain voltage will behave as the square wave that the input drives. For low gigahertz frequencies, the transmission line needs to be on the order of centimeters. Since this isn't very practical, an alternative architecture is to use a series of RLC tanks set at each of the odd harmonics to approximate the transmission line. Only a few tanks are necessary since most of the power is in the low order harmonics[6]. The class F architecture does not stress the transistor as much so more power can be generated per device. Efficiency for class F is similar to class E.

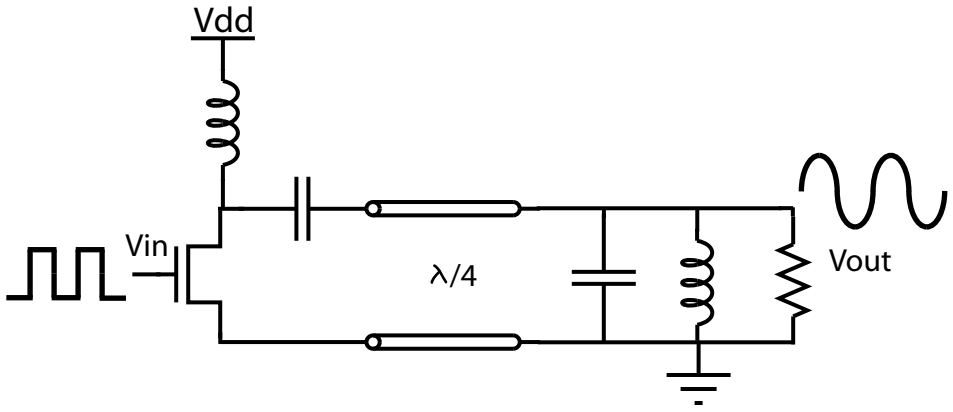

Figure 1-2 Standard class F power amplifier topology.

1.2 PWM Power Amplifier

This goal of this thesis is to look at a highly efficient integrated CMOS linear power amplifier architecture. In recent history, there have been several published CMOS radio frequency power amplifier designs. Aoki, Kee, et al. designed a 2.4 GHz power amplifier that runs at 41% efficiency[1]. Tsai and Gray designed a 1.9 GHz class E power amplifier that delivers 1 Watt at 48% efficiency[11]. Mertens and Steyaert designed a 700 MHz class E power amplifier that delivers 1 Watt at 62% efficiency[7]. There are a few other notable CMOS power amplifier designs, but they all vary their power supplies to reach the requisite output power[3, 12, 4]. In practice, varying the power supply is done by using a low power class S modulator that takes the input and output waveforms to determine the necessary supply voltage.

Instead of using a class S modulator to vary power, the proposed power amplifier architecture will use pulse width modulation. In this architecture, power is varied by changing the duty cycle of the input pulse, which should be inherently faster than varying a sturdy power supply. This architectural change should result in the ability to build higher bandwidth systems. The complete system can be seen in Figure 1-3. Typically, when data is transmitted, it is converted from a constellation point to a small sinusoidal signal that is sent to the power amplifier. In this architecture, the constellation can be directly sent to the power amplifier as polar coordinates. The amplitude of the constellation controls the output power. The phase of the constellation controls the phase at the output through the

voltage controlled oscillator.

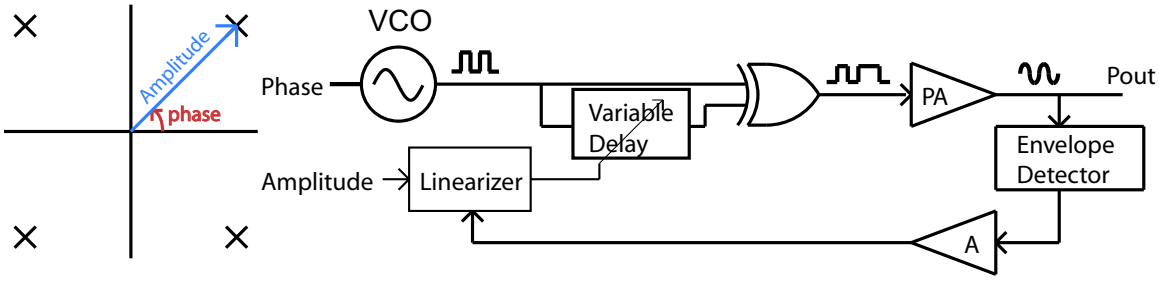

Figure 1-3 Proposed pulse width modulated power amplifier architecture.

For this architecture, a high efficiency class E power amplifier will be used. Inherently, the class E power amplifier is tolerant to slewing in the PWM edges which will be useful in controlling the power. The class F is a strong candidate, but a non 50% duty cycle square wave creates even order harmonics in the drain voltage. Since the class F power amplifier shorts even harmonics, the drain voltage may not create high efficiency switching conditions. Also, the class E PA requires fewer components allowing for a smaller, more easily integrated solution. The class D power amplifier is not a viable option at gigahertz speeds.

For a PWM power amplifier architecture, it is already known that limitations in the slew rate will strongly affect the dynamic range[6]. When the pulses get small enough that they no longer reach the supply voltage, the area of the pulse will become hard to control. When that happens, it will become increasing difficult to keep a steady output power. For $0.18\mu m$ CMOS technology, the rise and fall times are around 40ps or 4% of the period at 1 GHz. Since the circuit will be driving a large transistor, the rise and fall times may be longer than that.

In this thesis, three points will be shown. The first is that the PWM power amplifier architecture can be tuned for improved performance. It can be tuned for high efficiency at small duty cycles or large duty cycles. Also, there is a maximum power versus maximum efficiency tradeoff. These tuning tradeoffs will be discussed in chapter two. The second point is that a behavioral model of the power amplifier can be built from the fundamental components of the class E power amplifier. This behavioral model is nearly as accurate as HSPICE while running many times faster. This behavioral model is built in chapter

three. Using the behavioral model, the power amplifier will be shown to be very nonlinear. The last point is that techniques can be applied to linearize the power amplifier. The two techniques proposed are linearizing with a precompensating "linearizer" block and with feedback. Since the duty cycle to output power transfer curve can be calculated a priori, the "linearizer" block can compensate for the nonlinearity. Similarly, feedback can be used to linearize the input to output relationship using a peak detector. These linearization techniques are shown in chapter four. Chapter five summarizes the results.

Chapter 2

PWM Class E Power Amplifier

This chapter will examine class E power amplifier design and how the system operates with a pulse width modulated (PWM) input. From the base design, the system can be tuned to meet different operating needs. The system can be tuned for high output power or high efficiency. Also, the system can be designed for high efficiency at small or large duty cycles.

2.1 Class E Power Amplifier Design

The class E power amplifier, pictured in Figure 2-1, is a switch based power amplifier that achieves high efficiency at a constant power output. High efficiency can be obtained by keeping the voltage-current product (power dissipation) in the NMOS small. In the class E architecture, this is done using a technique called zero voltage switching (ZVS). This technique ensures that the switch voltage is near zero when the NMOS turns on. The matching network, consisting of a shunt capacitor and a series resonant tank, is designed to achieve ZVS and set the slope of the switch voltage to zero when the NMOS turns on. This allows for a long rise or fall time in the input waveform by keeping the voltage low while the current starts to turn on. At the turn off transition, little power is lost as well. The shunt capacitor, C_1, keeps the voltage low while the current shuts off. Most of the power loss occurs when the switch is on. The current through the drain is large enough that even with a small "ON" resistance, the power loss is still significant. A typical voltage and current

drain waveform is shown in Figure 2-2. The switch voltage reaches zero with zero slope when the switch turns on.

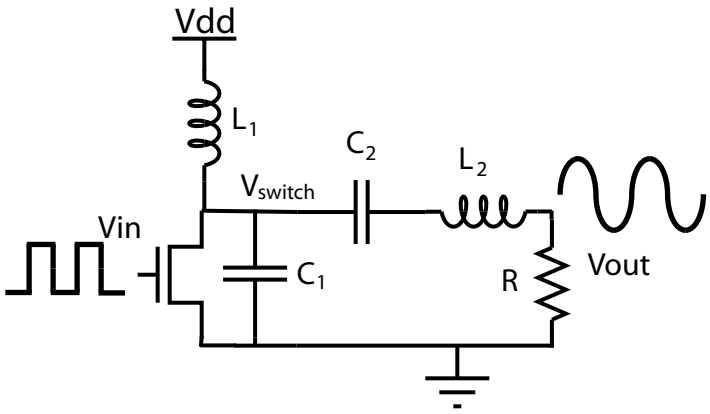

Figure 2-1 The topology for a class E power amplifier.

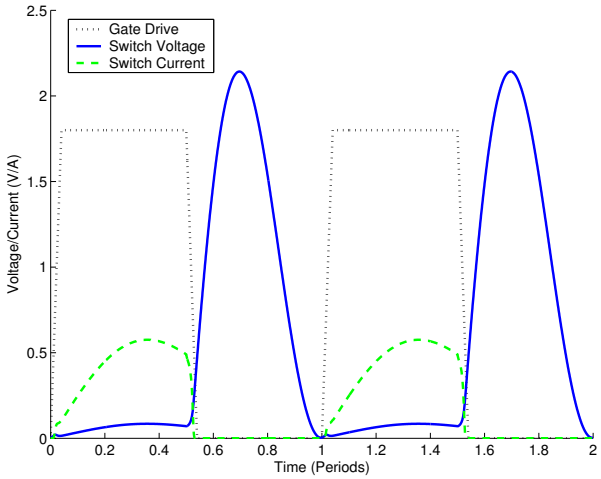

Figure 2-2 A typical drain current/voltage waveform.

The design of class E power amplifiers can be done analytically if the RF output is assumed to be sinusoidal (i.e. infinite loaded quality factor (Q), Q_L). When the loaded Q is not infinite, the solution can not be derived analytically. The finite loaded Q in any practical design results in a 10% to 38% error in the actual output power compared to the infinite Q analyically derived output power[8]. This error gets larger as the loaded Q becomes smaller (Q_L must be greater than 1.79 by design). To account for the output power error from the loaded Q, design equations that take into account loaded Q will be used. These equations are reproduced below from [8].

$$P = \frac{Vcc}{R}\,0.576801\left(1.0000086 - \frac{0.414395}{Q_L} - \frac{0.577501}{Q_L^2} + \frac{0.205967}{Q_L^3}\right) \quad (2.1)$$

$$C_1 = \frac{1}{2\pi f R\left(\frac{\pi^2}{4}+1\right)\frac{\pi}{2}}\left(0.99866 + \frac{0.91424}{Q_L} - \frac{1.03175}{Q_L^2}\right) + \frac{0.6}{(2\pi f)^2\,L1} \quad (2.2)$$

$$C_2 = \frac{1}{2\pi f R}\left(\frac{1}{Q_L - 0.104823}\right)\left(1.00121 + \frac{1.01468}{Q_L - 1.7879}\right) - \frac{0.2}{(2\pi f)^2\,L1} \quad (2.3)$$

$$L2 = \frac{Q_L R}{2\pi f} \quad (2.4)$$

Using $0.18\mu m$ CMOS technology, the maximum drain to source voltage is around two volts. Voltages greater than that will induce the hot carrier effect. Hot carriers are high energy (strong lateral electric field) electrons that are sent across the channel. Over time, the electrons bombarding the channel will degrade the performance of the device[10]. In a class E power amplifier, the peak switch voltage is around three times greater than the power supply. This limits the power supply to 0.6 volts with some safety margin.

The other consideration is the highest feasible Q of the matching network. In practice, the matching network's Q is typically five due to the parasitic resistances in integrated capacitors and inductors. The parasitics limits the loaded Q, Q_L, in the design equations and affects the tank resistance, R. Ideally, the tank resistance would be as small as possible to maximize output power. However, since the tank resistance needs to be converted into a 50Ω antenna, it is limited. Using a standard L-match, the resistor conversion ratio is set by the Q as shown in Equation 2.5[6]. The finite Q limits the tank resistance to about 2Ω.

$$R = \frac{R_{antenna}}{Q^2 + 1} \quad (2.5)$$

Using the power supply and tank resistance requirement, a 1 GHz class E power amplifier can be designed. The maximum power output can be calculated using Equation 2.1. To get an output power of 100mW with a power supply of 0.6V, the tank resistance must be 1.86Ω. Choosing a reasonable value of 2nH for L_1, the radio frequency choke (RFC), the resonant series tank and shunt capacitors can be calculated using Equation 2.2 and Equation 2.3 respectively. The resulting shunt capacitor, C_1, is 25.5pF and the resonant

capacitor, C_2, is 20.5pF. The resonant inductor, L_2, in the tank is calculated to be 1.5nH using Equation 2.4.

Simulating the resulting system in HSPICE results in the graph in Figure 2-3(a). The first thing to note is that the switch voltage does not return to zero nor does it have zero slope at turn on. This results in reduced power amplifier efficiency.

For improved efficiency, the class E matching network can be tuned. Since the design equations can't take into account the switch on resistance, tuning the class E network is well understood and expected. Based on the current zero slope point in the switch voltage waveform, matching network values can be adjusted to create the zero voltage switching condition. In the current design shown in Figure 2-3(b), the shunt capacitor C_1 can be reduced to create the zero voltage switching condition.

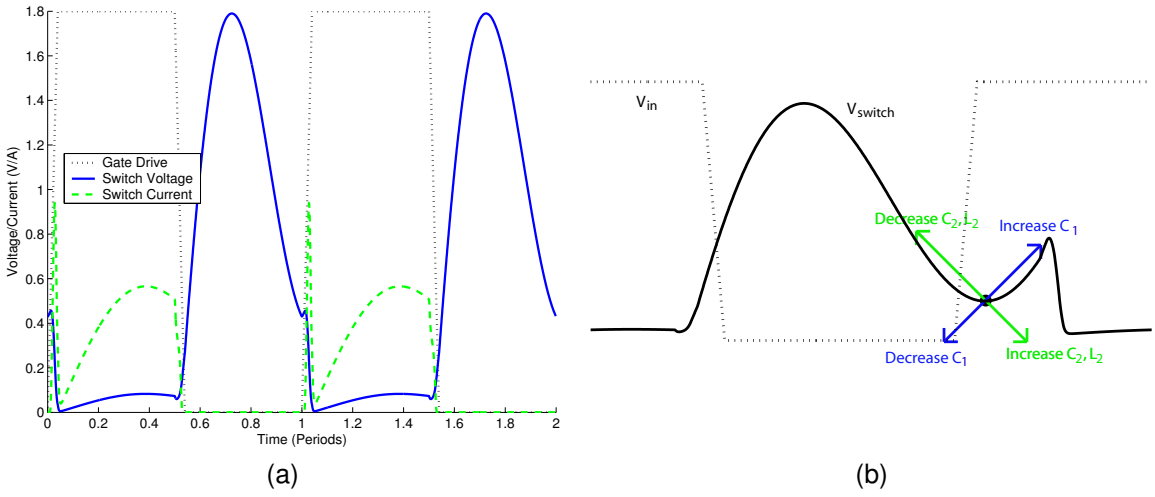

Figure 2-3 Class E power amplifier switch IV characteristic for current design (a). Tuning waveform based on N. Sokal's paper[8](b).

However, the efficiency of the system as a whole is the figure of merit. The efficiency at other duty cycles are equally important. If the 50% duty cycle isn't as efficient, but other duty cycles are more efficient, the overall system benefits. Before tweaking the matching network, the effect at other duty cycles must be analyzed.

2.2 Pulse Width Modulated Power Amplifier

The classical class E power amplifier has a constant power output since the input is a square wave with a 50% duty cycle. By using pulse width modulation (PWM) to vary the duty cycle, the output power can be changed. This PWM system can be designed as shown by the block diagram in Figure 2-4. A voltage controlled oscillator (VCO) outputs a square wave with a 50% duty cycle. The XOR can generate a square wave of any duty cycle by controlling the relative phase between two 50% duty cycle square waves. This variable duty cycle square wave is used to drive the class E power amplifier to produce a variety of output powers. The amplitude input sets the delay to generate the appropriate duty cycle. The phase input sets the phase delay of the VCO square wave.

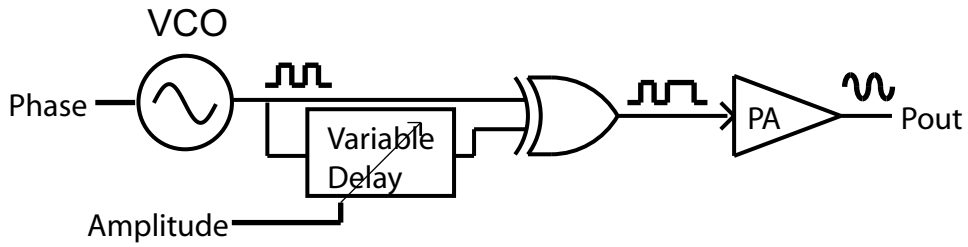

Figure 2-4 Block diagram of a pulse width modulated power amplifier.

Simulating the system in HSPICE, the periodic steady state output power and efficiency can be calculated at all duty cycles. The simulation results are summarized in Figure 2-5(b). At small duty cycles, the RFC has a small fraction of the cycle to charge up. This results in a low amount of energy being injected into the matching network and hence low output power. At large duty cycles, the RFC charges up much energy in a cycle, but releases it in such a quick pulse that it has very little fundamental frequency content. This also results in low output power. Output power is highest in the duty cycles between these two extremes. As expected, the efficiency is highest around 50% duty cycle since that is approximately where ZVS occurs. This can be seen in voltage and current waveform plots at different duty cycles shown in Figure 2-5(a).

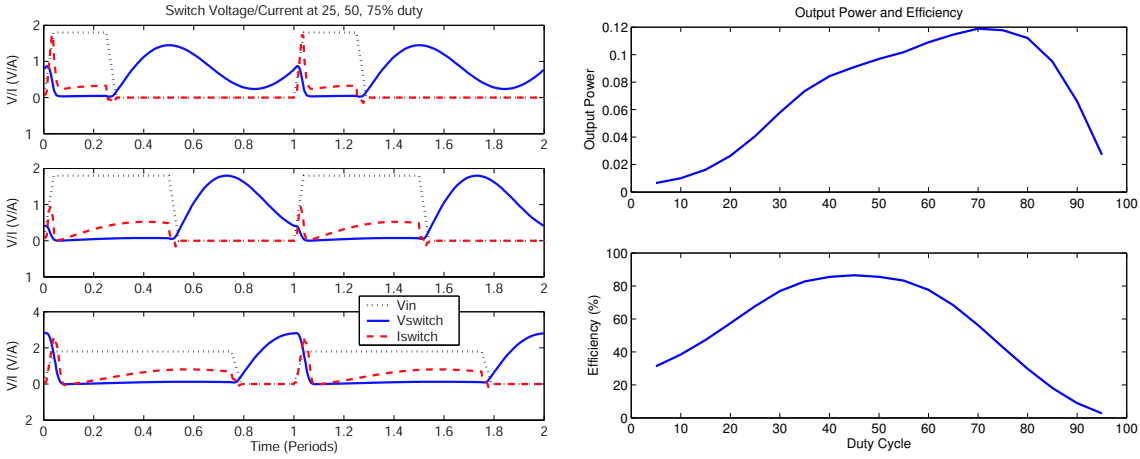

Figure 2-5 Periodic steady state switch IV waveforms at 25, 50, 75% duty cycle (a). Periodic steady state output power and efficiency at various duty cycles (b).

2.3 Class E Power Amplifier Behavior

In order to tune the network for optimal operation, the waveform behavior must be understood. With some equations, it may be possible to get an intuitive feel for how the system will behave as the matching network is changed. First, the waveform behaviors are analyzed when the switch is open and closed.

When the switch is closed as shown in Figure 2-6, the shunt capacitor is shorted and the series RLC resonates at the switch frequency. During this time, the RFC stores magnetic energy that will be released when the switch opens. It is assumed that the RFC is large enough relative to the switching period that the RFC can be modeled as a current source. When the switch is open, the current source releases energy into the network. This energy sloshes back and forth between the shunt capacitor and the series RLC tank. This sloshing allows the switch voltage to return to zero when the switch closes.

The description above is a very high level overview of the class E matching network voltage and current behavior. In the following subsections, a more mathematical view will be presented. Though a closed form solution for power output and efficiency will not be determined, the change of direction in the output power and efficiency can be determined for changes in the component values of C_1, C_2, and L_2.

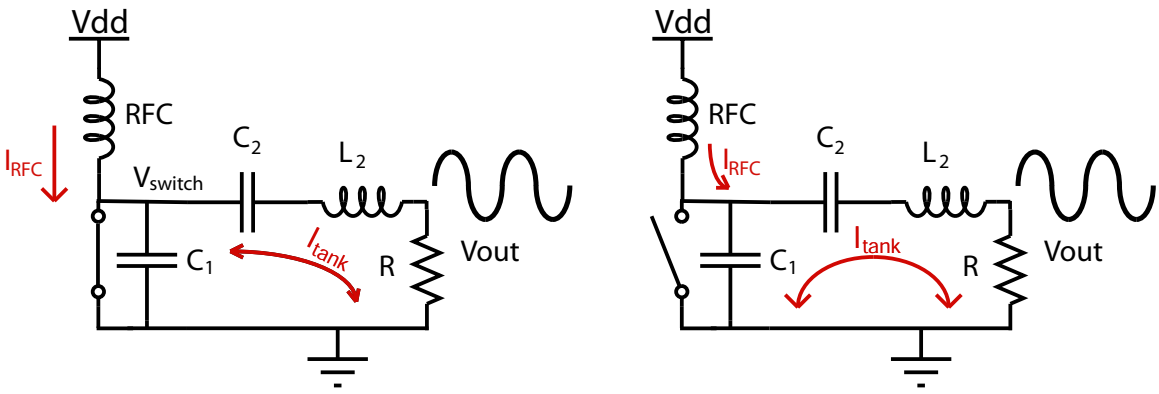

Figure 2-6 Direction of current flow when the switch is open and closed.

2.3.1 Output Power

The output power can be calculated using a series of Fourier transforms. The time domain switch voltage waveform is the convolution of the delta train at intervals of the period T with the switch voltage waveform over a period. In the frequency domain, the switch voltage frequency content is just the multiplication of the delta train at intervals of the fundamental frequency and the switch voltage frequency content of a period. Through experimental analysis, the switch Fourier transform has the form of a sin(f)/f response evaluated at the switch frequency and its harmonics. The output power can be calculated by figuring out the voltage transfer function of the series RLC tank shown in figure 2-7. This tank is a filter that can be characterized in terms of two parameters- the center frequency and quality factor. The center frequency is given by Equation 2.6, and the quality factor is given by Equation 2.7[5].

$$\omega_{0tank} = \frac{1}{\sqrt{L_2 C_2}} \tag{2.6}$$

$$Q_{tank} = \omega_{0tank} \frac{L_2}{R} \tag{2.7}$$

In a power amplifier, the output power of significance is the power of the fundamental frequency. Therefore, the deviation between the fundamental frequency and the center frequency of the tank has a strong influence in the output power. Also, a larger Q makes

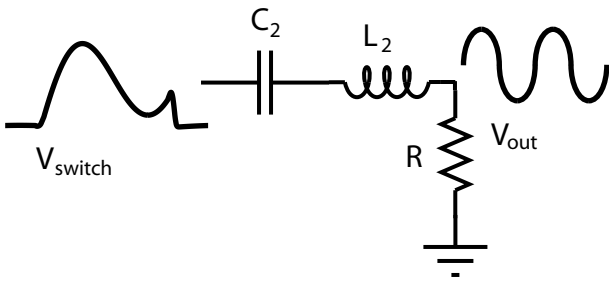

Figure 2-7 Diagram of the RLC tank that filters the switch voltage.

the filter more narrowband, which results in lower output power for a given frequency deviation. Using the change in deviation from the center frequency, the change in power output due from tuning C_2 and/or L_2 can be determined.

2.3.2 Power Amplifier Efficiency

When the power amplifier is being operated at ZVS, the dominant power loss is conduction loss from the transistor having nonzero "ON" resistance. However, when the switching is being operated away from the ZVS, conduction loss is no longer the main loss component. The dominant power loss component is the energy that is dumped by shunt capacitor, C_1, when the switch turns on. By looking at the switch voltage when the switch turns on, the power loss can be determined. However, since efficiency is a function of both output power and power loss, only an approximation for the efficiency can be obtained through analytical means.

Maximum efficiency ocurring at larger or smaller duty cycles can be determined by looking at the switch voltage. When the switch is opened, the switch voltage responds as a transient from ground to the supply voltage. The transient is given by the circuit parameters C_1, C_2, and L_2. Since the matching network, shown in Figure 2-8, is lightly damped, it will oscillate at the frequency determined by the components. This frequency is given by Equation 2.8, and the quality factor (Q) of this circuit is given by Equation 2.9[5].

$$\omega_{0match} = \frac{1}{\sqrt{L_2\left(\frac{C_1C_2}{C_1+C_2}\right)}} \tag{2.8}$$

$$Q_{match} = \omega_{0match}\frac{L_2}{R} \tag{2.9}$$

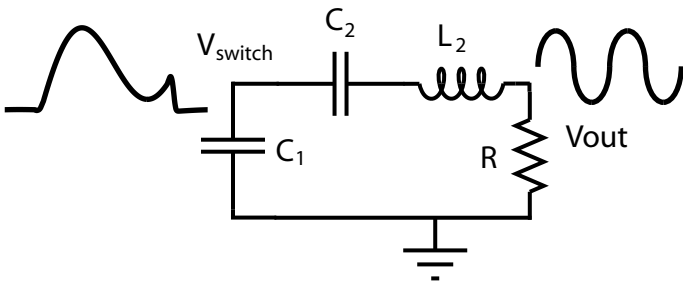

Figure 2-8 Diagram of the matching network that determines how the switch voltage behaves.

If the matching network resonants at a higher frequency, the ZVS point occurs earlier in the cycle. Higher efficiency will occur at larger duty cycles since the switch needs to be open for less time. If the matching network resonates at a lower frequency, then the ZVS condition will occur later in the period. In this case, higher efficiency will occur at smaller duty cycles. If one of the components in the matching network were altered, the change in resonant frequencies will determine whether higher efficiency will occur at smaller or larger duty cycles.

2.4 PWM Power Amplifier Tuning

The class E power amplifier is designed for maximum efficiency when driven by a square wave with a 50% duty cycle. When the power amplifier is driven by a pulse width modulated square wave, the efficiency is expected to drop since ZVS is violated. Since the figure of merit is system efficiency, tweaking the system may result in better overall efficiency despite breaking the ZVS condition at a 50% duty cycle. Thus, tuning the matching network is explored in this section.

The power and efficiency values are difficult to calculate for any given duty cyle and matching network. However using the methods described in Section 2.3, the direction of the change in the power and efficiency curves due to perturbations can be determined. In the following analysis, perturbations were done on three components of the matching

network– the shunt capacitor (C_1), resonant capacitor (C_2), and resonant inductor (L_2). These simulations were done in HSPICE.

2.4.1 Varying the Shunt Capacitor C_1

Increasing the size of the shunt capacitor causes the switch voltage to slow down. This can also be seen in the resonant frequency of the matching network. By increasing the size of C_1, Equation 2.8 shows that the resonant frequency is reduced. From Equation 2.6 and Equation 2.7, varying C_1 does not change the center frequency or Q of the tank. To first order, the output power should not change. However, the output power will change some since the Fourier transform of the switch voltage waveform over a period will be slightly different. In terms of efficiency, the system's maximum efficiency region is at smaller duty cycles since the voltage waveform takes longer to get back to zero slope due to the slower matching network resonant frequency.

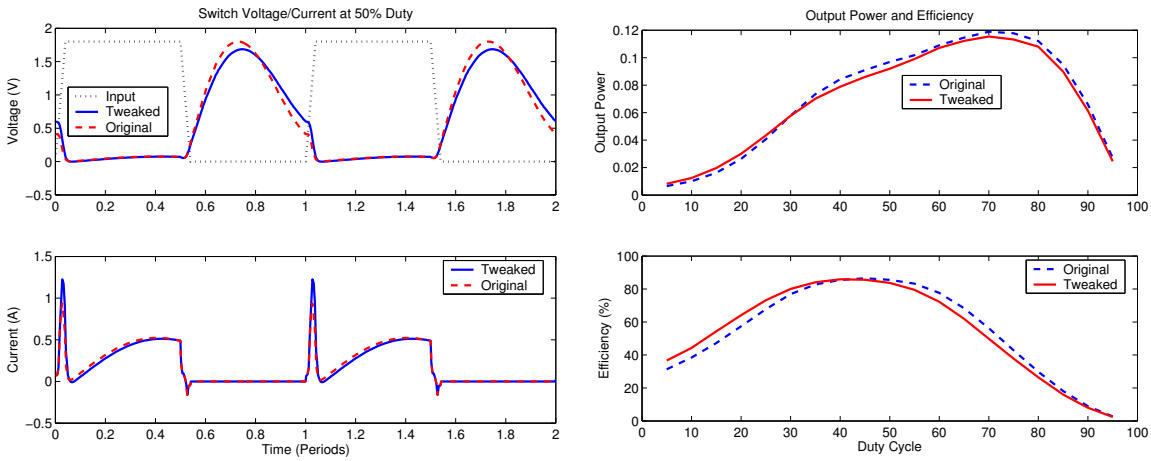

Figure 2-9 Increasing C_1: the switch voltage and current at 50% duty cycle (a) and new output power and efficiency characteristics (b).

In a simulation where C_1 was increased 20% to 30.5pF, the periodic steady state power and efficiency are shown in Figure 2-9. The power and efficiency plots behaved as expected. The center frequency and Q of the series tank stays at 0.91 GHz and 4.57 respectively. However, the resonant frequency and Q of the matching network change from 1.23 GHz and 6.14 to 1.18 GHz and 5.9 respectively. As expected, the output power stayed roughly

the same for all duty cycles and the maximum efficiency occurred at smaller duty cycles than the original system.

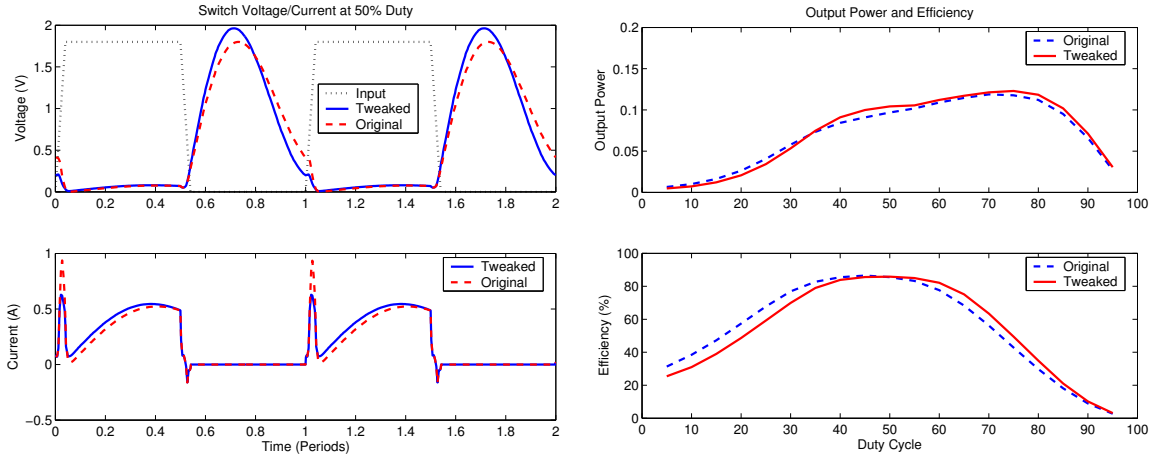

Figure 2-10 Decreasing C_1: the switch voltage and current at 50% duty cycle (a) and new output power and efficiency characteristics (b).

By decreasing the size of C_1, the exact opposite should happen. The output power should stay roughly the same for all duty cycles and the maximum efficiency occurs at larger duty cycles. In the simulation, C_1 was decreased by 20% to a values of 20.5pF. These results are shown in Figure 2-10. As before, the resonant frequency and the Q of the series tank stays the same. The resonant frequency and Q of the series tank increase to 1.29 GHz and 6.46 respectively. As expected, the output power stayed roughly the same for all duty cycles and the maximum efficiency occurred at smaller duty cycles than the original system.

2.4.2 Varying the Resonant Capacitor C_2

Increasing the resonant capacitance in the series tank changes the rate at which the energy sloshes between the shunt capacitor and the series tank. Since more energy must be moved around as a result of the increase, the resonant frequencies of the network and tank are expected to decrease. The output power is expected to decrease since the center frequency of the tank will be further from 1 GHz. High efficiency will occur at small duty cycles due to the increase in the matching network resonant frequency.

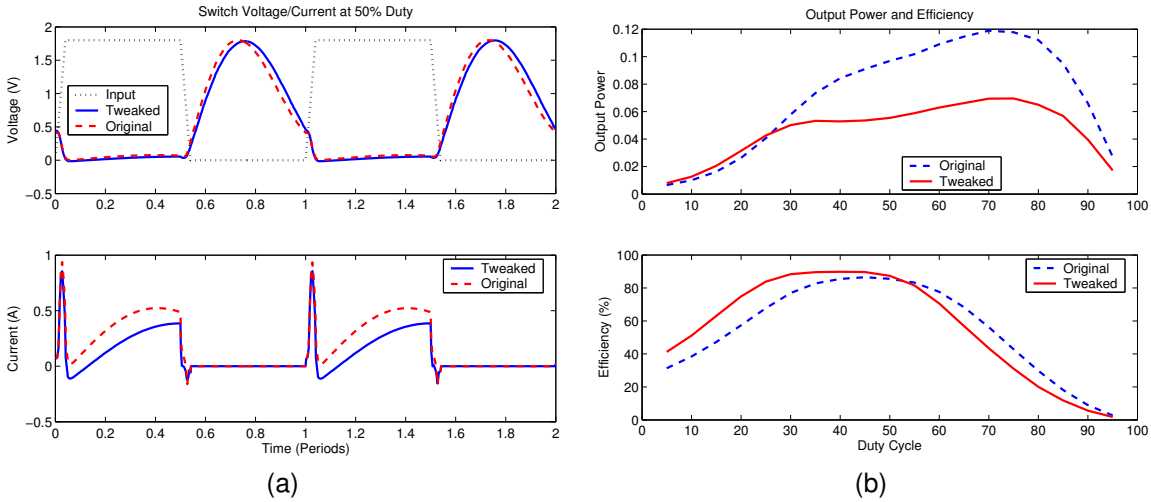

Figure 2-11 Increasing C_2: the switch voltage and current at 50% duty cycle (a) and new output power and efficiency characteristics (b).

When C_2 is increased 20% to 24.5pF, the network resonant frequency decreases from 1.23GHz to 1.17GHz. This results in better efficiency at smaller duty cycles. Similarly, the center frequency of the resonant tank moves from 0.91 GHz to 0.84 GHz, but the Q decreases from 4.57 to 4.18. This results in a lower output power. The results are shown in Figure 2-11.

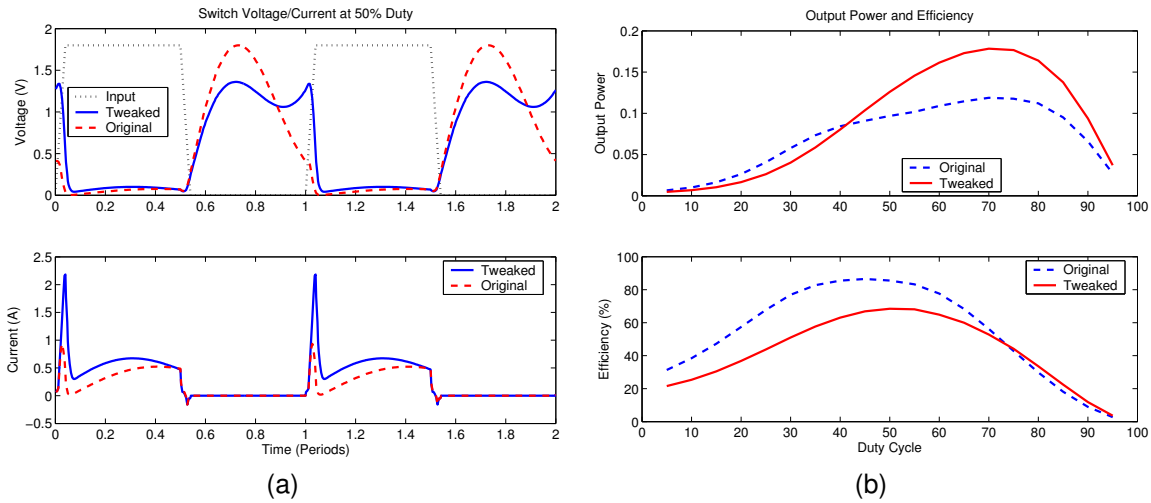

Figure 2-12 Decreasing C_2: the switch voltage and current at 50% duty cycle(a) and new output power and efficiency characteristics (b).

Similarly, decreasing the resonant capacitance in the series tank will reduce the amount of energy that needs to be sloshed. This causes the resonant frequencies to increase. When

C_2 is decreased 20% to 16.5pF, the network resonant frequency increases from 1.23GHz to 1.31GHz. This causes the system to have maximum efficiency at large duty cycles. The resonant tank center frequency and Q increase from 0.91 GHz and 4.57 to 1.02 GHz and 5.09 respectively. The combination of a higher Q and the center frequency at 1GHz causes the output power to increase tremendously over the nominal case. At large duty cycles, the power is nearly double the nominal case. The drawback is that the high output power and lower energy storage causes the switch voltage to not return to zero. This causes tremendous power loss when the switch turns on. This phenomenon can be seen in Figure 2-12.

2.4.3 Varying the Resonant Inductor L_2

Varying the resonant inductor has a similar effect as varying the resonant capacitor. By increasing the resonant inductance, the stored energy is increased and the oscillations will be slower. When L_2 is increased 20% to 1.8nH, the resonant frequency of the network decreases from 1.23GHz to 1.12 GHz. This improves efficiency at small duty cycles. The center frequency of the resonant tank decreases from 0.91 GHz to 0.83 GHz and the Q increases from 4.57 to 5.01. The net result is that the output power is much smaller than when the resonant capacitance was decreased. The results are shown in Figure 2-13.

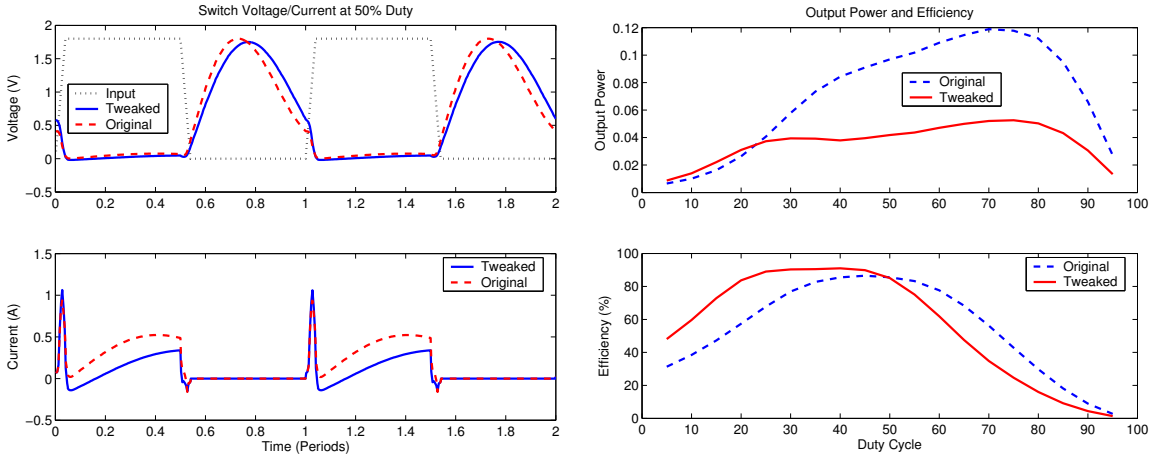

Figure 2-13 Increasing L_2: the switch voltage and current at 50% duty cycle (a) and new output power and efficiency characteristics (b).

Decreasing the resonant inductor by 20% to 1.2nH results in a higher resonant fre-

quency. The resonant frequency of the network increases from 1.23GHz to 1.37GHz. This results in the high efficiency region occurring at large duty cycles. The center frequency of the resonant tank moves from 0.91 GHz with a Q of 4.57 to 1.02 GHz with a Q of 4.08. This improves the output power to nearly twice the output power of the original design. As with increasing the resonant capacitance, the efficiency decreases since the voltage waveform does not have enough stored energy to return to zero. Figure 2-14 shows the waveforms.

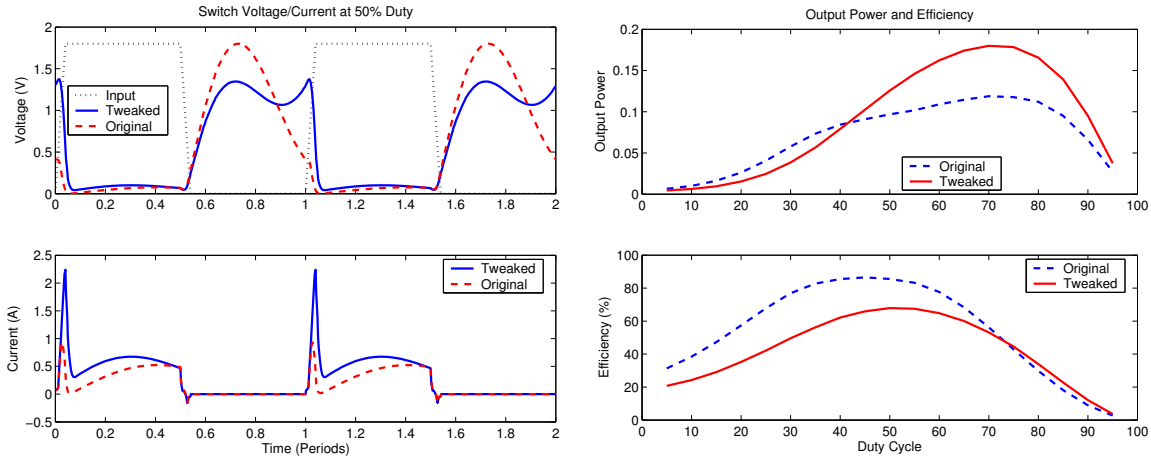

Figure 2-14 Decreasing L_2: the switch voltage and current at 50% duty cycle (a) and new output power and efficiency characteristics (b).

2.5 Summary

In this chapter, the class E power amplifier operation has been described in detail. The class E power amplifier is typically designed for maximum efficiency at a 50% duty cycle. At small duty cycles, the output power is lower and the efficiency is lower since the switch voltage does not return to zero at switch turn on. At large duty cycles, the output power is higher since the fundamental component in the switch waveform is larger, but the efficiency is reduced. Depending on system needs, the matching network can be designed to increase or decrease output power and efficiency. A summary of the tuning is shown in Figure 2-15.

Maximum efficiency can be traded off with maximum output power. Also, the maximum efficiency can be set at lower output powers or larger output powers. Depending on

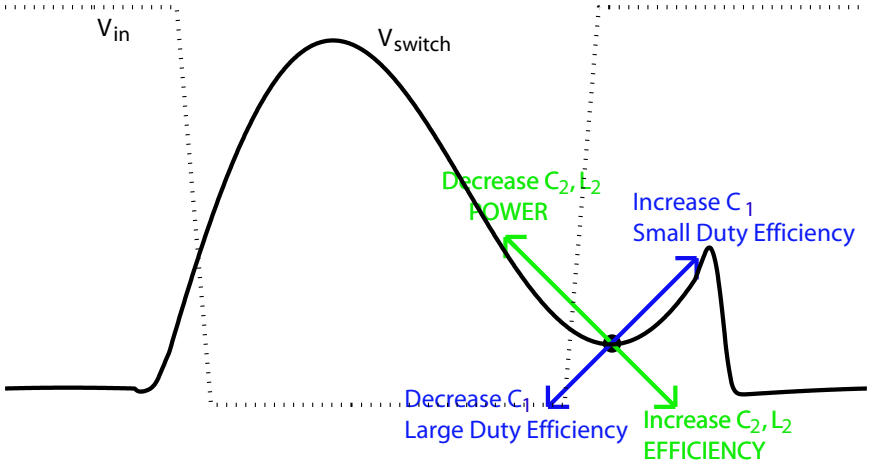

Figure 2-15 Tuning waveform with the effects of a pulse width modulated input. Based on N. Sokal's paper[8].

the system requirements, the matching network can be tuned appropriately. This will be explored in the future.

Chapter 3

Power Amplifier Modeling

In a system design, behavioral modeling must be done. Using programs such as HSPICE, which simulate every detail of every component, will lead to overly long simulation times. Generally, designers assume that the radio frequency choke (RFC) is a perfect current source and the NMOS transistor has only drain capacitance. However if inductors are built on-chip, the inductance in the RFC is small enough that this assumption is no longer valid. In the case of using a 2nH RFC, there are fluctuations in the current of at least 25%, depending on the duty cycle. The behavioral model discussed in this chapter will take into account current fluctuations in the RFC as well as most of the capacitive affects of the MOSFET. In this thesis, the behavioral simulator used is called CppSim. It is a custom C++ simulator that can be found at http://www-mtl.mit.edu/research/perrottgroup/tools.html.

3.1 Description of Behavioral Model

The class E power amplifier can be broken into three sections– a RFC, the NMOS switch, and the linear class E network. The RFC generates a current to bias the switch and drive the network. The switch controls the current drive into the class E network to produce the switch voltage V_{switch} at the drain of the switch and output voltage V_{out}. The model can be constructed by looking at each of these three components individually.

3.1.1 Radio Frequency Choke

Ideally, the RFC can be lumped with the rest of the linear network since it is another linear component. For AC behavior, this would be trivial since the RFC is connected to AC ground. However, in DC it behaves as a current source since it is large. One possible way to model this inductor is to use a current source with the transistor to drive the linear network that includes the RFC. An alternative approach, with minimal increase in computation time, is to model the inductor exactly for all frequencies. To get the output current of the inductor, the integral form of the ideal inductor equation will be used.

$$i_{L_1} = \frac{1}{L_1} \int_{-\infty}^{t} V_{CC} - V_{switch}(t)\, dt. \tag{3.1}$$

One benefit of using this approach is that the biasing current is exact for all situations including startup transients and variations in duty from cycle to cycle. This ability comes about because the biasing current is set by the feedback action from the switch voltage generated by the linear network. With a current source, you take out the feedback loop by calculating the bias current a priori across all duty cycles and temperatures. For the same reason, the current source can not simulate transients nor variations in the duty cycle. Clearly, the benefits of modeling the RFC by Equation 3.1 outweigh the added complexity.

3.1.2 NMOS Transistor

The NMOS transistor is more difficult to model. The transistor model can be broken down into two components– the DC characteristic and high frequency response. The DC characteristic can be modeled as the IV characteristic of the transistor. The BSIM3v3 model that can be found at http://www-device.eecs.berkeley.edu/ bsim3/ was used to create a CppSim module that realized the IV characteristic. Simulating a $10\mu m/0.18\mu m$ NMOS transistor at V_{GS} from 0 to 1.8V at 100mV intervals with CppSim and HSPICE, the IV curves, shown in Figure 3-1(a), are nearly identical. Looking at the error for various V_{GS} plots in Figure 3-1(b), the error is within 1% for all drain voltages above 50mV. At small drain voltages, the relative error increases, but the absolute error remains small. Since the transistor is primarily used as a switch, the error will be more significant that some other applications since

the drain voltage is small when the switch is on.

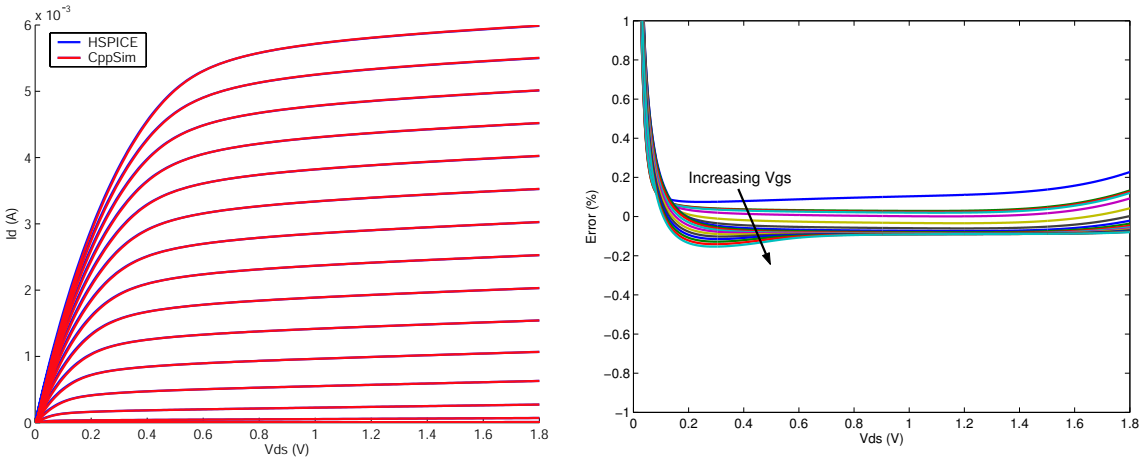

Figure 3-1 IV characteristic of an $10\mu m/0.18\mu m$ NMOS (a) and the error in the BSIM3v3 model (b).

The frequency response can be modeled by including the parasitic capacitors of the transistor. By adding all the parasitics, the model is greatly complicated. To make the model fast and relatively accurate, only the major capacitances are included. The three major culprits are the Gate-Source (C_{GS}), Gate-Drain (G_{GD}), and Drain (C_D) Capacitances. These are diagrammed in Figure 3-2.

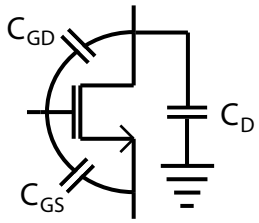

Figure 3-2 Major capacitances in a MOSFET.

The Gate-Source and Gate-Drain capacitances are caused by polysilicon gate oxide overlapping the drain and source diffusion regions. Since this capacitance is determined by the foundry process, these values are fixed and easily modeled. They can be modeled in the same way as the RFC:

$$i_{C_{gs}} = C_{ov}\frac{dV_{pulse}(t)}{dt} \tag{3.2}$$

$$i_{C_{gd}} = C_{ov}\frac{d(V_{pulse}(t) - V_{switch}(t))}{dt} \tag{3.3}$$

The Drain capacitance is caused by the depletion region between the drain and bulk. Since the depletion region expands and shrinks with changing gate voltage, this capacitance is nonlinear. The only way to model this more exactly is to change the entire NMOS model into the charge domain. However, simulations shown later in this chapter will reveal that an average capacitor approximates the nonlinear capacitor reasonable well.

An additional phenomenon that causes fluxuations in drain current is channel charge. When the gate is on, some current is flowing through the channel or equivalently some net charge is present in the channel. When the gate turns off, that charge is released out the drain and source. Though this charge changes the drain current only at the input pulse edges, it is enough to perturb the waveforms.

3.1.3 Linear Class E Matching Network

The last section to model is the linear class E matching network. This model takes an input current into the matching network and generates the output voltage waveform, V_{OUT}. From Kirchoff's current law, the current into the linear network is just the difference between the current through the RFC and the switch. This current can be multiplied by the impedance of the network to get the switch voltage. Similarly, the output voltage can be attained from the switch voltage since it's just a simple voltage division. The transfer functions for each of these calculations are given by Equation 3.4 and Equation 3.5. Combining these, the output voltage can be acquired. Though these equations are in the Laplace domain, they can be implemented in discrete-time using bilinear transforms.

$$\frac{V_{switch}}{I_{network}}(s) = \frac{L_2C_2s^2 + C_2Rs + 1}{L_2C_1C_2s^3 + C_1C_2Rs^2 + (C_1 + C_2)s} \tag{3.4}$$

$$\frac{V_{out}}{V_{switch}}(s) = \frac{C_2Rs}{L_2C_2s^2 + C_2Rs + 1} \tag{3.5}$$

Using similar transfer functions, the voltages and currents across every component can

be calculated as in HSPICE. However, to keep the simulation times fast, the only other output generated will be the switch voltage since it is necessary for the model to work properly. The switch voltage is necessary to set the drain voltage in the NMOS model and the voltage across the inductor in the RFC model.

3.2 Creating the Circuit in CppSim

To verify this three part model, the equations above have to turned into usable modules in CppSim. Though currently not available on the web, the CppSim package provides a BSIM3v3 DC transistor module that takes the gate, drain, source, and bulk voltages as inputs to produce the output drain current at any given temperature. This module reads in an HSPICE model parameter file to produce the proper IV characteristic. One way to implement the transistor described in the previous section is to encapsulate the DC transistor characteristic with code that implements the effect of the parasitics. By observing that the current into the matching network generates the switch and output voltage, the DC drain current can be fed into a block that adds in the effect of the parasitic capacitors. Since the RFC and class E matching network are also governed by equations, one unified block, called *E_Network*, can be used to compute the effects of the parasitic capacitors, RFC, and matching network. It will have two inputs, the DC drain current and the variable duty cycle input pulse, and two outputs, the switch and output voltages. The block diagram is shown in Figure 3-3. Additional outputs for the effective drain current and RFC current are added to get a more complete picture of the power amplifier. The module is implemented as the following code.

---

module: E_Network
parameters: **double** c1, **double** c2, **double** l1, **double** l2, **double** r
inputs: **double** ids, **double** vin
outputs: **double** vswitch, **double** vout, **double** idseff, **double** isup
classes:

```
  Filter vswitchinet("l2*c2*s^2+c2*r*s+1","l2*c1*c2*s^3+c1*c2*r*s^2+
                      (c1+c2)*s","Ts,c1,c2,l2,r",Ts,c1,c2,l2,r);
  Filter voutvswitch("c2*r*s","l2*c2*s^2+c2*r*s+1","Ts,c2,l1,l2,r",
```

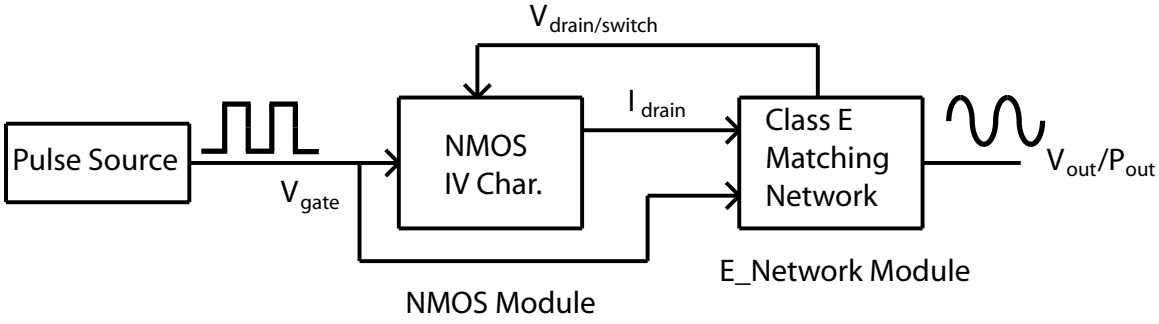

Figure 3-3 The CppSim block diagram for the class E power amplifier.

```
                    Ts,1.02*c2,l1,l2,r);
  Filter i_l1("1/l1","s","l1,Ts",l1,Ts);
  Filter igd("C*s","1","Ts,C",Ts,1.4632e-12);
  Filter igs("C*s","1","Ts,C",Ts,1.4632e-12);
code:
  igd.inp(vin-vswitch);
  igs.inp(vin);
  idseff = ids-igd.out-igs.out; //idseff = ids; in ideal case
  i_l1.inp(0.6-vswitch);
  isup = i_l1.out;
  vswitchinet.inp(isup-idseff);
  vswitch = vswitchinet.out;
  voutvswitch.inp(vswitch);
  vout = voutvswitch.out;
```

The current contributed by the Gate-Drain and Gate-Source overlap capacitance, i_{gd} and i_{gs} respectively, is realized using differentiators described by Equation 3.2 and Equation 3.3. The value of C_{ov} can be determined by looking at the operating point in HSPICE. C_{ov} turns out to be 1.46 pF for 400 parallel $10\mu m/0.18\mu m$ NMOS transistors in the $0.18\mu m$ TSMC process. Since the drain capacitance is in parallel with C_1, it is implemented by lumping its value with C_1. Through curve matching over various duty cycles, the equivalent junction capacitance turns out to be about 3pF. The RFC current is implemented with an integrator as described by Equation 3.1. The class E filter is implemented by cascading two filters as described by Equation 3.4 and Equation (3.5). One filter transforms the current into the linear network to the switch voltage. The second filter transforms the in-

put voltage waveform to the output voltage waveform. The actual current going into the network is the difference between the current flowing through the inductor and the effective drain current. The effective drain current is the difference between the ideal transistor current and the current drawn by the parasitics.

3.3 Simulation Results

In this section, the CppSim behavioral model described in Section 3.2 will be compared to the HSPICE simulations. The HSPICE simulations will take into account all capacitive effects, including channel charge, overlap capacitance, and the nonlinear depletion capacitances. The behavioral model only takes into account the overlap capacitance and uses an average capacitor for the nonlinear Drain capacitance. The main difference between the two models is that the channel charge is not simulated and the nonlinear depletion capacitance is averaged in the CppSim behavioral model. The key is to show the behavior model still produces results similar to an HSPICE simulation but simulates faster.. These simulations were run at room temperature.

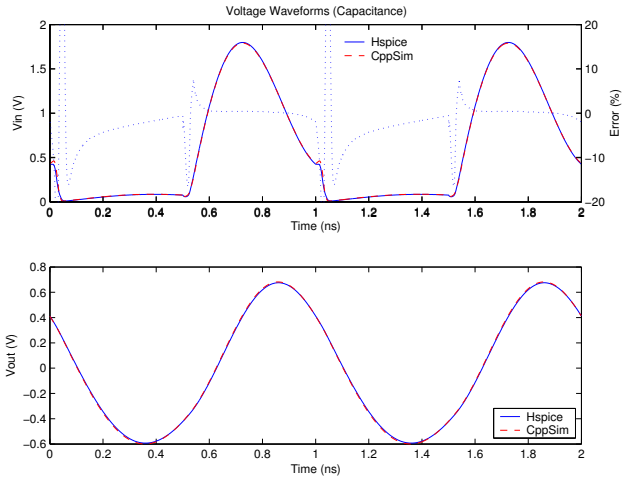

Figure 3-4 Switch and RF output voltage waveform for 50% duty cycle.

Figure 3-4 shows the CppSim and HSPICE simulations running at a 50% duty cycle. The CppSim switch voltage waveform is very close to the HSPICE simulation. The CppSim and HSPICE waveforms match very well, except at the input transition edges where

channel charge is a factor. The voltage deviation is about 50 mV at the input rising edge and 10 mV at the falling edge. However, the relative error is still less than 1% when the voltage is large. The output waveforms are essentially identical.

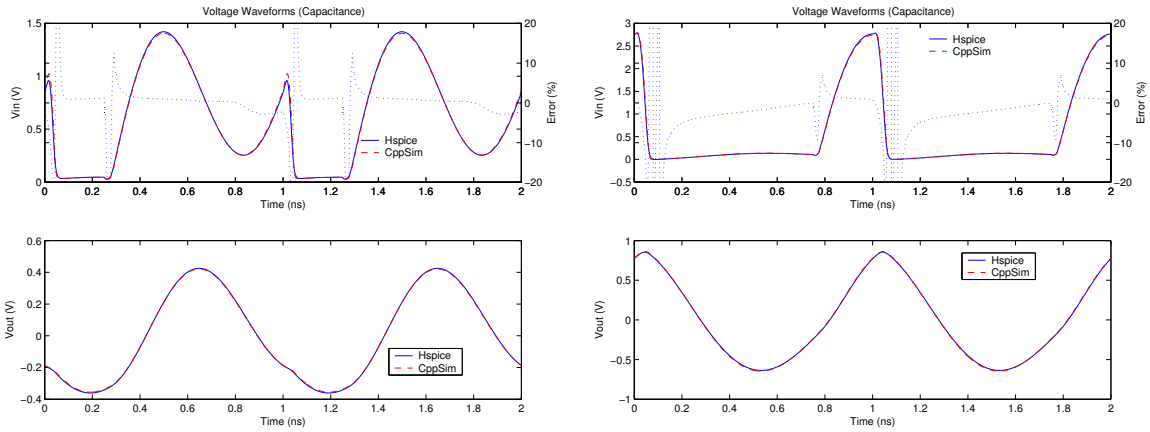

Figure 3-5 Switch and RF output voltage waveform for 25% (a) and 75% (b) duty cycle.

To verify that the voltage waveforms are accurate at other duty cycles, plots of 25% and 75% duty cycle are shown in Figure 3-5. As with the 50% duty cycle case, the switch voltage waveforms have small error except around the transition edges. In the 75% duty cycle plot, the error in the switch voltage is within 2% when the switch is open. In the 25% duty cycle case, the switch voltage is also within 2% except the error is 5% during the second switch voltage rise whe the switch is open. This is due to the change in the depletion capacitance with the switch voltage. Even with these larger switch voltage errors, the output voltage waveforms are nearly on top of each other.

Ultimately, the output power and efficiency are the figures of merit. If the power and efficiency curves do not match well, this model is not useful. Looking at the output power plot shown in Figure 3-6, the output power does match well. The error is within 2% at high output powers and increases to 5% at low output powers. The efficiency curve is always within 3% error. The increasing error at smaller duty cycles is due to channel charge. To first order, the bias current is set by the switch pulling on the RFC when the switch is on. For large duty cycles, the charge absorbed by the channel at the rising edge is small compared to the total charge pulled by the transistor. As the duty cycle decreases, the charge absorbed

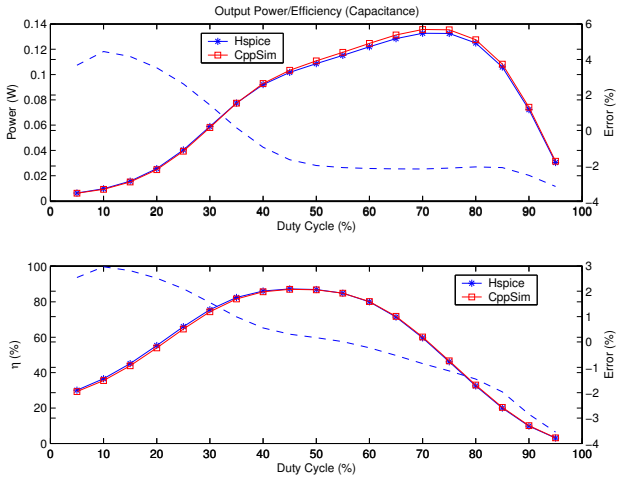

Figure 3-6 Output power and efficiency for nonideal transistor case.

by the channel becomes more significant compared to the total pulled charge.

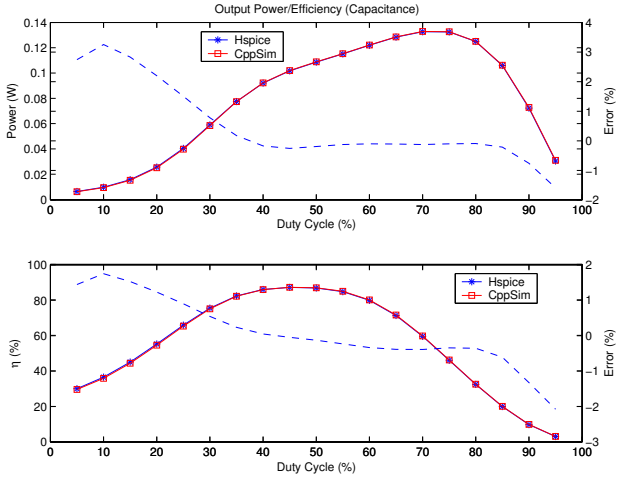

Figure 3-7 Output power and efficiency after compensating class E network.

The error in the power and efficiency plots can be further reduced by tuning the class E network as discussed in Section 2.4. With a 0.3% increase in the size of L_2 and C_2, the error in the power is about 0.25% for duty cycles greater than 35%. For smaller duty cycles, the output power error due to channel charge still increases, but only goes up to 3%. The efficiency error stays within 2% at all duty cycles.

The worst case output power error is 3%. The worst case efficiency error is at most 2%. These power and efficiency errors are small enough that the simulation speed improvement CppSim has over HSPICE makes it the simulation vehicle of choice for this project. The

power amplifiers were simulated for 300 ns (three hundred 1 GHz periods) at a time step of 1 ps. In CppSim, this was done by setting the time step, Ts, in the simulator to 1 ps. In HSPICE, this was done by setting delmax to 1 ps. The CppSim behavioral model ran in 105 seconds. The HSPICE simulation ran in 8 minutes and 25 seconds. Even in a system that has as few nodes as the class E power amplifer (6 total including the input, power, and ground), the CppSim simulation ran five times faster than the HSPICE simulation. If a more complicated system with many more nodes is simulated as will be in the future, the improvement will be even more significant.

3.4 Modeling Summary

The CppSim behavioral model can model the HSPICE circuit output power to within 3% and the efficiency within 2%. The difference in the simulation results is mainly due to the CppSim model not including the effects of channel charge and using an average capacitor to model depletion capacitance. The main benefit of switching to a behavioral model is the simulation speed improvement. For a 3% error in the behavioral model compared to HSPICE simulations, the simulation time is five times faster. Though the speed improvement seems trivial, a more complicated system with many more nodes will have a much larger speed improvement. In the next chapter, one such complicated system that will benefit from the speed improvement of the behavioral model is the power amplifier with feedback.

Chapter 4

Linearizing a Class E Power Amplifier

A pulse width modulated (PWM) class E power amplifier inherently does not have good linearity from input amplitude to output amplitude. This can be seen in a high level way. By varying the duty cycle as a function of input amplitude, the fundamental component of the square wave is changed in a nonlinear fashion. The fundamental component of the PWM square wave modulates the current into the class E network that generates the output waveform.

In this chapter, two different techniques of linearizing the relationship betweeen duty cycle and output voltage will be proposed. The first method uses precompensation which applies prior knowledge of the power amplifier characteristics to linearize the duty cycle to output voltage characteristic. The second method is to use amplitude feedback. Through simulations of the behavioral model in CppSim, feedback will be shown to be the preferred method of linearizing this system.

4.1 Linearity and Dynamic Range

Power amplifier linearity is typically defined from its input voltage amplitude to output voltage amplitude. For classical power amplifiers that take sinusoidal inputs and generate sinusoidal outputs, the power amplifier is considered linear in the range of input amplitudes that give you a constant gain. For a system that does not have a sinusoidal input, linearity is still defined in a fashion that is consistent with the above definition. Since the input to this

system is a baseband amplitude, the power amplifier is considered linear if the RF output amplitude is proportional to the baseband amplitude. These definitions are diagrammed in Figure 4-1.

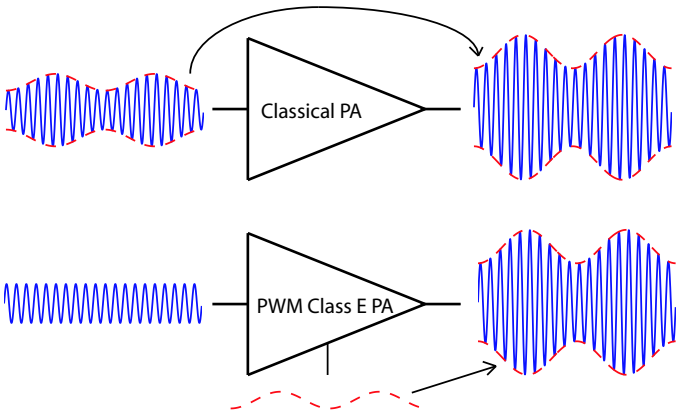

Figure 4-1 Linearity definitions for a classical PA and the proposed PWM class E PA.

There is distortion in any amplifier, but if the input is small enough, the distortion in small enough to be negligible. In power amplifiers, distortion exists as well. However, depending on the specifications on the modulation scheme, there is some tolerance to non-linearity. If the nonlinearity stays within this tolerance, the system can still be considered linear. In a single channel system, a typical number for spectral distortion tolerance is -30 dBc[2]. An alternative way to stating this specification is if the output amplitude is proportional to the input amplitude within 3% error, the system is considered linear.

The term that is more representative of the power amplifier's linearity is called dynamic range. The dynamic range is the continuous range of input amplitudes that generate a linear RF output amplitude within the spectral distortion tolerance. In typical class A power amplifiers, the dynamic range is very high (60+ dB) since the input can be backed off far away from the 1 dB compression point where distortion becomes significant[2]. However, for a pulse width modulated class E power amplifier, dynamic range will not be as high due to the nature of pulse width modulation. In the following sections where the power amplifier is linearized, the dynamic range of the systems will be measured using the -30 dBc spectral distortion tolerance metric.

4.2 Uncompensated Power Amplifier

The pulse width modulated class E power amplifier architecture is shown in Figure 2-4. The linear range in a this architecture is measured from the delay input in the variable delay to the output amplitude. Since the input will set the duty cycle, the uncompensated power amplifier's linearity is measured from the input duty cycle to the output amplitude. Since varying the duty cycle of the input pulse varies the fundamental component of the input pulse in a nonlinear fashion, the drain current and output voltage will be modulated in a nonlinear fashion. By using duty cycle as a way of generating different output powers, the linearity of the uncompensated power amplifier is poor. Using the -30 dBc linearity bound, the power amplifier dynamic range is 9.1 dB. The green region in Figure 4-2 is the output range that the power amplifier is linear. This range corresponds to duty cycles between 14% and 40%. Their corresponding minimum and maximum output powers are 10.8 dBm to 19.9 dBm. Though the system inherently has some dynamic range, this system is inefficient since it doesn't utilize the zero voltage switching condition for 50% duty cycle pulses. By utilizing the output around the zero voltage switching condition, a more efficient linear power amplifier can be built. This will be accomplished using precompensation and feedback.

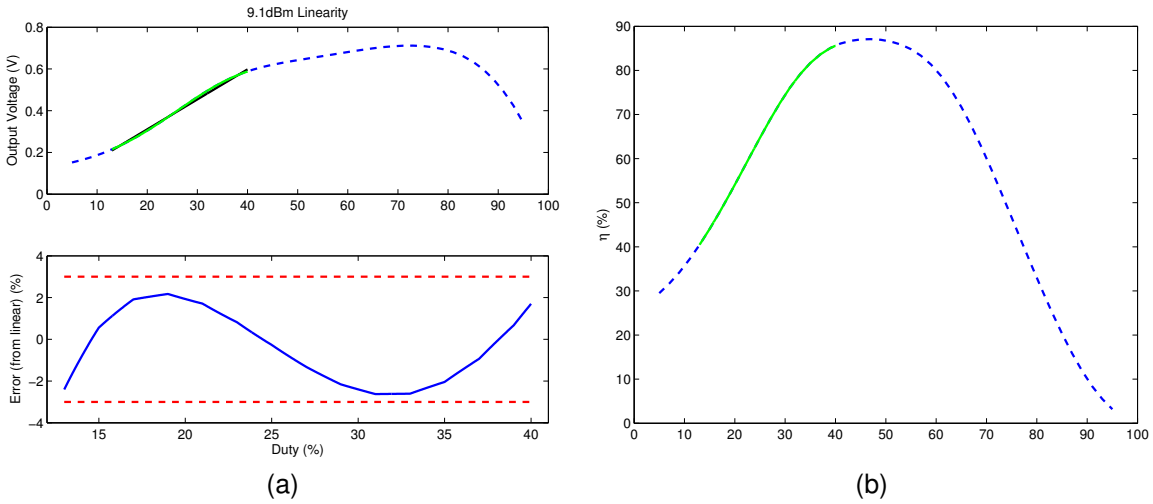

Figure 4-2 Inherent linearity (a) for a PWM power amplifier and its associated efficiency (b).

4.3 Precompensation

One method of linearization is by precompensation. For a given power amplifier design, the output voltage can be calculated for all input duty cycles a priori. The duty cycle to output voltage relationship can then be characterized in some functional form. Also, the inverse relationship can be found. Suppose an inverse block were added before the variable delay block as shown in Figure 4-3. Now, the input to the system is no longer a duty cycle but an amplitude. Also, if this inverse function were perfect the output should follow the input exactly.

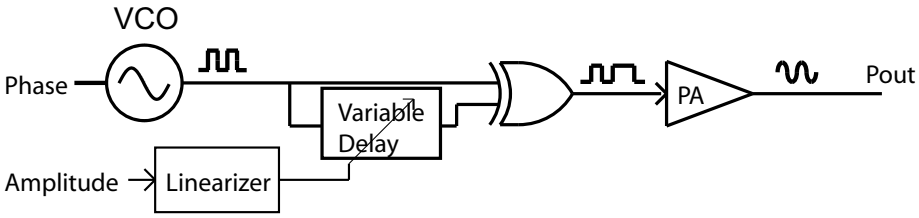

Figure 4-3 System diagram for a precompensated PWM power amplifier.

This inverse function can be found by simulating the uncompensated system across all duty cycles and recording the periodic steady state output voltage as shown in Figure 4-4. At large duty cycles, the output power drops off sharply and makes the function not one-to-one. At the extreme when the switch is always on, the output power is zero. Thus, for a given output power, there are two duty cycles that will produce it. Since the system is more efficient at the smaller duty cycles, the large duty cycles can be thrown out to make this relation one-to-one. A unique inverse function can be found from this one-to-one relationship.

A polynomial fit can be used to match the inverse relationship. Figure 4-5 shows that there seems to be two behaviors in the inverse relationship. For output voltages less than 0.14V, the output voltage increases quickly with changes in the duty cycle. For larger output voltages, the voltage increases slower with respect to duty cycle. The split behavior is due to the rise and fall times of the pulse width modulated square waves. At small duty cycles, the pulses form runt pulses that do not have enough time to reach the supply voltage before the voltage starts falling. In the $0.18\mu m$ process, typical rise and fall times are 40ps

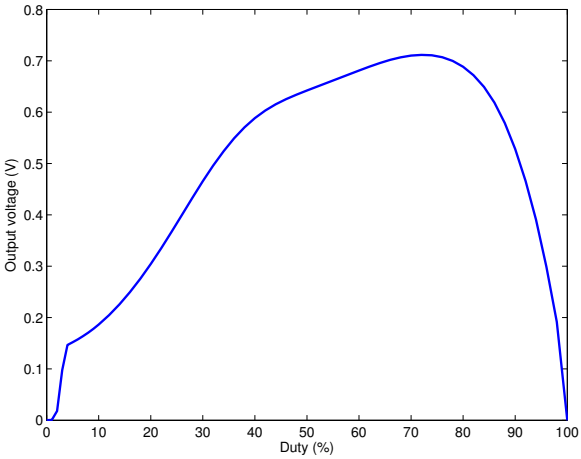

Figure 4-4 Duty cycle to output voltage relation of a PWM class E power amplifier architecture.

or 4% of the 1 GHz period. Thus, any duty cycles smaller than 4% will form runt pulses.

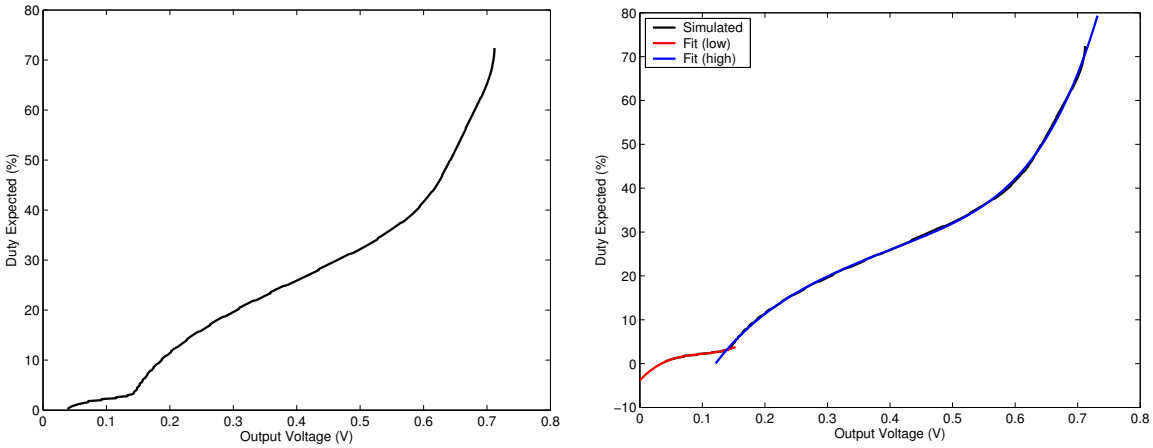

Figure 4-5 The duty cycle to output voltage inverse relationship (a) and its fit (b).

Since there are two different behaviors at small and large output amplitudes, the natural choice is to use a linearizer that has two outputs and choose between the two. Each output can be created by polynomial fitting a portion of the curve. For small output amplitudes, a 3rd order polynomial fit is used to get a the fit shown in red on Figure 4-5(b). Shown in blue is the 5th order fit for large output amplitudes. If a single fit was used for all output amplitudes, a 10th order fit would not be as good since the discontinuity at the small and large amplitude behavior boundary makes a high order fit necessary. Therefore, much more circuitry is needed to create a high order fit compared to creating a comparator to switch

between the two outputs.

When this system is behaviorally simulated with the linearizing block, the output is as expected. The steady state input amplitude to output amplitude plot is shown in Figure 4-6(a). The output follows the input for most inputs. When the input is below 0.035V, the linearization block starts to fail. The most important part of this characteristic is that the system is linear across the most efficient (and high power) portion of the power amplifier operating range. This linearization technique has now improved the dynamic range of the power amplifier to 14 dB across all temperatures. The power output range is now 7.2 dBm to 21.2 dBm. This is the range of the large duty cycles. To get any more dynamic range below that becomes increasingly difficult since that's in the runt pulse region where the gain is very high. Any error in precompensating the duty cycle will result in a large error in the output voltage. This is the cause of the vastly different errors at various temperatures. From the graph, potentially 20 dB of dynamic range is possible with a low order fit for runt pulses.

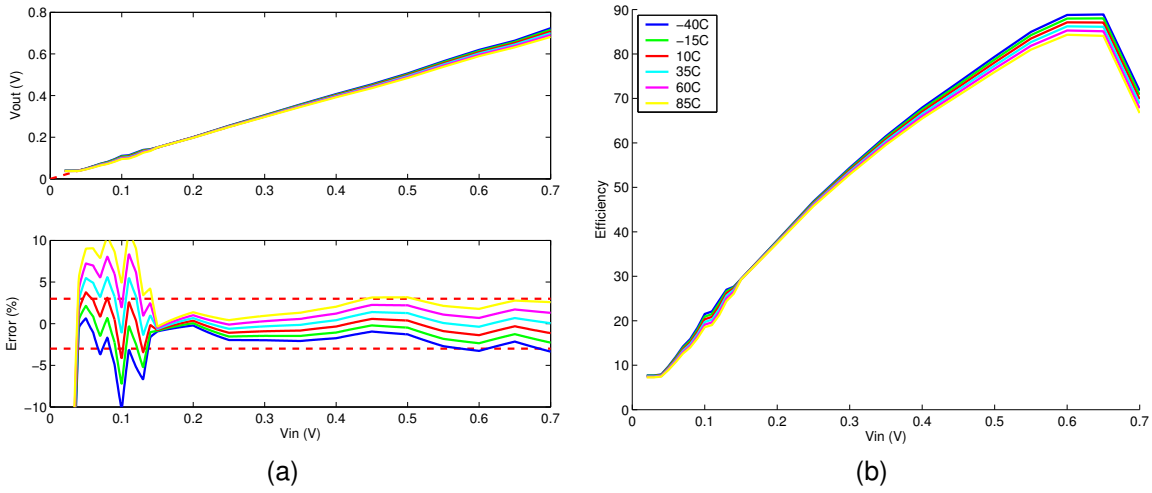

Figure 4-6 The precompensated system's linearity (a) and efficiency (b) across temperatures.

One of the concerns with a design like this is passive component variability. In chapter 2, it was shown that a 20% variation in a passive component will result in a drastic change in the output characteristic. If all the components varied within 10%, most likely the output characteristic would not perform as designed. Therefore, to use precompensation, the linearizing block must be programmable to adjust for changing output voltage characteris-

tics. In industry, an approach like this would not be practical. A product where every part must be tuned to work properly could not be mass produced. Also, creating a multiplier whose polynomial coefficients must be accurate to many decimal places would be difficult to design.

4.4 Feedback

An alternative way of linearizing the system is to add feedback. Feedback can be used to force the power amplifier output amplitude to follow the input amplitude more accurately at the expense of adding some transient response. This feedback system can be constructed as follows. Since the difference between the input amplitude and output amplitude must be zero in steady state, an integrator must be added to the input of the linearizer block to level shift the amplitude to the necessary input. A gain block is added before the integrator to speed up or slow down the integration. A peak detector is used to convert the RF amplitude information to baseband before it can be subtracted from the input baseband amplitude. The complete system is shown in Figure 4-7. Though this system seems like it would work, the only way to truly determine this is to check its stability by looking at its poles and zeros. In this system, the stability can be best seen from the root locus.

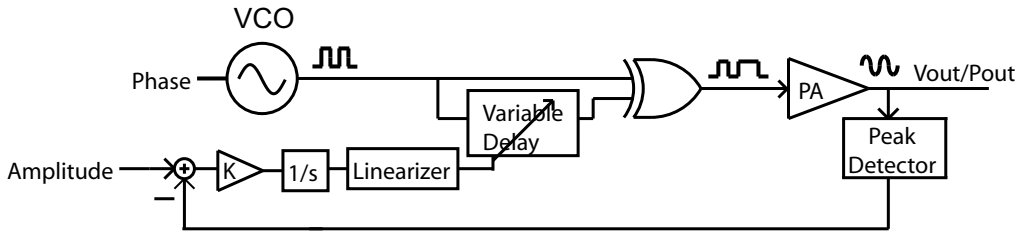

Figure 4-7 System diagram for a feedback system.

4.4.1 Root Locus Basics

Root locus is one of many methods to determine the closed loop poles and zeros using the open loop characteristics. What makes this method particularly powerful is that it resolves the tradeoff between high loop gain (faster system response) and stability. The location of

the poles and zeros will determine the system response. For this amplitude feedback loop, the root locus technique can be used to determine the gain K in the forward path to generate the best system response.

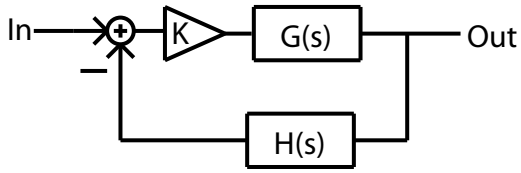

Figure 4-8 Block diagram of a general feedback system.

In a general feedback system, there is some frequency response, $K * G(s)$, in the forward path and some frequency response, $H(s)$, in the feedback path. The K in the forward path is called the *root locus gain*. The general feedback block diagram can be seen in Figure 4-8. The closed loop response of such a system is given by Equation 4.1. The closed loop poles can be found by solving for the roots of $1 + KG(s)H(s) = 0$. A root locus plot shows how the poles move when K is changed. The poles are plotted on a real and imaginary frequency axes. When K is close to zero, they start at the open loop poles. As the gain increases, the poles move toward the open loop zeros or towards infinity.

$$\frac{Out(s)}{In(s)} = \frac{KG(s)}{1 + KG(s)H(s)} \tag{4.1}$$

4.4.2 Frequency Response

In order to apply the root locus to our system, the frequency response of the system must be determined. The frequency response of the system can be solved by changing signal domains and lumping blocks together. In the forward path, the three blocks are the gain block, the integrator, and the linear power amplifier block. The power amplifier block is a lumping of the power amplifier and the circuitry that generates the pulse width modulated signals. These include the linearizer, variable delay, voltage controlled oscillator, and XOR gate. In the feedback path, there is only an peak detector. The system block diagram is shown in Figure 4-9.

The input to the feedback loop and the feedback signal are in the baseband domain.

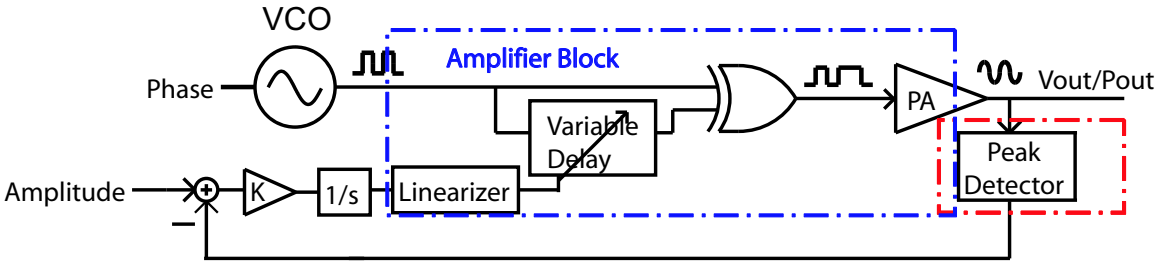

Figure 4-9 Block diagram of power amplifier system.

The difference is fed into a gain and integrator block whose output will be an amplitude in the baseband domain. The power amplifier block takes this input and creates an output amplitude signal in the RF domain. In the feedback path, the peak detector will take this amplitude in the RF domain and convert it down to an amplitude in the baseband domain.

Now that the signal domains have been determined, only the frequency response of the power amplifier block and peak detector needs to be calculated. With the linearizer, the power amplifier block can be thought of as a unity gain block with some undetermined poles and zeros. These poles and zeros can be determined following the signal path. The linearizer is a high bandwidth variable gain block where the poles and zeros are assumed to be at high enough frequencies that they do not play a role in the frequency response. The output of the linearizer drives the variable delay which generates a pulse width modulated square wave. By viewing the pulse width modulated square wave in the duty cycle domain, the variable delay and XOR gate can be thought of as a gain term with high frequency poles and zeros. As with the linearizer, these poles and zeros can be ignored. This means that all of the poles and zeros in the power amplifier block come from the class E power amplifier. The pulse width modulated square wave (duty in the duty cycle domain) modulates the current into the matching network at the switching frequency. Ignoring high frequency transistor parasitics, this is just a nonlinear gain block. This means that all the poles and zeros come from the matching network. From Section 3.1, there are two transfer functions that can transform the network current to the switch voltage and the switch voltage to the RF output voltage. Combining these two equations into Equation 4.2, the poles and zeros from these transfer functions are the dynamics of the power amplifier block.

$$\frac{V_{out}}{I_{network}}(s) = \frac{C_2 R}{L_2 C_1 C_2 s^2 + C_1 C_2 R s + C_1 + C_2} \tag{4.2}$$

The peak detector is just a low frequency pole that comes from the RC settling time of the output of the peak detector. This pole will be high enough frequency that the system dynamics will not be dominated by this pole and slow enough that there will not be large ripple at the output.

Plugging in the frequency response of all the blocks, the closed loop system is shown in Figure 4-10. By taking a look at the root locus, there are four poles and no zeros in the system. In the open loop case, there's a pair of complex conjugate poles at high frequencies and two low frequency poles at zero from the integrator and at a low frequency from the peak detector. When the loop is closed and the gain is increased, the high frequency complex conjugate pairs move towards infinity asymptotically at a plus or minus 135 degree angle. For low gains, the low frequency poles move toward each other on the real axis. They form a double pole before splitting as a complex conjugate pair asymptotically at plus or minus 45 degrees. At high enough gains, the poles move into the right half plane and make the system unstable. The pole movement is shown in Figure 4-11.

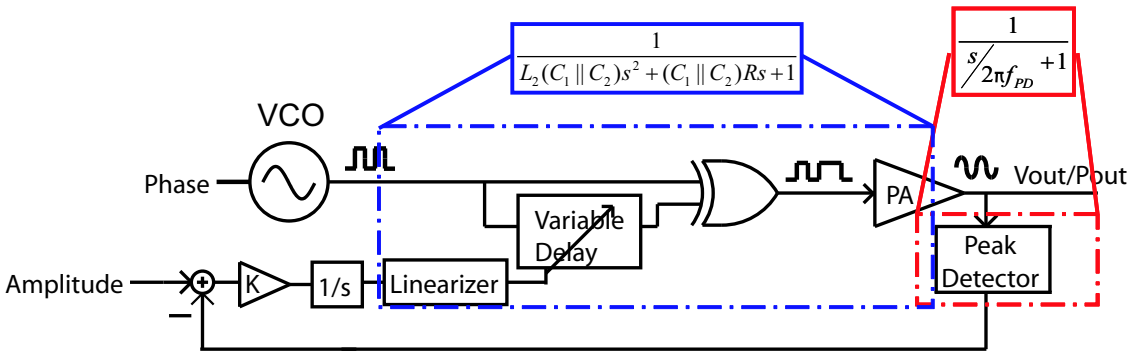

Figure 4-10 System Diagram broken down into a linear feedback system.

In this system, the integrator and peak detector poles are the dominant poles in the system. When the gain is low, the integrator pole dominates the slow system response. For the fastest system response, K has to be such that the integrator and peak detector poles form a double pole. For even larger K values, the response settles slower and has overshoot. From the root locus, the ideal gain K should $7.86e6$.

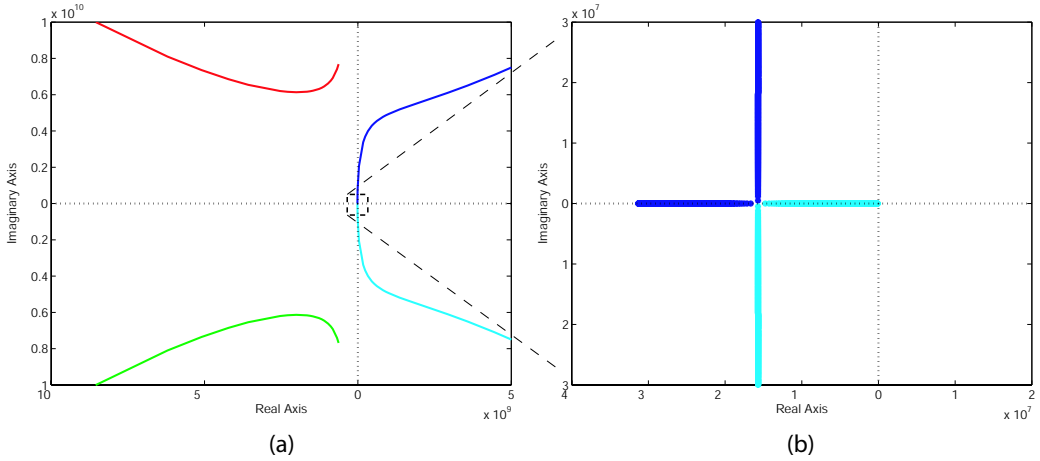

Figure 4-11 The root locus of the system (a) and zoomed in view at the dominant poles (b).

When this system is simulated at various baseband amplitudes with a gain of 7.86e6, the system becomes less temperature sensitive as shown in Figure 4-12. However, one drawback is that the error now seems to be input amplitude dependent. This error results from the fact that the peak detector measures the peak of the output instead of the amplitude of the fundamental frequency. This is a problem that will be fixed in the future with a mixer and a low pass filter. In that way, only the fundamental frequency amplitude will be measured. Even if this mixer were used, the architecture is still limited by the accuracy of the precompensation. The dynamic range of this system is about 20 dB. The output power range is 1.2 dBm to 21.2 dBm.

Since the precompensation block is currently limiting this architecture, the dynamic range of this architecture could potentially improve by removing the precompensation from the amplifier block. The tradeoff is that the gain of the amplifier block is no longer linear. Depending on the gain of the amplifier block, the dominant poles will move. If the gain is too high, the system will oscillate. If the gain is too low, the settling time will be very long. The gain of the amplifier block can be seen by looking from the output of the integrator to the output RF fundamental amplitude. The gain plot over various integrator outputs is shown in Figure 4-13.

In the precompensated case, the integrator output voltage corresponds to the baseband input voltage. Naturally, the gain of the amplifier block is unity when the precompensation

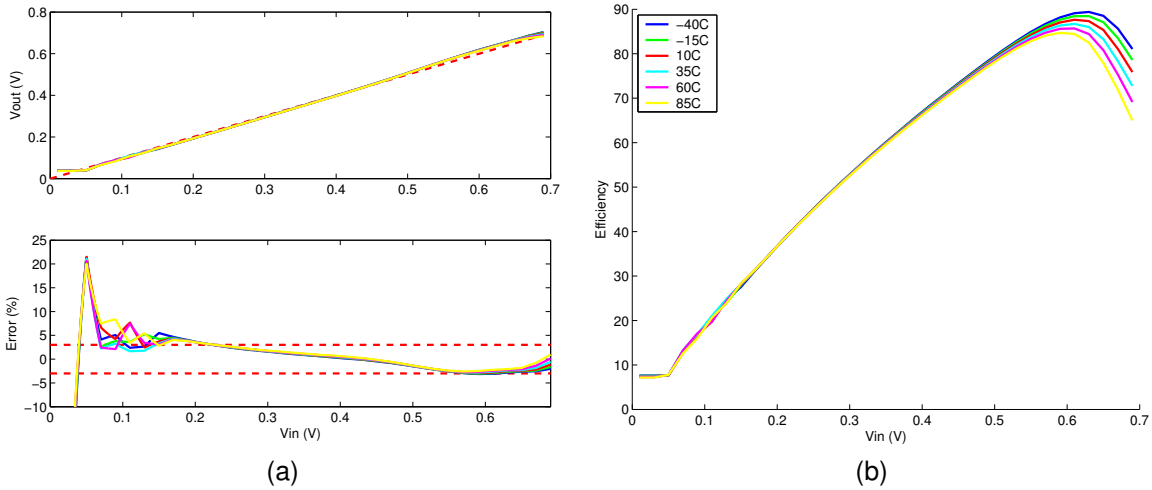

Figure 4-12 Linearity (a) and efficiency (b) plot for feedback around a precompensated system.

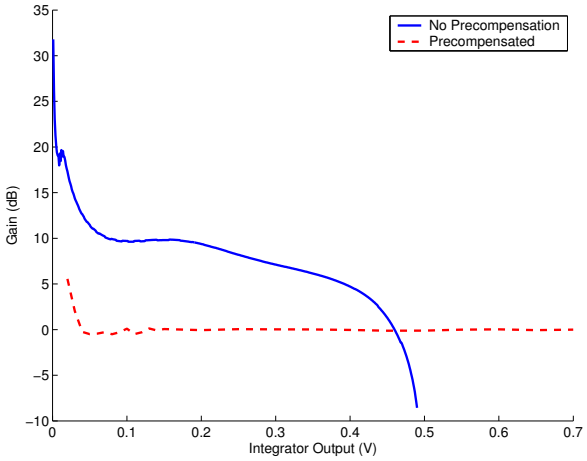

Figure 4-13 The gain of the power amplifier block over various integrator outputs.

block is included. When there is no precompensation, the integrator output is driving the variable delay block. The voltage corresponds to the phase shift. Since the power amplifier is operated with duty cycles under 75% to prevent inefficiencies, the delay voltage should never be over 0.375V. From Figure 4-13, the gain of the amplifier block varies over 20 dB for a dynamic range that is greater than the precompensated feedback system. If the poles do not move over a gain (K) range of 20 dB, the compensation block is not needed.

With a gain of K=$7.86e6$, the pole will move between a double pole at $-16e6$ to a conjugate pair at $-16e6 \pm 47e6$ with changes in the baseband input amplitude. The increase in the imaginary part results in an underdamped system that will overshoot up to 35%

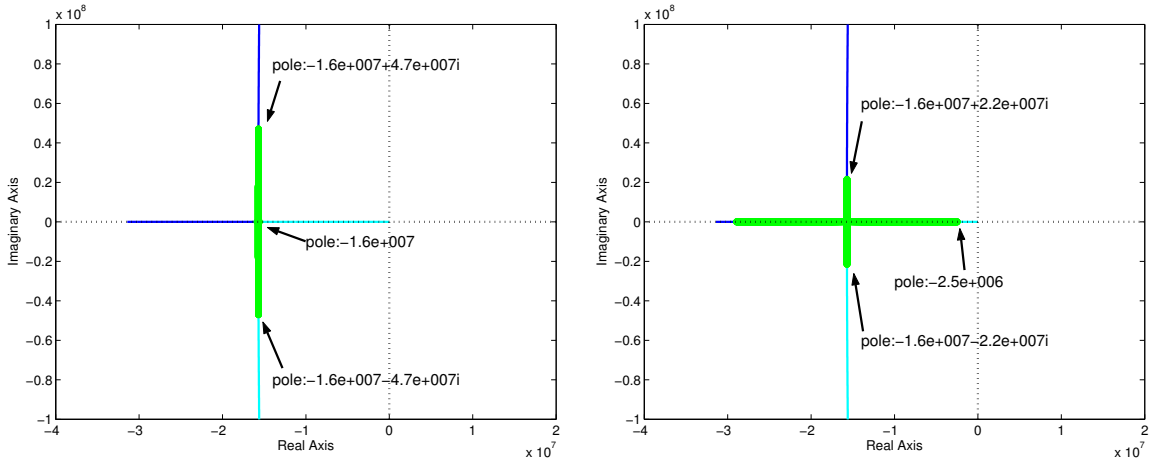

Figure 4-14 Pole movement within a gain of 20 dB with K=$7.86e6$ (a) and K=$2.27e6$ (b).

before settling at the steady state value. The high overshoot is a tremendous waste of power so a lower gain of K=$2.27e6$ is chosen to reduce the overshoot to less than 10%. In this case, the pole moves between a dominant single pole at $-2.5e6$ and a pair of conjugate poles at $-16e6 \pm 22e6$. The trade off with overshoot is a slow system response. The settling time has now increased over 6 times! Depending on the specifications of the system, efficiency (overshoot) can be traded with settling time.

When the system is simulated, it turns out that the overshoot causes another problem. When the system overshoots too much, the integrator output has the potential of going negative. If it goes negative, the variable delay creates bigger and bigger pulses as the integrator output gets more negative. This is essentially adding an inverter in the system. Since this behavior is not desirable, low overshoot is necessary to keep the variable delay between zero and half a period.

Using a gain of K=7.86e6, Figure 4-15 shows the resulting system simulations at various input levels. As with the precompensated feedback case, the output does not vary much with temperature. Also, the linearity error is dependent on the peak detector in a similar fashion as before. The dynamic range has improved to 23 dB compared to 20 dB in the best case precompensated feedback case. The output power range is now -1.7 dBm to 21.2 dBm.

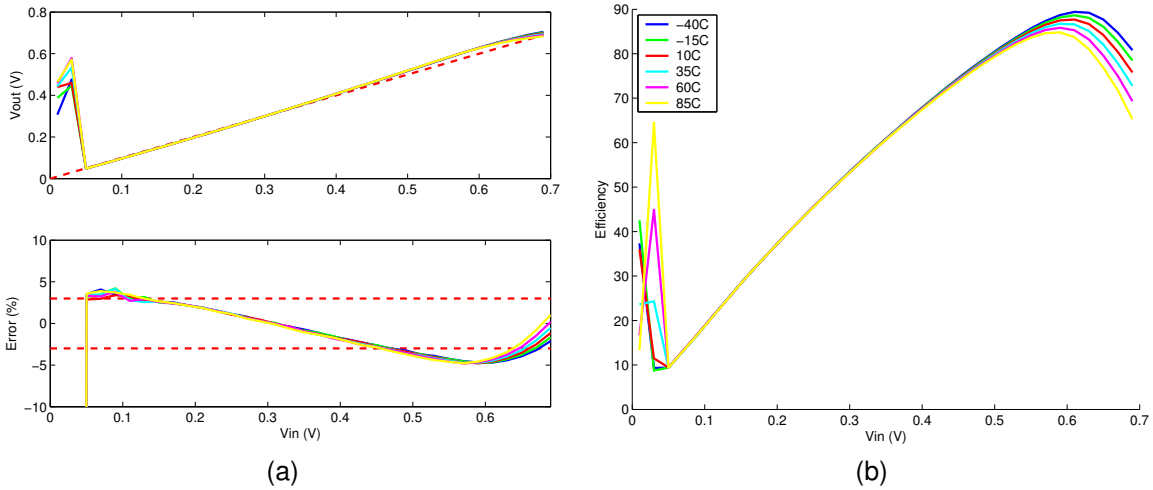

Figure 4-15 Linearity (a) and efficiency (b) plot for an amplitude feedback system.

4.5 Summary

This chapter presents two ways of linearizing a power amplifier characteristic. The first method is using a precompensation block to invert the nonlinear gain in the power amplifier. Though this does work well for large duty cycles, the accuracy necessary for small duty cycles is difficult to achieve. The second method is using feedback. Feedback cancels out temperature dependences and linearizes the output over a larger range than precompensation. The limiting factor with feedback is that at small duty cycles the nonlinear gain of the power amplifier becomes large enough to cause the feedback loop to become unstable.

Chapter 5

Conclusions

One way of creating a high efficiency power amplifier is by using the class E design. The resonant network of the class E amplifier creates the highly efficient zero voltage switching conditions. However, using just the class E power amplifier results in constant output power. This would limit the power amplifier to transmitting constant envelope modulation schemes such as Quadrature Phase Shift Keying (QPSK) or Gaussian Minimum Shift Keying (GMSK). Since many of today's modulation schemes such as Quadrature Amplitude Modulation (QAM) or Enhanced Data rate through GSM Evolution (EDGE) are not constant envelope, dynamic range is necessary. Dynamic range can be created using pulse width modulation. The varying duty cycle changes the current into the matching network to create different output powers. The issue with pulse width modulation is that it is a nonlinear process. Since power amplifiers require linear dynamic ranges, linearization techniques need to be applied.

This thesis looks at two methods of achieving linearity– precompensation and feedback. Precompensation uses the output characteristic to compensate at the input side. This strategy works well to get about 14 dB of dynamic range. However, this technique does not work well for mass production since any variation in matching network component values will still result in a nonlinear output characteristic. The alternative linearization technique is feedback. In addition to improving the dynamic range to 23 dB, feedback makes the power amplifier less sensitive to temperature variations. The limitation of feedback is that the high gain at small duty cycles can make the system unstable.

Currently, industry is interested in developing an integrated CMOS power amplifier that has high efficiency. One current approach is using a class E power amplifier and modulating the power supply. Theoretically, this approach has high efficiency at all power levels, but in practice this is not the case. In this thesis, the new architecture introduced is the pulse width modulated class E power amplifier. Though efficiency does take a hit at low power outputs, the output power can modulate faster than modulating the power supply. Faster amplitude modulation can be used to build higher bandwidth and data rate systems. Also, the class E matching network can be tuned for better performance based on the modulation scheme. If the transmitted symbol amplitudes tend to be large, the matching network can be tuned for higher efficiency at large duty cycles. If most of the transmitted symbol amplitudes are small, the matching network can be tuned for higher efficiency at small duty cycles.

5.1 Future Research

The MOSFET model in this thesis is not exact. Though it does a good job, it can be made more exact by doing a charge model. Two modeling issues would be solved by changing to this model. The first is that the effects of channel charge can be modeled. When the switch turns on and off, charge is injected and removed from the channel. The second is that depletion capacitance can be modeled exactly. The depletion capacitance changes as a function of voltage. Instead of including an average capacitor, the depletion capacitance can be modeled exactly as a function of drain voltage. These improvements were not pursued since they can improved the accuracy of the model by at most 5%.

The system can be improved by designing the feedback using a mixer and a lower pass filter. Ideally, the mixer and low pass filter would work perfectly. In practice, the input would be mixed with a square wave which would feedback some higher order products. However, the odd harmonic products are essentially squared values of much smaller numbers. This should make these products minimal.

Bibliography

[1] I. Aoki, S. Kee, D. Rutledge, and A. Hajimiri. Fully integrated cmos power amplifier design using the distributed active-transformer architecture. *Solid-State Circuits, IEEE Journal of*, 37:371 – 383, March 2002.

[2] S. C. Cripps. *RF Power Amplifiers for Wireless Communications*. Artech House, Boston, 1999.

[3] P. Heydari and Y. Zhang. A novel high frequency, high-efficiency, differential class-e power amplifier in 0.18um cmos. *Low Power Electronics and Design, 2003. ISLPED '03.*, pages 455 – 458, August 2003.

[4] T. T. Hung and M. N. El-Gamal. Class-e cmos power amplifiers for rf applications. *Circuits and Systems, 2003. ISCAS '03*, 1:I–449 – I–452, May 2003.

[5] M. Kazimierczuk and K. Puczko. Exact analysis of class e tuned power amplifier at any q and switch duty cycle. *Circuits and Systems, IEEE Transactions on*, 34:149 – 159, February 1987.

[6] T. H. Lee. *The Design of CMOS Radio Frequency Integrated Circuits*. Cambridge University Press, Cambridge, 1998.

[7] K. L. R. Mertens and M. S. J. Steyaert. A 700-mhz 1-w fully differential cmos class-e power amplifier. *Solid-State Circuits, IEEE Journal of*, 37:137 – 141, February 2002.

[8] N. Sokal. Class e high-efficiency power amplifiers, from hf to microwave. *Microwave Symposium Digest*, 2:1109 – 1112, June 1998.

[9] N. Sokal and A. Sokal. Class e – a new class of high-efficiency, tuned single-ended switching power amplifier. *Solid State Circuits, Journal of*, 10:168 – 176, June 1975.

[10] D. Sugiharto, C. Yang, H. Le, and J. Chung. Beating the heat [cmos hot-carrier reliability]. *Circuits and Devices Magazine*, 14:43 – 51, September 1998.

[11] K. C. Tsai and P. R. Gray. A 1.9 ghz 1w cmos class e power amplifier for wireless communications. *Solid-State Circuits, IEEE Journal of*, 34:1712 – 1720, July 1999.

[12] S. H.-L. Tu and C. Toumazou. Design of low-distortion cmos class e power amplifier for wireless communications. *Electronics, Circuits and Systems*, 3:1433 – 1436, September 1999.