# A Temperature-to-Digital Converter for a MEMS-Based Programmable Oscillator With $<\pm 0.5$-ppm Frequency Stability and $<1$-ps Integrated Jitter

Michael H. Perrott, *Senior Member, IEEE*, James C. Salvia, Fred S. Lee, Aaron Partridge, Shouvik Mukherjee, Carl Arft, Jintae Kim, Niveditha Arumugam, Pavan Gupta, Sassan Tabatabaei, Sudhakar Pamarti, Haechang Lee, and Fari Assaderaghi

***Abstract*—MEMS-based oscillators offer a silicon-based alternative to quartz-based frequency references. Here, a MEMS-based programmable oscillator is presented which achieves better than $\pm$0.5-ppm frequency stability from $-40\,^{\circ}$C to 85 °C and less than 1-ps (rms) integrated phase noise (12 kHz to 20 MHz). A key component of this system is a thermistor-based temperature-to-digital converter (TDC) which enables accurate and low noise compensation of temperature-induced variation of the MEMS resonant frequency. The TDC utilizes several circuit techniques including a high-resolution tunable reference resistor based on a switched-capacitor network and fractional-N frequency division, a switched resistor measurement approach which allows a pulsed bias technique for reduced noise, and a VCO-based quantizer for digitization of the temperature signal. The TDC achieves 0.1-mK (rms) resolution within a 5-Hz bandwidth while consuming only 3.97 mA for all analog and digital circuits at 3.3-V supply in 180-nm CMOS.**

***Index Terms*—Fractional-$N$ frequency synthesizer, high frequency stability, low phase noise, MEMS, phase-locked loop (PLL), pulsed biasing, quartz alternative, reference frequency, switched-capacitor resistor, switched resistor, temperature compensation, temperature-to-digital, thermistor, VCO-based quantizer.**

## I. Introduction

TIMING devices are required in virtually every electronic system and represent a multibillion dollar market. Recently, there has been much interest in replacing traditional quartz-based oscillators with silicon-based alternatives [1]–[9]. When seeking high frequency stability, MEMS-based oscillators have offered the most promising silicon-based solution with state-of-the-art frequency stability for non-ovenized implementations being reported at $\pm 10$ ppm [10]. Frequency stability for ovenized MEMS-based oscillator implementations has been reported at $\pm 0.05$ ppm [8], but correction of fabrication variation and programmable output frequency was not addressed. In this paper, a programmable MEMS-based oscillator is presented that achieves frequency stability of better than $\pm 0.5$ ppm over a $-40\,^{\circ}$C to 85 °C temperature range, thereby improving state of the art frequency stability performance for non-ovenized implementations by over an order of magnitude while also providing correction of fabrication variation and a fully programmable output frequency. The key circuit to obtain such improvement is a thermistor-based temperature-to-digital converter (TDC) that achieves 0.1-mK (rms) resolution within a 5-Hz bandwidth.

The overall circuit architecture of the presented MEMS-based programmable oscillator is shown in block diagram form in Fig. 1. In this approach, a MEMS resonator is wire bonded to a CMOS die that includes an oscillator sustaining circuit, temperature sensor, fractional-$N$ synthesizer, and various supporting circuitry. The output of the sustaining circuit is a 48-MHz reference frequency, $F_{RES}$, which is immediately doubled to 96 MHz and then fed into a fractional-$N$ synthesizer [11]. The fractional-$N$ synthesizer outputs any frequency between 2.1 and 2.6 GHz with better than 1-ppb resolution, and the relatively high reference frequency of 96 MHz allows a wide PLL bandwidth greater than 500 kHz in order to suppress VCO noise [11]. By sending the fractional-$N$ synthesizer output into a programmable frequency divider (i.e., divide-by-$M$ circuit), any frequency in the range of 0.5–220 MHz can be achieved through proper combination of the fractional-$N$ synthesizer and programmable divider settings.

As illustrated in Fig. 1, a key issue of the MEMS resonator frequency is that it varies with temperature by approximately $-31$ ppm/°C. Uncompensated, this leads to an output frequency variation of approximately 4000 ppm from $-40\,^{\circ}$C to 85 °C. However, this temperature variation is corrected by using a TDC to sense the resonator temperature and then adjust the output frequency through the high resolution tuning path of the fractional-$N$ synthesizer. Digital fifth order polynomial correction, which operates on the digital inverse of the TDC

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M. H. Perrott was with SiTime Corporation, Sunnyvale, CA 94085 USA. He is now with Masdar Institute of Science and Technology, Microsystems Program, Abu Dhabi, United Arab Emirates (e-mail: mhperrott@gmail.com)..

J. C. Salvia, A. Partridge, S. Mukherjee, C. Arft, N. Arumugam, P. Gupta, S. Tabatabaei, and H.-C. Lee are with SiTime Corporation, Sunnyvale, CA 94085 USA.

F. S. Lee was with SiTime Corporation, Sunnyvale, CA 94085 USA. He is now with Fairchild Semiconductor, San Jose, CA 95134 USA.

J.-T. Kim was with SiTime Corporation, Sunnyvale, CA 94085 USA. He is now with the Electronics Engineering Department, Konkuk University, Gwangjin-gu, Seoul, Korea.

S. Pamarti is with the University of California, Los Angeles, CA 90095 USA.

F. Assaderaghi was with SiTime Corporation, Sunnyvale, CA 94085 USA. He is now with InvenSense, Sunnyvale, CA 94089 USA.

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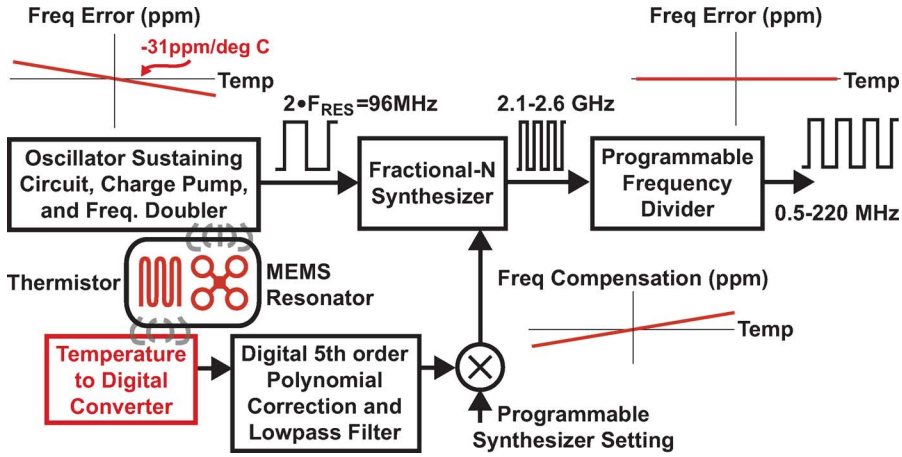


Fig. 1. Programmable MEMS-based oscillator circuit consisting of a MEMS die composed of a resonator and thermistor wire-bonded to a CMOS die which includes a sustaining circuit, fractional-$N$ synthesizer, programmable frequency divider, temperature compensation circuits, and supporting circuitry.

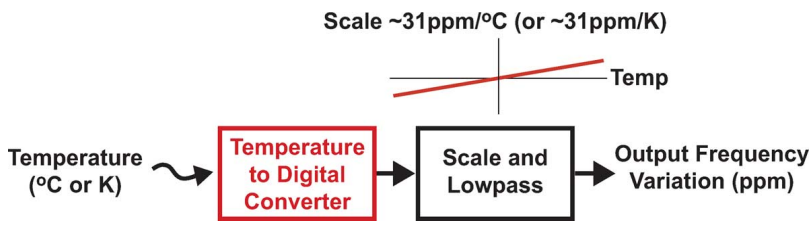


Fig. 2. Impact of TDC noise on output frequency variation of oscillator.

output, compensates for curvature in the TDC characteristic, and digital filtering attenuates high-frequency TDC noise. This paper demonstrates that this approach achieves better than ±0.5 ppm frequency stability from −40 °C to 85 °C after compensation [12].

As shown in Fig. 2, noise in the TDC leads to variation of the output frequency according to a scale factor set by the required slope of the compensation path. While low-pass filtering reduces the impact of TDC noise at higher frequencies, the bandwidth of such filtering must be set adequately high to allow reasonable tracking of instantaneous frequency variations in the MEMS resonator due to temperature. Since relatively low tracking bandwidth is acceptable for many applications, frequency variation due to TDC noise occurs at relatively long time scales and is characterized by an Allan Deviation specification [13].

In this work, our goal is to achieve less than 5-ppb Allan Deviation at strides of 0.1, 1, and 10 s. One can think of stride as a windowed sampling of instantaneous frequency, where the window length sets the bandwidth of an effective sinc function filter. As an example, a 0.1-s stride corresponds to measuring frequency at a 10-S/s rate with effective sinc filter bandwidth of approximately 5 Hz. Since longer strides correspond to longer windows (i.e., lower bandwidth), the maximum bandwidth of concern for strides greater than or equal to 0.1 s is 5 Hz.

To achieve better than 5-ppb Allan Deviation performance at 0.1-s stride, the required TDC noise within a 5-Hz bandwidth is calculated as

$$5\ \text{ppb(rms)}\frac{1}{31\ \frac{\text{ppm}}{\text{K}}} = 161\ \mu\text{K(rms)}. \tag{1}$$

As such, the desired Allan Deviation performance leads to a very challenging requirement that the TDC noise be of the order of 100 $\mu$K(rms) within a 5-Hz bandwidth (i.e., 10 S/s). Such TDC noise performance is a challenging requirement given the current state of the art of 2 mK at 1 S/s [14], 5 mK at 10 S/s [15], and 40 mK at 32 S/s [10].

To address this challenge, this paper presents a thermistor-based TDC circuit that achieves 100-$\mu$K(rms) resolution within a 5-Hz bandwidth with low area and state-of-the-art power efficiency. Incorporated within a MEMS-based programmable oscillator, the TDC enables better than ±0.5-ppm frequency stability and less than 5-ppb Allan Deviation at strides of 0.1 , 1, and 10 s. Section II provides a short background section that highlights the advantages of thermistor-based temperature sensing over bipolar designs for this application space. Section III presents the proposed TDC architecture along with key circuit techniques to enable high performance. Section IV provides noise analysis of the TDC, and Section V presents measured results of the TDC as well as the overall MEMS-based programmable oscillator. Finally, Section VI concludes.

## II. Background

Fig. 3 compares bipolar and thermistor-based TDC circuits. The bipolar design is typically based on voltage signals obtained by using two bipolar devices with different areas and/or emitter currents. In particular, the impact of temperature on the difference of $V_{\text{BE}}$ voltages is calculated as

$$\Delta V_{\text{BE}} = V_{\text{BE}} - V_{\text{BE2}} = \frac{kT_K}{q}\ln\left(\frac{I_{c1}}{I_{c2}}\frac{A_2}{A_1}\right) \tag{2}$$

where $k$ is the Boltzmann constant, $q$ is the magnitude of charge of an electron, $T_K$ is temperature in Kelvin, and $A_1$ and $A_2$ are the emitter areas of the bipolar transistors whose collector currents are $I_{c1}$ and $I_{c2}$, respectively. Given a typical ratio of

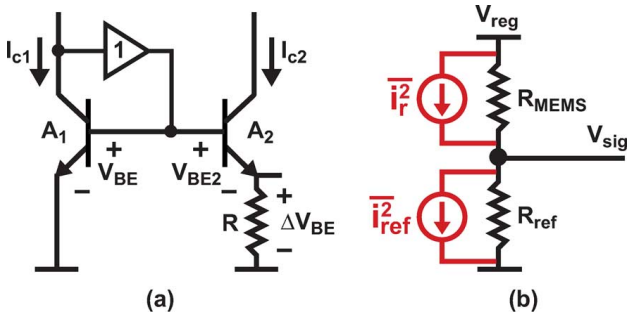


Fig. 3. Comparison of temperature sensing approaches. (a) Bipolar-based. (b) Thermistor-based.

$(I_{c1}/I_{c2}) \cdot (A_2/A_1) \approx 8$, $\Delta V_{\rm BE}$ has a temperature-to-voltage signal of approximately 180 $\mu$V/°C, and $V_{\rm BE}$ has a temperature-to-voltage signal of approximately $-2$ mV/°C. Intuitively, the effective signal-to-noise ratio (SNR) of $\Delta V_{\rm BE}$ is relatively low due to its small temperature-to-voltage signal. Bipolar temperature sensors often leverage both $V_{\rm BE}$ and $\Delta V_{\rm BE}$ to achieve accurate performance, with a ratio of $\Delta V_{\rm BE}/V_{\rm ref}$ or $V_{\rm BE}/V_{\rm ref}$ typically being formed, where $V_{\rm ref} = V_{\rm BE} + \alpha \Delta V_{\rm BE}$ and $\alpha$ is a gain factor chosen such that $V_{\rm ref}$ is relatively constant with temperature [16]. Unfortunately, both ratios suffer from inclusion of the low SNR signal $\Delta V_{\rm BE}$, which complicates efforts of achieving an extremely low-noise TDC as targeted in this paper. An additional issue for a MEMS-based oscillator application is that it is fairly costly to integrate high-quality bipolar devices on the MEMS die as desired for best thermal tracking of the MEMS resonator.

In contrast, a thermistor-based temperature sensor [17], as shown in Fig. 3(b), offers a relatively high temperature-to-voltage signal and utilizes a single-crystal silicon, temperature-sensitive resistor, $R_{\rm MEMS}$, that is cofabricated on the same die as the MEMS resonator using the SiTime MEMS First process [18], [19]. This process allows the thermistor to be hermetically vacuum encapsulated and anchored such that it is isolated from external mechanical stresses that adversely affect traditional BJT temperature sensors [19]. Cofabrication allows less than 200-$\mu$m separation between resonator and thermistor, thus allowing close thermal tracking of the two elements. A four-point topology is used for the thermistor to avoid having its temperature-dependent resistance be influenced by the resistance of the wirebonds and metal interconnects.

The temperature-sensitive voltage signal is produced by creating a voltage divider circuit with $R_{\rm MEMS}$ and a reference resistor, $R_{\rm ref}$, which is assumed to be relatively temperature-stable. Given the measured resistance versus temperature curve of $R_{\rm MEMS}$ shown in Fig. 4, the corresponding slope of resistance change versus temperature is 0.32% per °C at room temperature. If we assume that $V_{\rm reg} \approx 1.3$ V and $R_{\rm MEMS} \approx R_{\rm ref}$ at room temperature, the temperature-to-voltage signal of the thermistor-based temperature sensor is calculated to be

$$\begin{aligned}\Delta V_{\rm sig} &\approx \frac{1}{4}\left(\frac{\Delta R_{\rm MEMS}}{R_{\rm MEMS}}\right) V_{\rm reg} \\ &\approx \frac{1}{4}\left(\frac{0.0032}{^\circ{\rm C}}\right) 1.3\ {\rm V} \\ &= 1.04\ \frac{\rm mV}{^\circ{\rm C}}. \end{aligned} \tag{3}$$

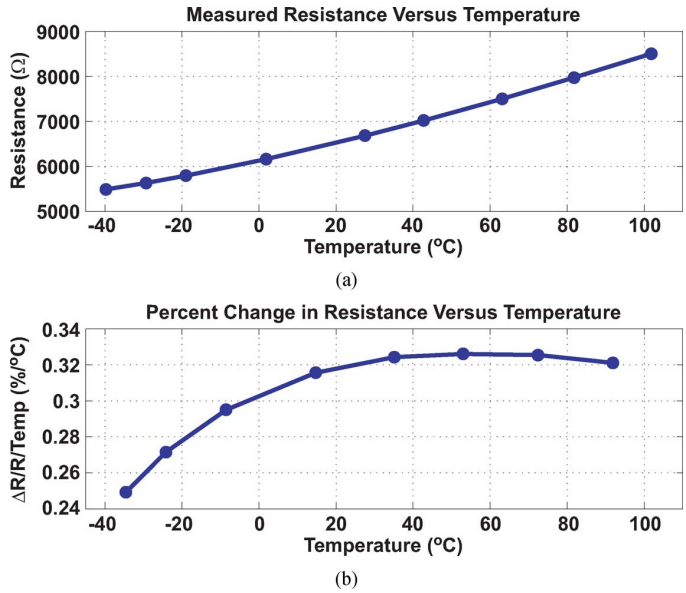


Fig. 4. Measured characteristics of MEMS thermistor. (a) Resistance versus temperature. (b) Percent change in resistance versus temperature.

Note that (3) reveals a significantly larger temperature-to-voltage signal than the typical $\Delta V_{\rm BE}$ value of 180 $\mu$V/°C for a bipolar TDC.

To better understand the fundamental resolution limits of the thermistor temperature sensor shown in Fig. 3(b), the single-sided noise spectral density of its output is calculated as

$$\overline{v_{sig}^2} = \left(\overline{i_r^2} + \overline{i_{\rm ref}^2}\right)\left(R_{\rm MEMS} \| R_{ref}\right)^2 \frac{V^2}{\rm Hz}. \tag{4}$$

Assuming $R_{\rm MEMS} = R_{\rm ref} = 6.6\ {\rm k}\Omega$, and the bandwidth of interest is 5 Hz, the rms voltage noise is obtained as

$$\begin{aligned}\sigma_{V_{\rm sig}} &= \sqrt{\overline{v_{\rm sig}^2} \cdot 5\ {\rm Hz}} \\ &= \sqrt{2\frac{4kT_K}{6.6\ {\rm k}\Omega}(3.3\ {\rm k}\Omega)^2 \cdot 5\ {\rm Hz}} \\ &= 16.5\ {\rm nV(rms)} \end{aligned} \tag{5}$$

where $T_K$ is assumed to have a room temperature value of 298 K. Combining (3) and (5), the fundamental resolution limit within a 5-Hz bandwidth under the given assumptions for the thermistor-based TDC is calculated as

$$\begin{aligned}{\rm TS\ resolution} &= \frac{16.5\ {\rm nV(rms)}}{1.04\ \frac{\rm mV}{^\circ{\rm C}}} \\ &= 15.9\ \mu^\circ{\rm C(rms)} \\ &= 15.9\ \mu{\rm K(rms)}. \end{aligned} \tag{6}$$

As such, our goal of achieving 100 $\mu$K(rms) within a 5-Hz bandwidth is attainable with this structure.

## III. Proposed TDC Architecture

Here, we provide details of the proposed TDC. We first discuss a key strategy of its implementation, which is to simplify digitization of the temperature signal through the use of a

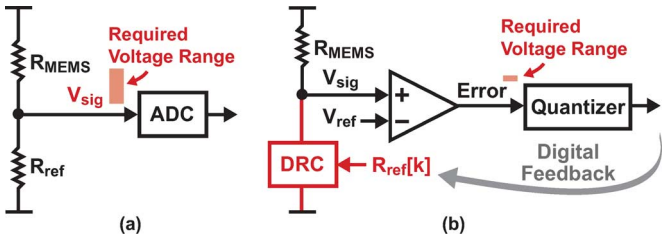


Fig. 5. Comparison of required digitization complexity for (a) constant $R_{\rm ref}$ and (b) tunable $R_{\rm ref}$ which tracks $R_{\rm MEMS}$.

high-resolution tunable reference resistor. A switched resistor method combined with a pulsed bias technique is then presented which removes much of the bias noise using a correlated double-sampling technique. A pseudodifferential version of the resistance error measurement circuit is then proposed, followed by a description of a VCO-based quantizer used to digitize this error. Finally, the overall TDC system is presented.

### *A. Simplification of the Digitization Process Using a Tunable Reference Resistor*

While the temperature sensor is at the heart of any TDC, the key performance bottleneck often becomes the analog-to-digital converter (ADC) needed to digitize the temperature signal. Therefore, there is great advantage in choosing a TDC architecture that simplifies the digitization process such that analog complexity is reduced and high performance is achieved.

Fig. 5 compares a strategy in which (a) an ADC digitizes the overall temperature signal versus (b) a multibit quantizer digitizes a residual error signal. The latter approach allows significant reduction of the required signal range for performing quantization, thereby simplifying the quantizer design in achieving a given level of quantization noise performance. However, approach (b) also imposes the challenge of achieving a digitally tunable reference resistor, which we will refer to as a digital-to-resistance converter (DRC), that has a wide tuning range and very high resolution. In effect, the DRC digital control value becomes the effective output of the TDC, which is set through a digital feedback path based on the residual error measured by the quantizer.

The proposed high-resolution DRC is achieved with the fully integrated switched capacitor network shown in Fig. 6. On average, the effective resistance of this network is given as

$$R_{ref} = \frac{T_{\rm clk}}{C_2} = \frac{T_{480}}{C_2} N_{\rm nom} \tag{7}$$

where $T_{\rm clk}$ is the period of the clock that controls the switching action of $C_2$ between $C_1$ and ground. Note that $C_1$ is much larger than $C_2$ and acts as a charge reservoir which provides low-pass filtering of the switching action of $C_2$ on node $V_{\rm sig}$. $T_{clk}$ is formed through frequency division of a high-speed reference clock $\rm clk_{480}(t)$, whose period is defined as $T_{480}$. By using a digital $\Delta$-$\Sigma$ modulator, the instantaneous divider values $N[k]$ are dithered such that their average matches the input to the modulator $N_{\rm nom}[k]$. This approach allows extremely high resolution control of the DRC. At steady state, where $R_{\rm ref} = R_{MEMS}$, $N_{\rm nom}[k]$ becomes

$$N_{\rm nom} = \frac{C_2}{T_{480}} R_{\rm ref} = \frac{C_2}{T_{480}} R_{\rm MEMS}. \tag{8}$$

Note that $N_{\rm nom}[k]$ must be greater than one under all conditions in order to achieve a practical frequency divider implementation.

A low value for $T_{480}$ is desirable to reduce the noise impact of the $\Delta$-$\Sigma$ dithering operation on $T_{clk}$ as depicted in Fig. 6. Also, (8) reveals that a low value of $T_{480}$ enables a small capacitor value for $C_2$. Realization of $1/T_{480} = 480$ MHz is achieved using an integer-N phase-locked loop (PLL) whose reference frequency is the clock-doubled MEMS sustaining circuit output of $2 \cdot F_{RES} = 96$ MHz. While this leads to a reference frequency that slightly varies with temperature due to its dependence on $F_{RES}$, such variation is quite small compared to that of $R_{MEMS}$ and can therefore be taken out by polynomial correction of the TDC output. Also, it is important to note that the switched capacitor network is fairly insensitive to jitter of its clock [20], which allows a compact and low power implementation of the integer-N PLL since its phase noise performance can be somewhat relaxed.

### *B. Switched Resistor Measurement Technique With Low Noise Pulse Biasing*

Fig. 7 displays our proposed method of comparing $R_{MEMS}$ and $R_{ref}$ in which a CMOS switch is placed between the two resistors. This approach avoids the need for an explicit reference voltage and differential amplifier, thus saving power and area.

To explain the operation of the proposed resistor comparison circuit, first consider the case where the switch is open such that $V_R(t)$ settles to $V_{\rm reg}$ and $V_C(t)$ settles to ground. When the switch is closed, $V_R(t)$ and $V_C(t)$ will rapidly change in opposite directions and settle to the same voltage value (assuming negligible switch resistance). In case of equal values of resistance, the movement of $V_R(t)$ and $V_C(t)$ will be equal and opposite. As discussed later in the paper, the frequency of opening and closing the switch $1/T_{\rm chop}$ is chosen to be in the tens-of-kilohertz range, which is much lower than the switching frequency of $C_2$ in Fig. 6 which is in the tens-of-megahertz range.

Given the above observation and ignoring transients, summation and amplification of $V_R(t)$ and $V_C(t)$ leads to a signal, $V_{\rm amp}(t)$, that does not change between switch positions if $R_{\rm MEMS}$ and $R_{\rm ref}$ have equal values. However, any mismatch in the resistance values will lead to $V_{\rm amp}(t)$ having a nonzero peak-to-peak amplitude as indicated in Fig. 7. The peak-to-peak amplitude is measured by performing a pairwise subtraction of a windowed average voltage of $V_{\rm amp}(t)$ in the two switch positions as

$$V_{\rm avg1}[k] - V_{\rm avg2}[k] \approx {\rm Gain} \frac{R_{\rm ref} - R_{\rm MEMS}}{R_{\rm ref} + R_{\rm MEMS}} V_{\rm reg}. \tag{9}$$

The averaging windows for $V_{\rm avg1}[k]$ and $V_{\rm avg2}[k]$ are chosen to avoid being influenced by transient effects. As expected, the peak-to-peak amplitude computed in (9) becomes zero if $R_{\rm MEMS}$ equals $R_{\rm ref}$ and is otherwise positive or negative depending on the sign of the error between the two resistor values. Note also that a small amount of resistance in the switch does not alter the fact that (9) will only be zero when the resistor values are equal since the steady-state current through each resistor must be identical when the switch is on.

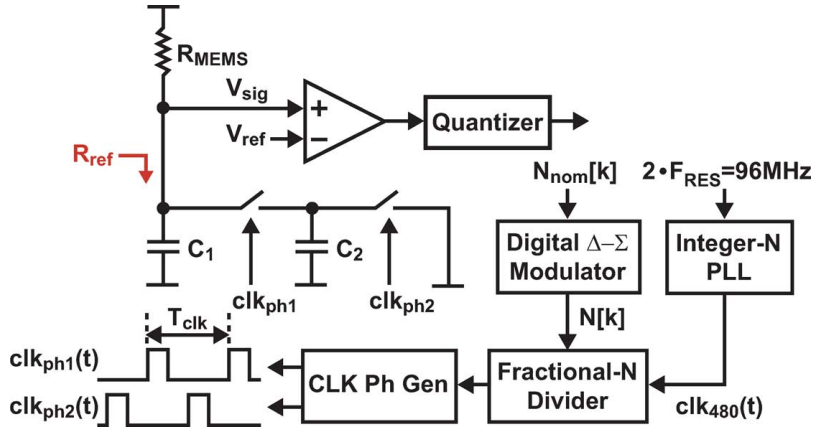


Fig. 6. Implementation of a high resolution DRC using a switched capacitor network and fractional-$N$ frequency division.

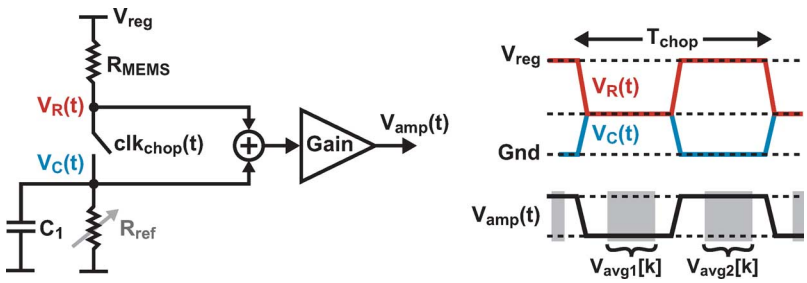


Fig. 7. Proposed switched resistor measurement technique for measuring error between $R_{\mathrm{ref}}$ and $R_{\mathrm{MEMS}}$.

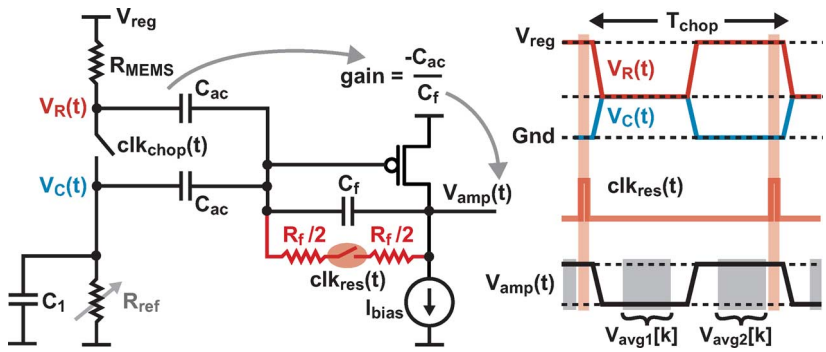


Fig. 8. Implementation of switched-resistor measurement technique using a capacitively coupled addition amplifier along with a pulsed bias feedback resistor.

Summation and amplification of $V_R(t)$ and $V_C(t)$ is implemented with the capacitively coupled amplifier circuit shown in Fig. 8. Metal finger caps are used to implement $C_{\mathrm{ac}}$ and $C_f$ in order to obtain high linearity in the summation operation. Careful layout of the $C_{\mathrm{ac}}$ capacitors is performed since mismatch between them leads to steady-state mismatch between $R_{\mathrm{MEMS}}$ and $R_{\mathrm{ref}}$; a small amount of mismatch is tolerable since the digital polynomial correction will correct for such issues. Overall, Fig. 8 indicates that the proposed switched resistor temperature sensor structure is quite simple, with a common-source PMOS amplifier being used as the active element.

Capacitively coupled amplifiers operated in a continuous-time manner typically require a very large feedback resistor in order to provide input biasing of the amplifier. A large feedback resistor leads to long settling times for the amplifier as well as significant noise at low frequencies. As shown in Fig. 8, we can take advantage of the pairwise measurement approach to significantly reduce the resistor value through a pulse biasing technique. By pulsing the resistor on *between* pairwise measurements, the settling characteristic caused by the resistor does not directly influence the individual pairwise measurements. In fact, the noise generated by the resistor will be sampled when the switch is turned off and, therefore, cancelled out by the subtraction operation given in (9) since it is common to each of the pairwise measurements. Here, we see that the pairwise subtraction operation in (9) corresponds to a correlated double-sampling technique.

The pulsed bias technique can be taken a step further by applying it to the current bias and voltage regulator of the resistor comparison circuit as shown in Fig. 9. The current bias consists of a current mirror circuit in which resistive degeneration is used to lower the impact of $1/\mathrm{f}$ noise, and the mirror voltage is sampled onto an $RC$ network, formed by $R_{\mathrm{bias}}$ and $C_{\mathrm{bias}}$, which lowers the impact of charge injection. Similarly, a simple

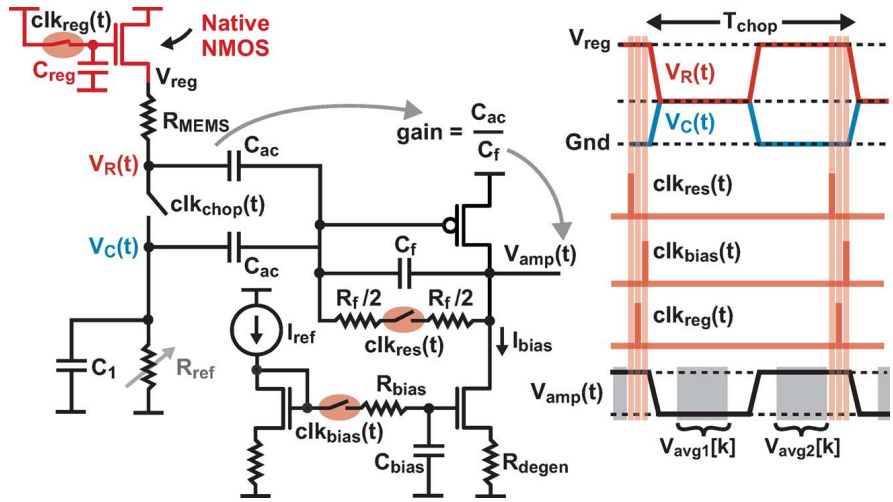


Fig. 9. Application of pulsed bias technique to the current source and voltage reference of the resistor error measurement circuit.

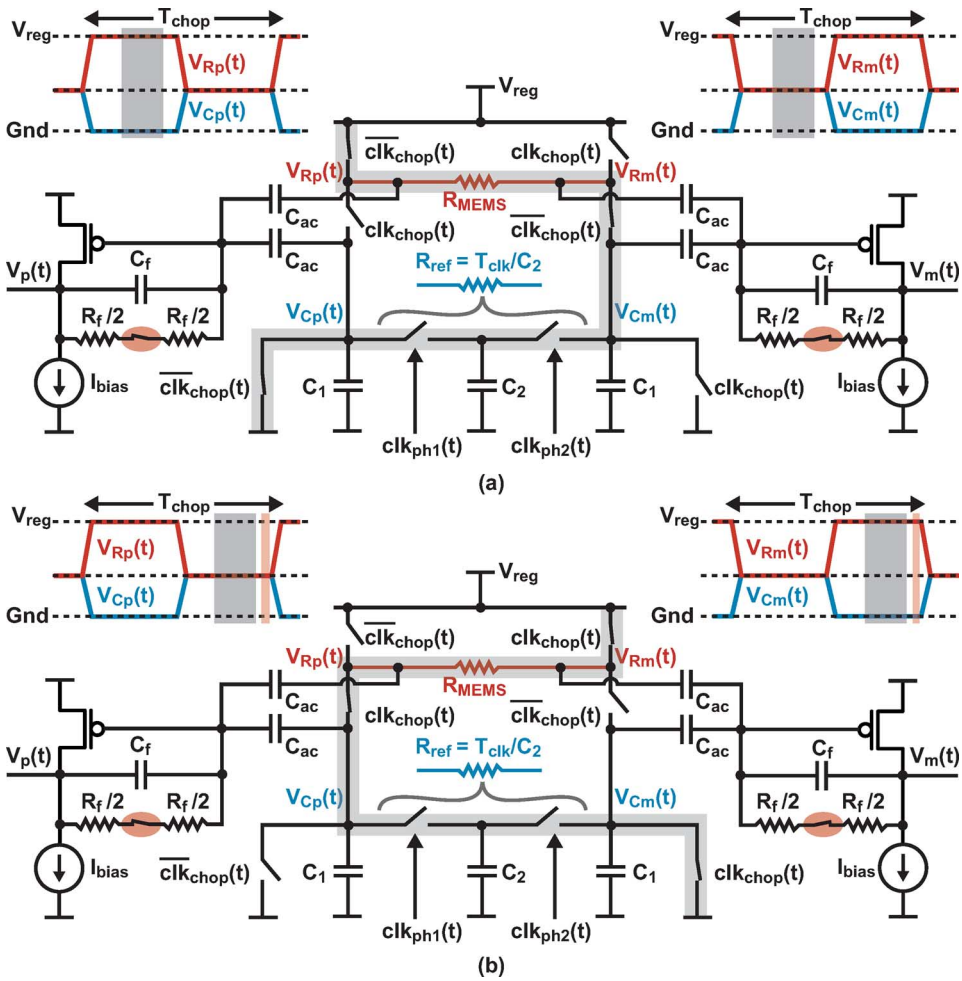


Fig. 10. Pseudodifferential version of the resistor error measurement circuit in which (a) the first half of the chop cycle occurs and (b) the second half of the chop cycle occurs.

voltage regulator is achieved by sampling the supply voltage onto the gate of a native NMOS. In both cases, the on-time of the sampling operation is placed between pairwise measurements, which leads to cancellation of the sampled bias noise. Note that, during the pairwise measurements, the native NMOS regulator suppresses small perturbations on the supply according to its intrinsic gain, $g_m r_o$. Also, in order to avoid undesirable coupling, the pulsed bias of the resistor feedback, current bias, and voltage regulator are designed to occur in a nonoverlapping manner as depicted in the figure.

Finally, Fig. 10 displays a pseudodifferential version of the resistor comparison circuit. The structure shares the MEMS

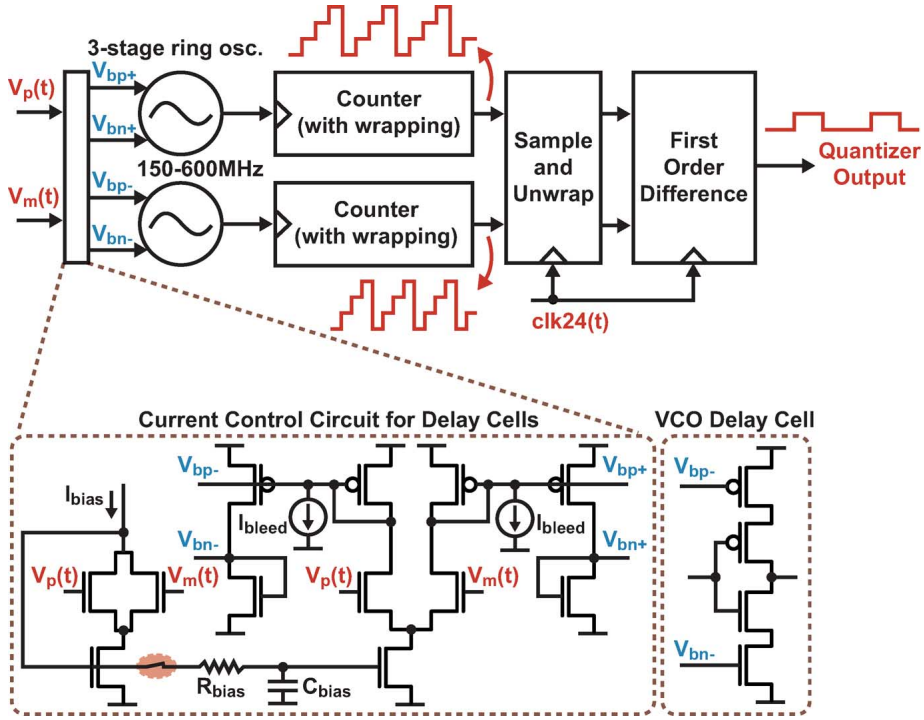


Fig. 11. VCO-based quantizer implementation.

thermistor, $R_{\mathrm{MEMS}}$, and reference resistor capacitor, $C_2$, with each side of the pseudodifferential circuit so that excellent matching is achieved between the two sides. As the figure indicates, the nodes $V_R(t)$ and $V_C(t)$ are connected to the regulated supply and ground or to each other in opposite phases of $\mathrm{clk}_{\mathrm{chop}}(t)$. Also, the four-point topology of the MEMS thermistor is utilized to avoid the impact of wirebonds and metal interconnects on its resistance versus temperature characteristic. The overall pseudodifferential TDC structure offers cancellation of noise sources common to each path such as regulator noise on node $V_{\mathrm{reg}}$, significant reduction of electromigration effects on $R_{\mathrm{MEMS}}$, and a convenient differential output signal to feed into the quantizer circuit which follows.

### C. VCO-Based Quantizer

While several different architectures could be utilized for digitizing the resistor error signal, the VCO-based quantizer structure, shown in Fig. 11, offers the advantage of providing a highly digital implementation that is relatively simple to design. Here the pseudodifferential outputs of the resistor comparison circuit, $V_p(t)$ and $V_m(t)$, are fed into two free-running voltage-controlled ring oscillators [21], [22], [31]. The difference in voltage between $V_p(t)$ and $V_m(t)$ is manifested as a difference in frequency between the two oscillators. Digital counter structures record the accumulated phase of each oscillator, and the digital count values are sampled at the edges of a 24-MHz reference clock $\mathrm{clk}_{24}(t)$. After sampling, the count values are unwrapped and then compared with the previous count values such that a first-order difference operation is achieved. The first-order difference effectively converts the sampled phase of the oscillators (in the form of their count values) to quantized frequency and acts to first-order noise shape the resulting quantization noise. Subtraction of the quantized frequency values then yields the quantized frequency difference between the oscillators, which corresponds to a digitized representation of the difference in input voltages, $V_p(t) - V_m(t)$.

As shown in Fig. 11, the delay cells of the oscillators correspond to current starved inverters which have both NMOS and PMOS control devices. An analog current control circuit is used to set the voltages of the delay cell control nodes, and operates by directing current from a differential pair into current mirrors which separately control the two oscillators. This control circuit yields a relatively constant value for the sum of the oscillator currents, and also enforces a minimum frequency value of approximately 150 MHz for each of the oscillators through the use of bleeder currents as shown in the figure. Also, the pulse biasing technique is used to eliminate the noise from the current bias by sampling the current bias voltage onto capacitor $C_{\mathrm{bias}}$ between the pairwise measurement windows as discussed in the previous subsection.

Finally, one should note that the control circuit and delay cells are the only analog circuits within the VCO-based quantizer, with the rest of the circuit being purely digital in its implementation. Since the differential input to the quantizer will be zero (ignoring offset and noise) under steady-state conditions, nonlinearity of the voltage-to-frequency characteristic of the oscillators is not of significant concern for this design.

### D. Overall System

Fig. 12 displays the overall TDC architecture which uses digital feedback to set $N_{\mathrm{nom}}[k]$ such that the value of the reference resistor, $R_{\mathrm{ref}}$, matches the value of the MEMS thermistor, $R_{\mathrm{MEMS}}$. As shown in the figure, this feedback is realized by performing windowed averaging of the VCO-based quantizer output in order to form $V_{\mathrm{avg1}}[k]$ and $V_{\mathrm{avg2}}[k]$, subtracting these

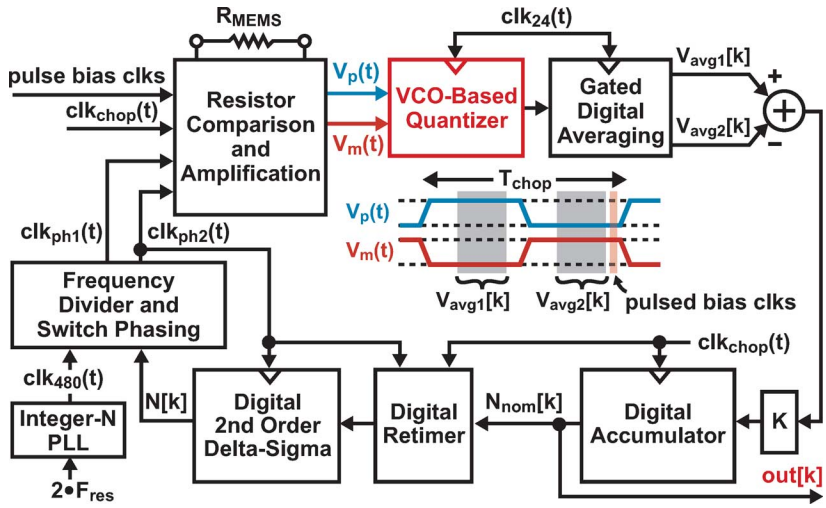


Fig. 12. Overall temperature-to-digital converter architecture.

two signals and scaling by factor $K$, and then feeding the resulting signal into an accumulator whose output sets the value of $N_{\rm nom}[k]$. Note that a digital retimer circuit is required between the accumulator output and digital second order $\Delta$–$\Sigma$ modulator since the latter circuit has a variable frequency clock, $\mathrm{clk}_{\rm ph2}(t)$, set by the output of the frequency divider forming $T_{\rm clk}$ for the switched capacitor network.

As revealed by Fig. 12, a key benefit of the proposed system architecture is that it provides a highly digital implementation of the TDC. Indeed, the only analog circuits required are the passive components and single-stage amplifiers used in the resistor comparison circuit along with the oscillator delay stages and control circuit used in the VCO-based quantizer. Note that, since the windowed averaging used to form signals $V_{\rm avg1}[k]$ and $V_{\rm avg2}[k]$ is performed in the digital domain, the subsequent subtraction of these signals removes the impact of all noise and offset common to these signals within the analog domain. This includes pulsed bias noise as well as offset of the pseudo-differential PMOS common-source amplifiers and VCO-based quantizer.

The windowed averaging causes the VCO-based quantizer to act like an incremental first-order $\Delta$-$\Sigma$ modulator [23]. Each $T_{\rm chop}$ period corresponds to 1024 $\mathrm{clk}_{24}(t)$ cycles such that $f_{\rm chop} = 1/T_{\rm chop} = 23.4$ kHz. Within this $T_{\rm chop}$ period, the averaging windows are chosen as 256 $\mathrm{clk}_{24}(t)$ cycles for both $V_{\rm avg1}[k]$ and $V_{\rm avg2}[k]$. The remaining 512 cycles outside of the averaging windows are used to avoid the impact of transients caused by changes in switch state within the resistor measurement circuit and for generation of the nonoverlapping pulsed bias clocks.

The closed-loop bandwidth of the feedback structure is set to be approximately 500 Hz through proper choice of the scaling factor $K$ indicated in Fig. 12, which helps in achieving fast initial settling of the TDC and is comfortably lower than the effective sampling rate of the feedback loop corresponding to $f_{\rm chop} = 23.4$ kHz. The closed-loop dynamics are designed to be stable across variations of the analog elements within its structure such as the $K_v$ value of the VCO-based quantizer. In the case of $K_v$ gain variations, for instance, the resulting change in open loop gain alters the closed loop bandwidth away from its 500-Hz nominal value, but no calibration is required to correct this issue since the TDC bandwidth is not a critical specification.

A subtle issue presented by the architecture in Fig. 12 is that the reduction of range in the VCO-based quantizer in order to achieve high resolution with a simple design also implies that it can saturate when significantly large disturbances occur. In such a case, the system responds in a slew rate limited fashion, thereby increasing the settling time compared to the linear response dictated by the 500 Hz bandwidth. Fortunately, since temperature variations typically occur within a bandwidth much less than 500 Hz, this does not present an issue for steady-state operation. Also, while this issue could present a problem when striving for fast settling at power-up, we can take advantage of the highly digital implementation of the TDC to adaptively change the feedback behavior when large errors are encountered and therefore counter the slew rate issue. A simple example of such an approach, which is implemented in the TDC digital logic, is to configure the feedback as a bang-bang system with large steps for a fixed time during power-up, after which it is reconfigured to have linear dynamics as represented in Fig. 12.

## IV. TDC Noise Analysis

Fig. 13 displays the analog circuits within the TDC and their associated noise sources. Here a single ended implementation is assumed for simplicity with the switch between resistors being closed. In the case where the switch between resistors is open, similar noise performance is obtained, as discussed below.

It is useful to categorize the various noise sources according to the circuit blocks of their origin. The core temperature sensor formed by the MEMS and reference resistor contains thermal noise $\overline{i_r^2}$ of $R_{\rm MEMS}$, $kT/C$ noise $\overline{i_{ktc}^2}$, of the switched capacitor network, and $\Delta$-$\Sigma$ quantization noise $\Delta T_{\rm ds}$ caused by variations of $T_{\rm clk}$. The amplifier circuit contains current noise $\overline{i_{\rm pmos}^2}$ of its PMOS device. Finally, the VCO-based quantizer contains input-referred $\overline{v_{\rm vco}^2}$, corresponding to the combined impact of its input-referred oscillator phase noise $\overline{v_{\rm vco\_pn}^2}$ and quantization noise $\overline{v_{\rm vco\_q}^2}$. As indicated in the figure, our noise calculations will be referenced to the input of the VCO-based quantizer while including the impact of its input-referred noise in our analysis.

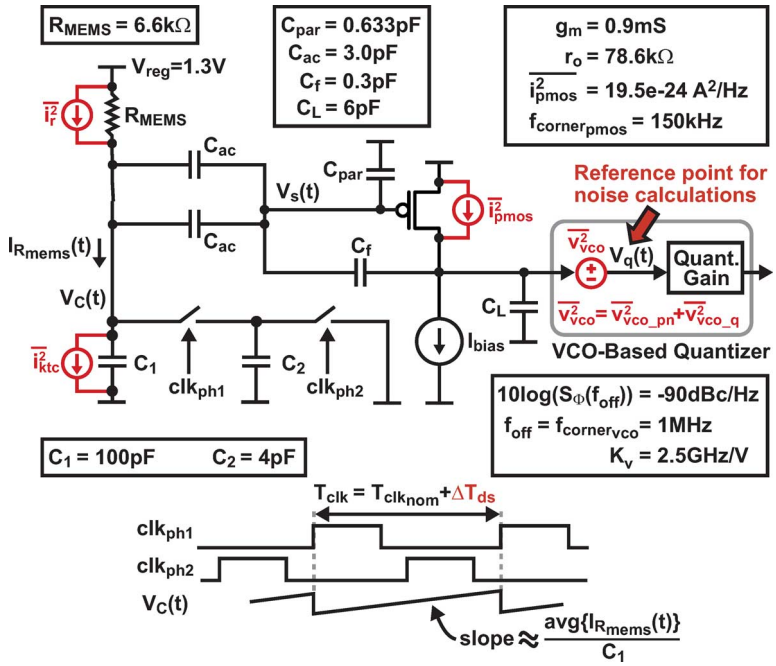


Fig. 13. Diagram and parameters for noise analysis.

We begin by examining the influence of the $kT/C$ noise generated within the switched capacitor network implementing $R_{\rm ref}$. Within a given period of $T_{\rm clk}$, two independent $kT/C$ noise events occur corresponding to when $C_2$ disconnects from capacitor $C_1$ and when $C_2$ disconnects from ground. Defining $T_{\rm clk_{nom}}$ as the nominal period of $T_{\rm clk}$, which is dithered according to the $\Delta$-$\Sigma$ modulator, the single-sided $kT/C$ current noise spectral density is calculated as

$$\overline{i_{ktc}^2} = 2\frac{1}{T_{\rm clk_{nom}}}2kT_K C_2 = 4kT_K\frac{1}{R_{\rm ref}}. \qquad (10)$$

Interestingly, the $kT/C$ noise of the switched-capacitor network is the same as would be encountered with a normal resistor of value $R_{\rm ref}$. As such, the fundamental noise performance of the temperature sensor portion of the TDC, which is set by $\overline{i_r^2}+\overline{i_{ktc}^2}$, is the same as earlier calculated in (5).

In order to explore the impact of the other noise sources shown in Fig. 13, it is useful to calculate their noise spectra referenced to signal node $V_q(t)$ as provided in Table I. These calculations include the effect of low-pass filtering by the PMOS amplifier and allow straightforward comparison of their relative impact on the overall noise performance of the TDC. Verification of these calculations was performed through transient noise simulation of the circuits using the CppSim simulator [24].

Given the parameter values shown in Fig. 13 and expressions in Table I, calculated noise spectra for each noise source referenced to node $V_q(t)$ are shown in Fig. 14. Focusing first on noise in the temperature sensor portion of the circuit, we note that the noise due to $R_{\rm MEMS}$ and $R_{\rm ref}$, $S_r(f)+S_{ktc}(f)$, is accompanied by an additional noise spectrum, $S_{ds}(f)$, caused by dithering of $T_{\rm clk}$ by amount $\Delta T_{\rm ds}$ according to the second order $\Delta$-$\Sigma$ modulator. Relatively speaking, $S_r(f)+S_{ktc}(f)$ dominates at low frequencies and $S_{\rm ds}(f)$ dominates at high frequencies due to the shaping action of the $\Delta$-$\Sigma$ modulator. A subtle issue, which is not shown in the figure for simplicity, is that $S_{\rm ds}(f)$ is filled in at low frequencies due to noise folding caused by the nonlinear behavior of the charge sampling process within the switched capacitor network. Fortunately, detailed CppSim simulations confirm that this folded noise is negligible compared with $S_r(f)+S_{ktc}(f)$.

Moving beyond temperature sensor noise, the PMOS amplifier and input-referred phase noise plus quantization noise of the VCO-based quantizer contribute noise spectra $S_{\rm pmos}(f)$ and $S_{\rm vco}(f)$, respectively, as shown in Fig. 14. Here $S_{\rm vco}(f)$ has only slight impact on the system, which is due to the fact that amplification by the PMOS amplifier lowers its relative contribution compared to other noise sources. In fact, $S_{\rm pmos}(f)$ is the dominant noise source for the TDC at frequencies less than 1 MHz, with the key contributor being $1/f$ noise in the PMOS device. Note that this observation will also be true when the switch between resistors is open since this condition will only remove the impact of the non-dominant noise spectra $S_r(f)+S_{ktc}(f)$ and $S_{\rm ds}(f)$.

The impact of $S_{\rm pmos}(f)$ on the overall TDC noise performance is set by the windowed chopping action in the system as depicted in Fig. 15. In particular, this chopping action modulates the spectral density of $S_{\rm pmos}(f)$ from frequencies $f_{\rm chop}, 2f_{\rm chop}$, etc. to baseband according to the Fourier-series coefficients of the chop waveform shown in the figure. The dominant impact of $S_{\rm pmos}(f)$ is caused by its spectral density at $f_{\rm chop}$, which is roughly 9 dB higher than the spectral density of the temperature sensor noise, $S_r(f)+S_{ktc}(f)$, as shown in Fig. 14.

The windowed chopping action causes an additional SNR penalty in the system due to the fact that the chop waveform is nonzero only half of the time and that the resistor divider circuit alternates between signal and reference values during each $T_{\rm chop}$ period. To explain, let us assume that $V_{\rm avg1}[k]$ corresponds to where the switch between resistors is closed and $V_{\rm avg2}[k]$ to where the switch between resistors is open. In such

TABLE I
TDC SINGLE-SIDED NOISE SPECTRAL DENSITY CALCULATIONS REFERENCED TO SIGNAL NODE $V_q(t)$.

**Calculations of TDC Single-Sided Noise Spectra**

| |
|---|
| $S_r(f) = 2\frac{2kT_K}{R_{MEMS}}\lvert H_{rc}(f)\rvert^2\lvert G_{amp}(f)\rvert^2$ |
| $S_{ktc}(f) = 2\frac{1}{T_{clk_{nom}}}2kT_KC_2\lvert H_{rc}(f)\rvert^2\lvert G_{amp}(f)\rvert^2$ |
| $S_{ds}(f) = 2\frac{1}{T_{clk_{nom}}}\frac{\Delta q_{ds}^2}{12}\lvert H_{ds}(z)\rvert^2\lvert H_{cap}(f)\rvert^2\lvert G_{amp}(f)\rvert^2$ |
| $S_{pmos}(f) = \overline{i_{pmos}^2}\left\lvert\frac{1}{g_m}\right\rvert^2\left\lvert\frac{2C_{ac}+C_{par}+C_f}{2C_{ac}}G_{amp}(f)\right\rvert^2(1+\frac{f_{corner_{pmos}}}{f})$ |
| $S_{vco\_pn}(f) = 2\left\lvert\frac{f_{off}}{K_v}\right\rvert^2 S_\Phi(f_{off})(1+\frac{f_{corner_{vco}}}{f})$ |
| $S_{vco\_q}(f) = 2\frac{\Delta q_{vco}^2}{12}\frac{T_{chop}}{2}$, where $\Delta q_{vco} = \frac{1}{K_vT_{chop}/4}$ |

**Supporting Definitions and Calculations**

| |
|---|
| $G_{amp}(s) = \frac{2C_{ac}}{C_f}\frac{B_{amp}H_{amp}(s)}{1-B_{amp}H_{amp}(s)}$ |
| $H_{amp}(s) = \frac{-g_mr_o}{1+sr_o(C_L+C_f)}$, $B_{amp} = \frac{C_f}{2C_{ac}+C_{par}+C_f}$ |
| $H_{rc}(s) = \frac{R_{eff}}{1+sR_{eff}C_1}$, $R_{eff} = R_{MEMS}\lVert R_{ref} = R_{MEMS}/2$ |
| $H_{cap}(s) = \frac{R_{MEMS}}{1+sR_{MEMS}C_1}$ |
| $H_{ds}(z) = (1-z^{-1})^2$, $z = e^{j2\pi fT_{clk_{nom}}}$ |
| $\Delta q_{ds} = T_{480}\,avg\{I_{R_{mems}}(t)\} = T_{480}\frac{V_{reg}/2}{R_{MEMS}}$ |

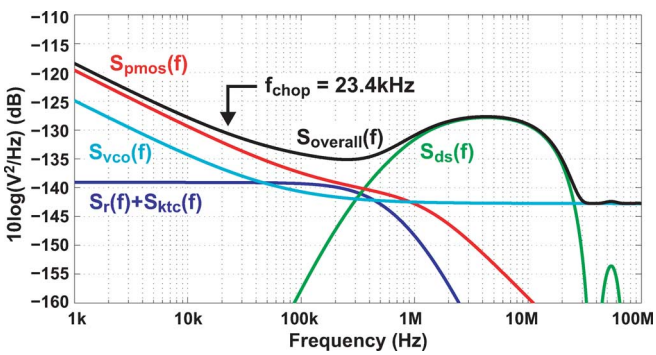


Fig. 14. Calculated noise spectra referenced to signal node $V_q(t)$.

case, only $V_{\text{avg1}}[k]$ sees the voltage divider signal formed by the two resistors; $V_{\text{avg2}}[k]$ instead sees a reference signal formed by setting $V_R(t)$ and $V_C(t)$ to supply and ground, respectively. As such, the signal averaging window is only one quarter of the $T_{\text{chop}}$ period, and the noise averaging window is half of the $T_{\text{chop}}$ period. For white noise, this would lead to a penalty in SNR of 9 dB, but the shaped spectrum of $S_{\text{pmos}}(f)$ somewhat reduces this penalty to about 8 dB. Fortunately, the pseudodifferential TDC implementation provides a 3-dB boost in SNR, though it comes at a cost of twice the power and area.

Overall, when combining the influence of the PMOS amplifier noise, $S_{\text{pmos}}(f)$, the windowed chopping action, and the differential implementation, we estimate that the fundamental resolution of the TDC calculated in (6) will be degraded by approximately $9 + 8 - 3 = 14$ dB. This leads to a predicted TDC noise performance of 15.9 $\mu$K $\cdot$ $10^{14/20} = 80$ $\mu$K(rms) within a 5-Hz bandwidth, which implies an output spectral density for the TDC (scaled to units of Kelvin) of 80 $\mu\text{K}/\sqrt{5\ \text{Hz}} = 36$ $\mu\text{K}/\sqrt{\text{Hz}}$ at low frequencies as indicated in Fig. 15. These calculated estimates are reasonably close to the measured TDC noise performance presented later in this paper.

Given the above observations, it would seem beneficial to increase the averaging windows for $V_{\text{avg1}}[k]$ and $V_{\text{avg2}}[k]$ in order to lessen the SNR penalty of the zero-times of the chop waveform and to chop at a higher frequency in order to lessen the impact of $1/f$ noise in the PMOS amplifier. Unfortunately, there is a tradeoff between these two issues which is set by the transients occuring from the switched resistor measurement technique. Increasing the relative averaging windows for $V_{\text{avg1}}[k]$ and $V_{\text{avg2}}[k]$ within a given $T_{\text{chop}}$ period implies that such transients must occur over a smaller relative time. However, given a fixed transient time, this would imply that a slower chopping frequency is required which increases the impact of the PMOS $1/f$ noise. The choice of allowing the worse case transient time to occupy up to half of the $T_{\text{chop}}$ period provides a reasonable compromise in which a high chopping frequency is achieved while maintaining reasonable averaging windows for $V_{\text{avg1}}[k]$ and $V_{\text{avg2}}[k]$.

## V. MEASURED RESULTS

A photograph of the MEMS die attached and wire bonded to the 180-nm CMOS die is shown in Fig. 16. On the CMOS die, the analog portion of the TDC consumes 0.15 mm$^2$, the integer-$N$ PLL that produces the 480-MHz clock for the TDC consumes 0.03 mm$^2$, and the digital portion of the TDC (including the digital fifth order polynomial compensation and digital TDC filter) consumes 0.23 mm$^2$ (i.e., 37% of the overall digital route). Assuming a 3.3-V power supply, measured current consumption of the overall chip is 33 mA for a 48-MHz output clock (no load). Measured current consumption for the combined TDC and integer-$N$ PLL is 3.93 mA, of which 2.8 mA is estimated for the analog portion of the TDC and entire integer-$N$ PLL, and the remainder for digital blocks (including the fifth-order polynomial correction and lowpass filtering) and non-TDC circuits on the same supply domain. As for other key circuit blocks on the CMOS IC, the estimated current consumption of the fractional-$N$ synthesizer and output frequency divider is 16.6 mA based on SPICE-level simulations, of which 13.1 mA is estimated for the feedback and output frequency dividers due to differential, current-mode logic being employed for these high speed circuits [25], [26], and estimated current consumption of the MEMS sustaining circuit is 2 mA based on SPICE-level simulations.

In presenting the MEMS-based programmable oscillator performance, we first focus on TDC related performance demonstrating $<\ \pm 0.5$-ppm frequency stability and less than 5-ppb Allan Deviation at strides of 0.1, 1, and 10 s. The overall phase noise performance of the oscillator is then presented with demonstration of better than 1-ps (rms) integrated jitter.

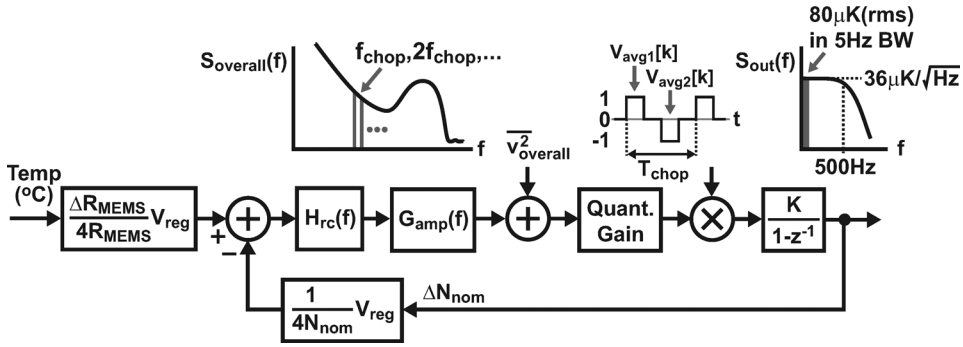


Fig. 15. System-level analysis of TDC noise.

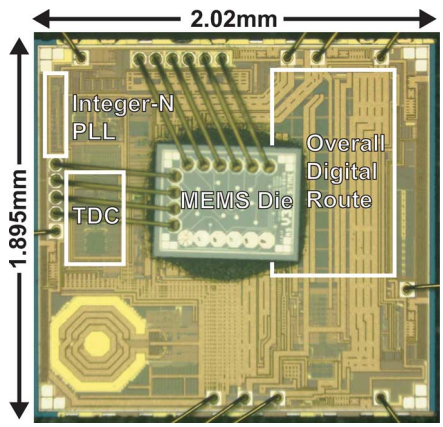


Fig. 16. Die photograph of MEMS die with resonator and thermistor wire-bonded to a 0.18-$\mu$m CMOS chip with supporting circuitry.

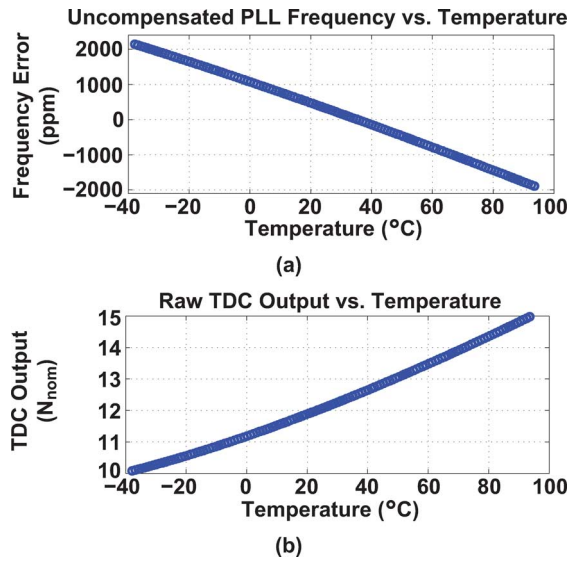


Fig. 17. Measured results for (a) uncompensated output frequency and (b) raw TDC output.

### *A. Frequency Stability, Allan Deviation, and Phase Noise at Lower Frequency Offsets*

Fig. 17 displays measured results for the uncompensated output frequency and raw TDC output of the device across a temperature range of $-40\,^{\circ}$C to $85\,^{\circ}$C. As expected, the uncompensated frequency varies approximately 4000 ppm across this temperature range and displays a slight amount of curvature. The raw output of the TDC also displays curvature, which, as will be shown later, leads to slightly degraded noise performance at low temperatures since the reduced TDC slope leads to a higher frequency compensation slope and therefore higher impact on frequency deviation as depicted in Fig. 2.

Fig. 18 displays measured results for the compensated output frequency for 101 devices based on individual 12-point temperature calibration as well as the Allan Deviation performance for 20 devices at room temperature. As the figure reveals, the compensated output frequency is stable to well within $\pm 0.5$ ppm, and the Allan Deviation is less than 5 ppb at room temperature. Such performance is competitive with recent work on temperature compensated crystal-based oscillators [27]. Note that 12-point temperature calibration was chosen for characterization purposes and does not correspond to the optimal or minimal number of temperature points required to obtain the reported frequency stability performance.

To better understand the impact of the TDC on the oscillator phase noise, Fig. 19 shows measured phase-noise plots for different configurations of the TDC output. In the figure, the lowest curve corresponds to the case where the TDC is disabled such that the phase noise is set by the 48-MHz MEMS sustaining circuit. Enabling the TDC output without filtering reveals that the TDC noise dominates the overall phase noise for offset frequencies below 10 kHz. Application of a 12-Hz bandwidth digital filter at the TDC output, which is the normal operating mode of the device, suppresses the impact of the TDC noise at higher offset frequencies such that the TDC only dominates the noise performance below 200 Hz.

Focusing directly on the noise performance of the TDC, Fig. 20 displays measured spectral density plots of its output scaled to degrees Celsius at three temperatures of $-40\,^{\circ}$C, $25\,^{\circ}$C, and $85\,^{\circ}$C. These plots reveal that the closed-loop TDC bandwidth is approximately 500 Hz and that the low-frequency spectral density is close to the calculated value of 36 $\mu\text{K}/\sqrt{\text{Hz}}$, as shown in Fig. 15. Integrating the measured noise spectral density within a 5-Hz bandwidth yields rms noise levels of 98 $\mu$K at $25\,^{\circ}$C, 97 $\mu$K at $85\,^{\circ}$C, and 167 $\mu$K at $-40\,^{\circ}$C. The slightly elevated noise at cold temperature is due to the reduced TDC slope at such temperatures as seen in Fig. 17(b).

Fig. 21 displays a comparison of the measured performance of the TDC with other state-of-the-art designs as made available in [28]. Assuming 5-Hz bandwidth and room temperature as the

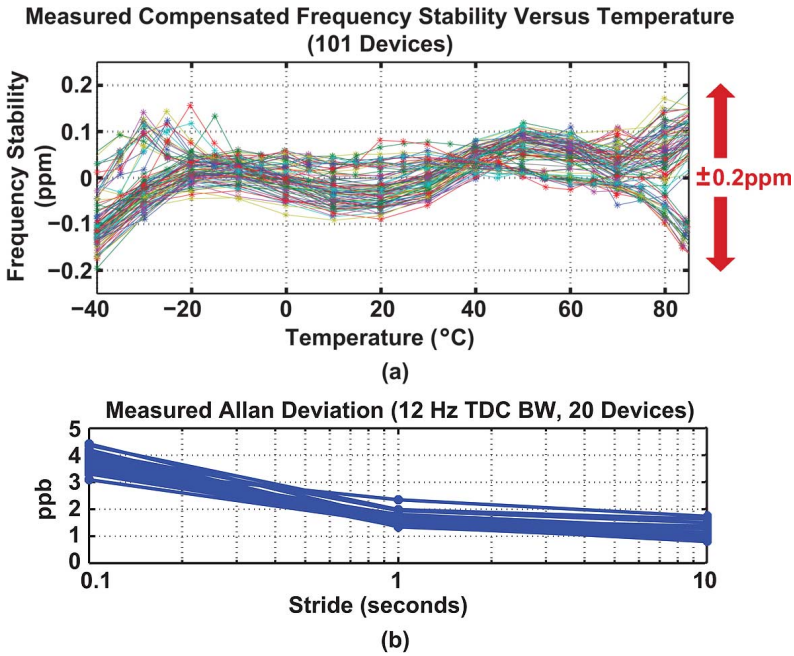


Fig. 18. Measured results for (a) compensated output frequency and (b) Allan Deviation at room temperature for strides of 0.1, 1, and 10 s.

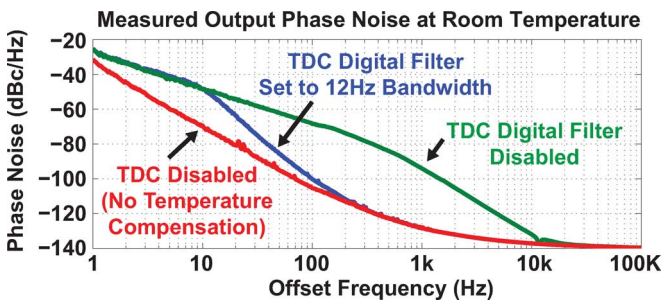


Fig. 19. Measured phase-noise plots with different amounts of TDC filtering as well as disengagement of the TDC.

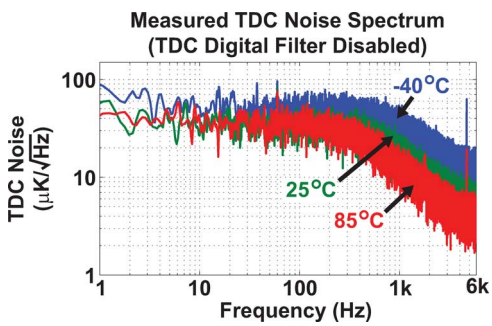


Fig. 20. Measured TDC noise spectrum at −40 °C, 25 °C, and 85 °C.

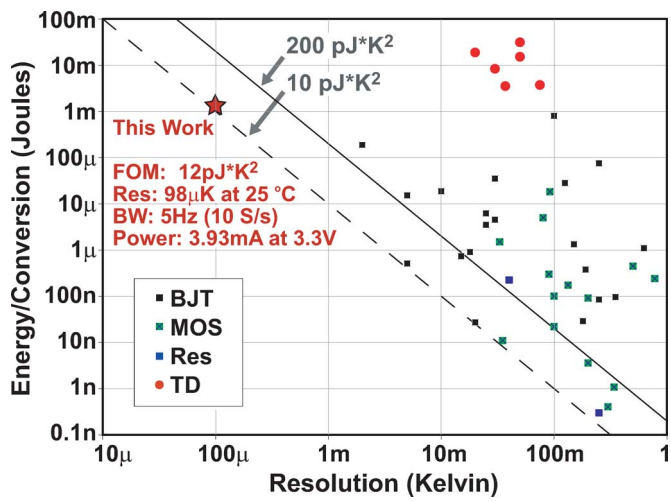


Fig. 21. Comparison of proposed TDC with other recent designs based on the "Smart Temperature Sensor Survey" by Makinwa [28].

nominal operating point, the proposed TDC obtains well over an order of magnitude better resolution than all of the other TDC designs in this survey. Further, the proposed TDC also achieves power efficiency of 12 pJ · K$^2$, which is on par with the most power efficient designs in the survey. One should note that the power calculation for the proposed TDC includes all analog and digital circuits (including fifth-order polynomial compensation and digital filtering) as well as the integer-$N$ PLL used to generate the 480-MHz reference clock.

### *B. PLL Design and Overall Phase Noise*

The overall phase-noise performance of the MEMS-based programmable oscillator is primarily influenced by the 48-MHz MEMS sustaining circuit, the TDC, and the fractional-$N$ PLL. Fig. 19 revealed the influence of the 48-MHz MEMS sustaining circuit and TDC, which impact phase noise at low frequency offsets. We now briefly discuss the fractional-$N$ PLL, in which the design goal is to ensure that its contribution to phase noise at lower frequency offsets is below that of the MEMS sustaining circuit and to achieve sufficiently low phase noise at higher frequency offsets such that the overall integrated phase noise is less than 1 ps.

Fig. 22 shows the key details of the fractional-$N$ frequency synthesizer [11], which uses a switched resistor loop filter [29] topology in combination with a native NMOS voltage regulator

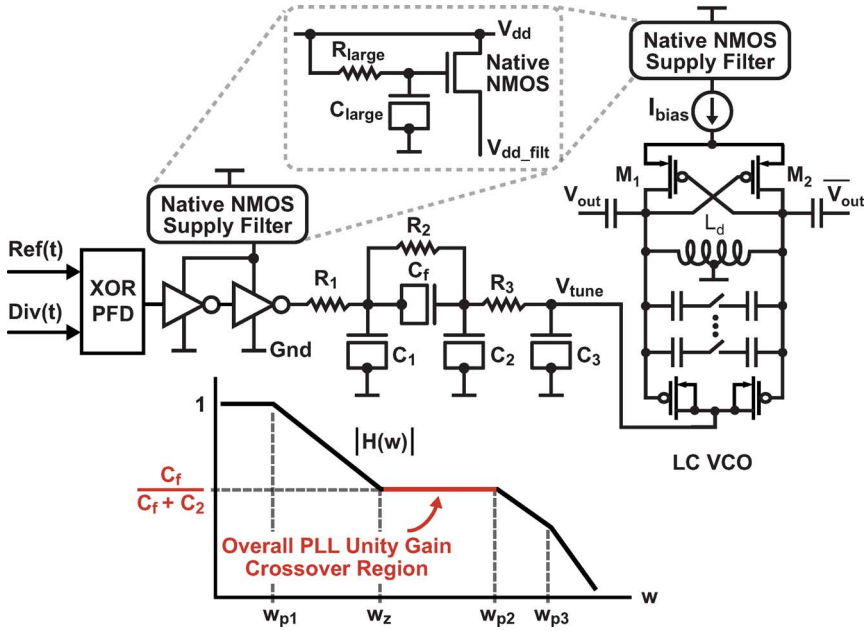


Fig. 22. Loop filter for fractional-$N$ synthesizer used within the MEMS-based programmable oscillator.

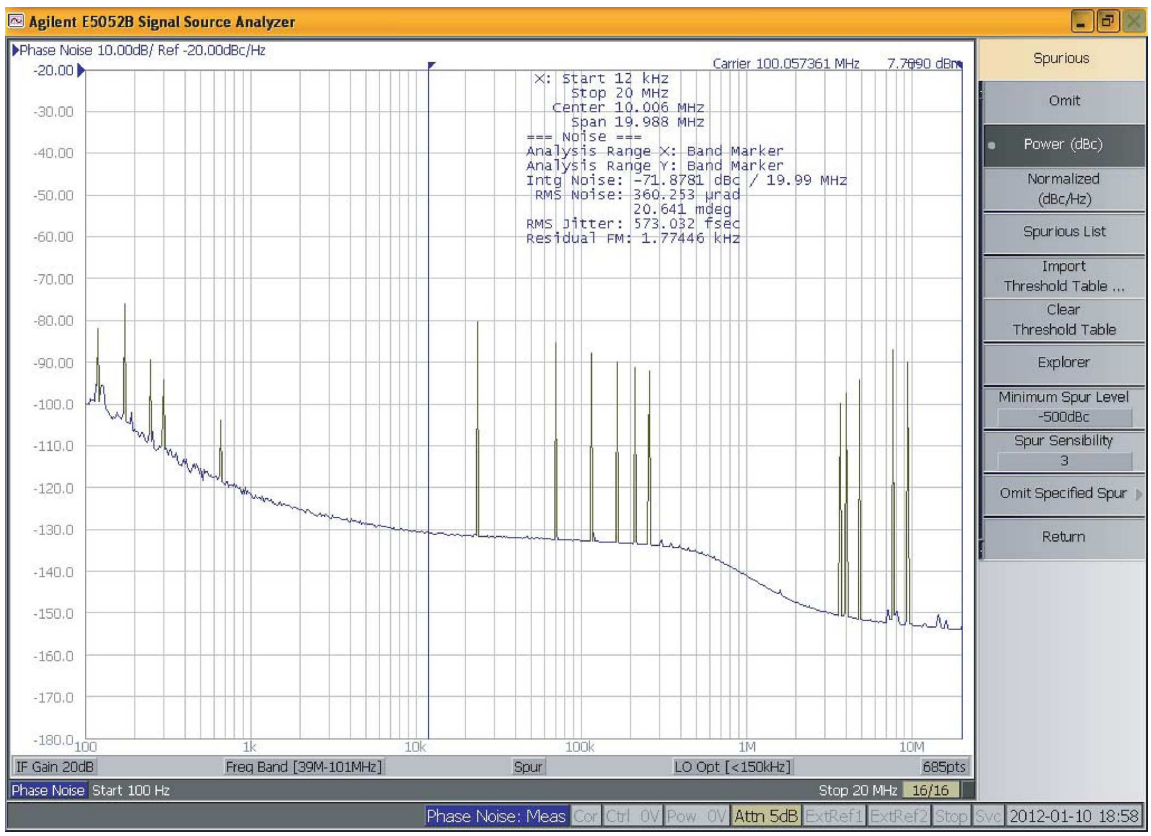


Fig. 23. Measured phase noise.

to achieve low noise at low frequency offsets. To explain, resistors have low $1/f$ noise relative to MOS devices, so that a switched resistor topology provides an easier path to suppressing such noise compared with a traditional charge pump PLL [11]. However, a low-noise voltage regulator is required to drive the resistors, and this is accomplished by the native NMOS voltage regulator shown in the figure. Of the total die area, the loop filter consumes 0.08 mm$^2$, the native NMOS RC filter consumes 0.085 mm$^2$, the LC-VCO consumes 0.4 mm$^2$, and the rest of the PLL consumes 0.065 mm$^2$.

The overall measured phase noise performance of the MEMS-based programmable oscillator is shown in Fig. 23. Integrated phase noise from 12 kHz to 20 MHz is 573 fs (rms) (including spurs), of which the Random Jitter (RJ) component

[30] is 475 fs (rms). As such, the proposed MEMS-based oscillator achieves not only $\pm 0.5$-ppm frequency stability, but also subpicosecond integrated jitter performance.

## VI. Conclusion

This paper presented a MEMS-based programmable oscillator with frequency stability $< \pm 0.5$ ppm from $-40\,^{\circ}$C to 85 °C, Allan Deviation $<$ 5 ppb at strides of 0.1, 1, and 10 s, and integrated phase noise (12 kHz to 20 MHz) of $<$ 1 ps (rms). The oscillator supports any output frequency in the range of 0.5–220 MHz through simple factory programming.

A key component to achieving high frequency stability and low Allan Deviation is an energy-efficient, thermistor-based TDC that achieves $<$ 100 $\mu$K (rms) resolution within a 5-Hz bandwidth at room temperature. Several circuit techniques were presented to enable this level of TDC performance. First, a high-resolution reference resistor was achieved through the combination of a switched-capacitor network and fractional-$N$ frequency division techniques. Second, a switched-resistor measurement technique was introduced to remove the need for a reference voltage and differential amplifier. This technique intrinsically provided correlated double-sampling functionality which enabled a pulsed bias technique to substantially reduce bias noise. Finally, a VCO-based quantizer was utilized to achieve a highly digital approach for digitization of the temperature signal.

In summary, the measured results of the presented MEMS-based programmable oscillator demonstrate similar performance to high end quartz-based clock references. Unlike quartz solutions, however, the MEMS-based approach is achieved with standard silicon processing which directly takes advantage of the large economy of scale of consumer semiconductor products. Also, rather than ceramic or metal packaging as required for quartz-based oscillators, inexpensive plastic packaging can be utilized since the MEMS resonator and thermistor are self-encapsulated at the wafer level. These advantages, along with the high level of programmability of the device, provide a compelling path forward to using MEMS-based oscillator technology for even the most demanding clocking needs of the electronic industry.

## Acknowledgment

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**Michael H. Perrott** (SM'09) received the B.S. degree in electrical engineering from New Mexico State University, Las Cruces, in 1988, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, in 1992 and 1997, respectively.

From 1997 to 1998, he was with Hewlett-Packard Laboratories, Palo Alto, CA, where he was involved with high-speed circuit techniques for Sigma-Delta synthesizers. In 1999, he was a Visiting Assistant Professor with the Hong Kong University of Science and Technology. From 1999 to 2001, he was with Silicon Laboratories, Austin, TX, where he developed circuit and signal processing techniques to achieve high-performance clock-and-data recovery circuits. He was an Assistant and then Associate Professor of electrical engineering and computer science with the Massachusetts Institute of Technology, Cambridge, from 2001 to 2008. He was with SiTime Corporation, Sunnyvale, CA, from 2008 to 2010, where he developed key technology for MEMS-based oscillators. He is currently a Professor with the Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates, where he is focusing on low-power mixed-signal circuits for health and fitness and other applications.

**James C. Salvia** received the B.S. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, in 2005, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 2008 and 2010, respectively. His Ph.D. dissertation, "Micro-oven based temperature compensation systems for MEMS oscillators," focused on circuit and system development for the stabilization and temperature control of microresonator-based oscillators.

As a Research Assistant with Carnegie Mellon University, he developed on-chip magnetic inductors for high-frequency applications. He is currently developing CMOS circuitry for high-performance MEMS timing references with SiTime Corporation, Sunnyvale, CA.

Dr. Salvia is a National Science Foundation Graduate Fellow and a National Defense Science and Engineering Graduate Fellow.

**Fred S. Lee** received the B.S./M.Eng. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, in 2002 and 2007, respectively.

He is currently with Fairchild Semiconductor, San Jose, CA, where he leads the development of multi-DOF MEMs-based sensors. From 2008 to 2011, he was with SiTime Corporation, Sunnyvale, CA, designing MEMs-based fractional-N PLLs, MEMs-based temperature sensors, and RF/mixed-signal circuits. From 2007 to 2008, he was with Rambus Inc., Los Altos, CA, working on multi-GHz wireline and 60-GHz wireless transceivers.

Dr. Lee was a corecipient of the DAC/ISSCC Student Design Contest Award in 2004 and the ISSCC Jack Kilby Best Student Paper Award in 2007.

**Aaron Partridge** received the B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1996, 1999, and 2003, respectively.

He is presently Founder and Chief Scientist with SiTime Corporation, Sunnyvale, CA. From 2001 through 2004, he was a Project Manager with the Robert Bosch Research and Technology Center (RTC), Palo Alto, CA, where he coordinated MEMS resonator research. In 1987, he cofounded Atomis, Inc., a manufacturer of STM, AFM, and ballistic emission electron microscopes, where he was Chief Scientist through 1991 when Atomis was sold to Surface Interface Inc. He has authored and coauthored over 30 scientific papers and 60 patents.

Dr. Partridge serves on the IEEE International Solid-State Circuits Conference IMMD Subcommittee and is the Editorial Chair of the IEEE International Frequency Control Symposium.

**Shouvik Mukherjee** received the B.S.E.E. degree from Nagarjuna University, Nagarjuna Nagar, India, in 1991, and the M.S.E.E. degree from Lamar University, Beaumont, TX, in 1993.

Since then, he has held logic design and CAD positions with various companies such as Synergy Semiconductor, Cadence Design Systems, Centillium Communications, and Actel Corporation. He is currently a Logic Designer with SiTime Corporation, Sunnyvale, CA.

**Carl Arft** received the B.S. degree in electrical engineering from Michigan Tech University, Houghton, and the M.S. and Ph.D. degrees in Electrical Engineering from University of California, Davis, all in electrical engineering.

He has been active in the MEMS field for over 15 years. Previously, he was involved with several optical MEMS start-up companies, including C Speed Corporation and Newport Opticom. From 2004 to 2006, he served as a Faculty Fellow with the University of California, Davis. Currently, he is Director of Test Development Engineering with SiTime Corporation, Sunnyvale, CA, the world's leading supplier of MEMS-based timing references.

**Jintae Kim** received the B.S. degree from Seoul National University, Seoul, Korea, in 1997, and the M.S. and Ph.D. degrees from University of California, Los Angeles, CA, in 2004 and 2008, respectively, all in electrical engineering.

From 1997 to 2001, he was with Xeline, Seoul, Korea, designing baseband ICs for high-speed power-line communication. During the summers of 2003 and 2004, he was with Barcelona Design, Sunnyvale, CA, developing CAD algorithms for analog circuit optimization. From 2008 to 2011, he was with Agilent Technologies, Santa Clara, CA, working on ultra high-speed interleaved A/D converter designs. From 2011 to 2012, he was with SiTime Corporation, Sunnyvale, CA, where he worked on high-performance frequency synthesizers and low-power temperature sensor designs. He is currently an Assistant Professor with Konkuk University, Seoul, where he is focusing on low-power mixed-signal IC designs for communi Ocation and sensor applications.

Dr. Kim was a recipient of the IEEE Solid-State Circuits Predoctoral Fellowship in 2007.

**Niveditha Arumugam** received the B.S. degree from the College of Engineering Guindy, Chennai, India, in 2006, and the M.S. degree from Stanford University, Stanford, CA, in 2008, both in mechanical engineering.

Between 2007 and 2008, she was a Research Assistant with the Stanford Microsystems Group, focusing on microfabricated devices for small-scale biomechanics. Since August 2008, she has been with SiTime Corporation, Sunnyvale, CA, characterizing MEMS resonators, mixed-signal circuits, and MEMS-based oscillators.

**Pavan Gupta** received the B.S. degree from the University of California, Los Angeles, in 1997, and the M.S. degree from Stanford University, Stanford, CA, in 2000, both in mechanical engineering.

He was with IBM as a Test and Mechanical Engineer developing precision mechanisms for hard-disk-drive test equipment until 1999. From 2000 to 2003, he was with Cspeed Corporation, developing packaging and optics technologies for a novel 3-D MEMS-based optical cross connect. From 2003 to 2005, while with Formfactor, he managed several teams responsible for process and manufacturing engineering of advanced MEMS-based probe cards for massively parallel semiconductor wafer probing. Since 2005, he has been with SiTime Corporation, Sunnyvale, CA, directing the packaging and characterization of SiTime's MEMS-based oscillators.

**Sassan Tabatabaei** received the Ph.D. in electrical engineering from the University of British Columbia, Vancouver, BC, Canada, in 2000.

He is currently Director of Strategic Applications with SiTime Corporation, Sunnyvale, CA. Prior to this, he held executive and technical management positions with a number of companies. His technical interests include signal integrity, timing, jitter, clocking analysis, instrumentation, test, and design. He holds several U.S. patents in these areas.

**Sudhakar Pamarti** received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, in 1995, and the M.S. the Ph.D. degrees in electrical engineering from the University of California at San Diego, La Jolla, in 1999 and 2003, respectively.

He is an Associate Professor of electrical engineering with the University of California, Los Angeles. Prior to this, he was with Rambus Inc. from 2003 to 2005 and Hughes Software Systems from 1995 to 1997, developing high-speed I/O circuits and embedded software and firmware for a wireless-in-local-loop communication system, respectively.

Dr. Pamarti was a recipient of the National Science Foundation CAREER Award for developing digital signal conditioning techniques to improve analog, mixed-signal, and radio frequency integrated circuits.

**Haechang Lee** received the B.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1998 and 2007, respectively.

As the Director of Circuit Design with SiTime Corporation, Sunnyvale, CA, he oversees all IC development including fractional synthesizers, temperature sensors, ADCs, and MEMS interface circuits. Before joining SiTime, he held positions with Rambus Inc. and Arda Technologies, developing high-speed and low-power transceivers for backplane, chip-to-chip processor bus, and memory interface applications. He has authored and coauthored more than 20 technical papers.

Dr. Lee is a member of Phi Beta Kappa and Tau Beta Pi.

**Fari (Fariborz) Assaderaghi** received his B.S. degree in Electrical Engineering from SDSU, graduating Summa Cum Laude and University Valedictorian in 1989. He received his M.S. and Ph.D. degrees in Electrical Engineering from UC Berkeley in 1992 and 1994, respectively.

After graduation, Dr. Assaderaghi joined HP Labs. From 1995 to 2001 he was with IBM TJ Watson Research Center where he co-developed the first commercial version of CMOS SOI for VLSI. The technology became the workhorse for IBM's microprocessors and was used in Apple's processors, as well as Sony Playstation-3 Cell Processor. From 2001 to 2003, he was the technology director for Silicon Wave Inc., a San Diego-based company developing Bluetooth products. From 2003 to 2008, he was with Rambus (Los Altos, CA), as senior director of engineering. His groups were responsible for developing high speed data communication circuits. From 2008 to 2012, he was with SiTime (Sunnyvale, CA), a developer of MEMS-based timing products. As Senior VP of Engineering and Operations, he was responsible for development and manufacturing of all SiTime's products. During his tenure, he helped grow the company's shipments from less than 1 million units/year to over 50 million units/year. In June 2012, he joined InvenSense, a provider of MEMS-based products as VP of Advanced Technology Development. Dr. Assaderaghi has contributed to more than 80 technical papers, and holds 50 patents.