A Low Area, Switched-Resistor Based Fractional-N Synthesizer Applied to a MEMS-Based Programmable Oscillator

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***Abstract*—MEMS-based oscillators have recently become a topic of interest as integrated alternatives are sought for quartz-based frequency references. When seeking a programmable solution, a key component of such systems is a low power, low area fractional-N synthesizer, which also provides a convenient path for compensating changes in the MEMS resonant frequency with temperature and process. We present several techniques enabling efficient implementation of this synthesizer, including a switched-resistor loop filter topology that avoids a charge pump and boosts effective resistance to save area, a high gain phase detector that lowers the impact of loop filter noise, and a switched capacitor frequency detector that provides initial frequency acquisition. The entire synthesizer with *LC* VCO occupies less than 0.36 sq. mm in 0.18 μm CMOS. Chip power consumption is 3.7 mA at 3.3 V supply (20 MHz output, no load).**

***Index Terms*—MEMS, fractional-N synthesizer, reference frequency, phase-locked loop (PLL), loop filter, high gain phase detector, switched resistor, switched capacitor, frequency acquisition, frequency detection, phase detection, oscillator, temperature stable.**

I. Introduction

RECENTLY there has been much interest in seeking more integrated alternatives to crystal resonators for the clocking needs of the electronics industry [2]–[8]. In this paper, we consider a MEMS-based programmable oscillator, shown in block diagram form in Fig. 1, in which a MEMS resonator is wire bonded to a CMOS die that contains an oscillator sustaining circuit, temperature sensor, fractional-N synthesizer, and various digital blocks. The output of the sustaining circuit provides a 5 MHz reference frequency to the fractional-N synthesizer, which outputs a higher frequency that can be digitally adjusted with sub-ppm resolution over a $>20\%$ tuning range. By then sending the fractional-N synthesizer output into a programmable frequency divider (i.e., divide-by-M circuit), any frequency in the range of 1 to 110 MHz can be achieved by proper combination of the fractional-N synthesizer and programmable divider settings.

As shown in Fig. 1, the sub-ppm resolution provided by the fractional-N synthesizer carries the additional benefit of allowing straightforward compensation for frequency deviation of the MEMS resonant frequency due to process and temperature variations. To do so, a temperature sensor on the CMOS die is utilized in combination with digital logic that performs polynomial multiplication of the digitized temperature value in order to compensate for curvature in the MEMS frequency variation across temperature. As we will see later in this paper, this approach allows better than ± 30 ppm accuracy to be achieved across a temperature range of -40 to 85 degrees C.

As observed from the above discussion, the fractional-N frequency synthesizer is a key enabling technology for achieving an efficient implementation of the MEMS programmable oscillator. In this paper, we focus on achieving a low area, low design complexity, and low power fractional-N synthesizer structure for this application space. In particular, we introduce a switched resistor loop filter topology which provides low area and reduced analog complexity compared to more traditional charge pump based designs, a high gain phase detector which lowers the impact of loop filter noise, and a switched capacitor frequency acquisition circuit that requires little area and power and has no impact on the steady state noise performance of the synthesizer.

Section II provides a short background discussion on traditional synthesizers based on a charge pump phase-locked loop (PLL) structure. We then introduce the proposed switched resistor loop filter topology in Section III and describe its key attributes. Section IV provides noise analysis of the proposed structure, and points out the advantages offered by increasing the phase detector gain. Section V introduces a high gain phase detector structure, as well as a switched capacitor frequency detection circuit to enable fast and reliable frequency acquisition. Section VI discusses the issue of nonlinearity in the switched resistor loop filter, and Section VII provides details of the prototype and measured results. Finally, Section VIII concludes the paper.

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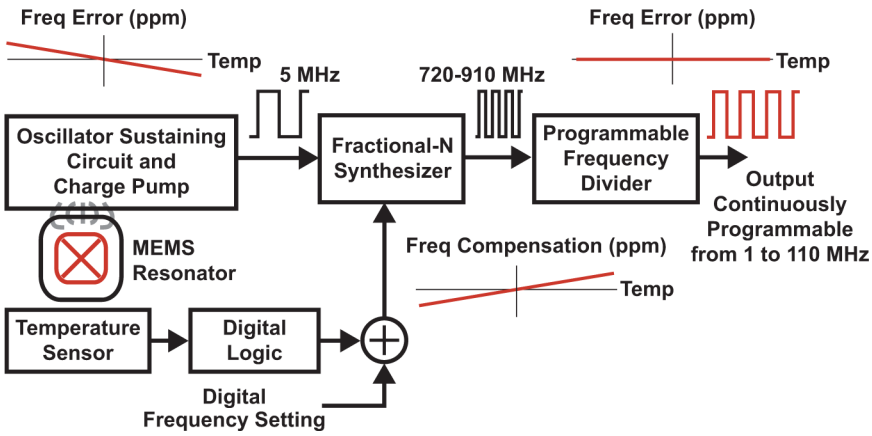

Fig. 1. Programmable MEMS-based oscillator circuit consisting of a MEMS die wire-bonded to a CMOS die consisting of a sustaining circuit, fractional-N synthesizer, programmable frequency divider, temperature sensor, and temperature compensation circuits.

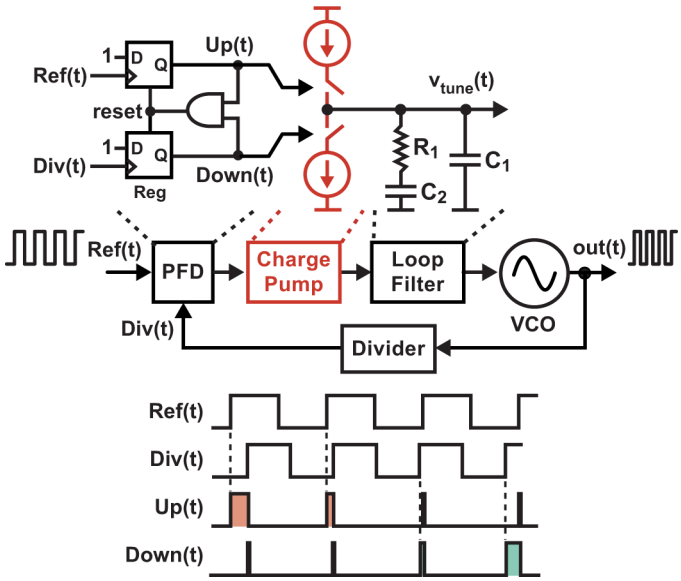

Fig. 2. Frequency synthesizer based on a charge pump PLL structure.

II. Background

Fig. 2 displays a traditional frequency synthesizer based on a charge pump PLL topology [9]. A voltage-controlled oscillator (VCO) outputs a variable frequency that is tuned according to an input voltage, $V_{\rm tune}(t)$. Feedback is used to lock the VCO output frequency to a multiple of the reference frequency through the use of a frequency divider, phase detector (PD), and charge pump based loop filter. The phase detector is commonly implemented as the tristate design shown in the figure, which intrinsically provides frequency detection capability. The phase detector produces *Up* and *Down* pulses whose pulsewidth varies with the phase difference between the reference frequency, *Ref*, and divider output, *Div*. The charge pump converts the *Up* and *Down* PD signals into current pulses which are then filtered by the *RC* network of the loop filter to form the $V_{\rm tune}(t)$ voltage.

The charge pump PLL structure is prevalent as the PLL topology of choice across a wide range of applications. As seen in Fig. 2, it offers a seemingly simple implementation, can achieve low power operation, and can be applied to both integer-N and fractional-N frequency synthesizers. However, this seemingly simple design often turns out to be quite design intensive [10] and typically leads to a large area loop filter implementation. Indeed, considerable design effort is often spent on addressing analog considerations such as avoiding deadzone behavior in the PD, minimizing current mismatch and maximizing output resistance for the *Up* and *Down* currents across the full range of the charge pump, and providing a well controlled, and often low noise, bias current for the charge pump. While such analog issues can be dealt with by experienced and skilled analog designers, an intriguing approach is to look for a different PLL topology that is simpler to design while also achieving a low power and low area implementation with adequate phase noise performance.

III. Proposed Switched Resistor Loop Filter

In this paper, we consider eliminating the charge pump, and indeed all active circuitry, from the loop filter in order to achieve a frequency synthesizer topology with reduced analog design effort [11]. Fig. 3 displays the proposed switched resistor loop filter topology, which consists of a passive network driven by

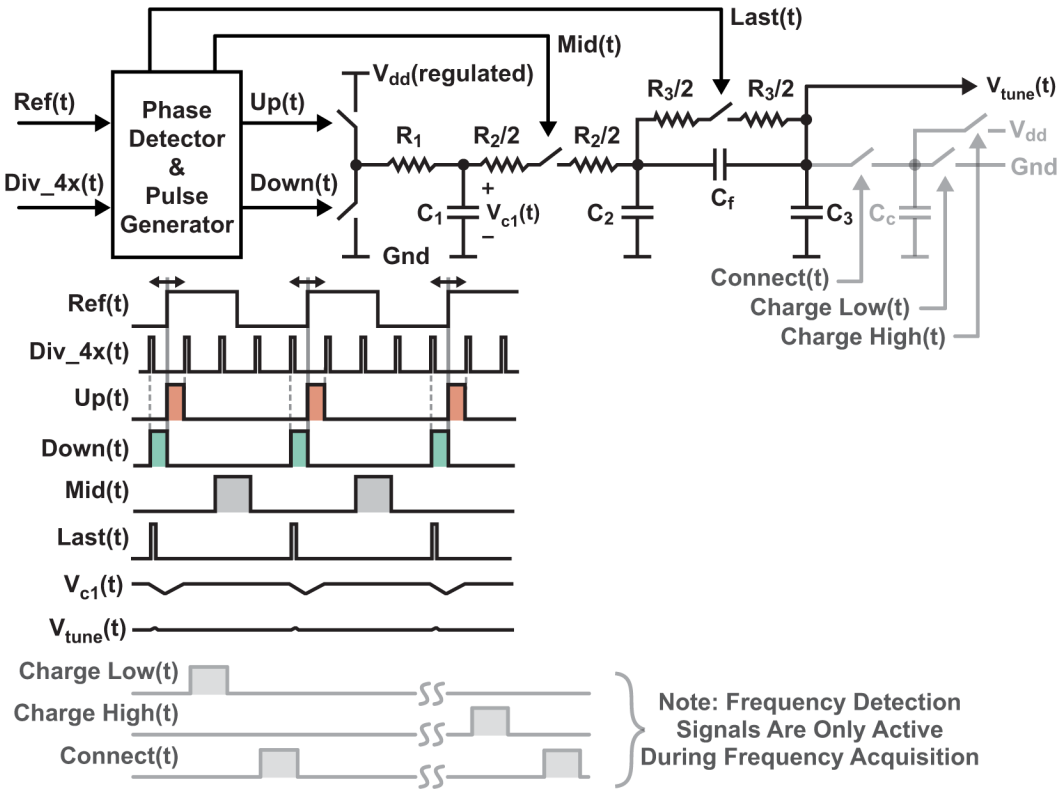

Fig. 3. Proposed switched resistor loop filter. Note that the R_3 pulsing frequency can also be set lower than the reference frequency, and is implemented at 1/4 the reference frequency in the prototype.

CMOS switches [12], [13], and has similarities to the voltage-mode exponential CP-PFD recently introduced in [14]. In contrast to the Up/Sample/Reset approach in [14], here *Up* and *Down* pulses are generated by a PD, and are fed into switches that connect to an on-chip regulated supply voltage or ground before feeding into the passive loop filter. Frequency detection is performed during initial startup of the PLL through the use of a simple switched capacitor network shown in the figure. Once the PLL is locked, this switched capacitor network is automatically shut off so that it has no impact on the phase noise performance of the synthesizer during steady state operation.

As shown in Fig. 3, the phase detector can also be used to create multi-phase pulse signals, as will be explained later in this paper. We can leverage these pulse signals to switch on the resistors within the loop filter in a non-overlapping manner as shown in the figure. By doing so, the reference spur performance of the PLL is improved by effectively blocking the ripple that occurs on capacitor $C_1, V_{c1}(t)$, due to the *Up* and *Down* pulsing from reaching the VCO tuning voltage, $V_{\rm tune}(t)$. A similar technique has been applied to PLLs with the use of sample and hold circuits [15], [16].

Pulsing the resistors also provides a simple method of boosting time constants within the passive loop filter, which helps to enable a low area loop filter. Note that this technique has also been applied to active filters [17]. Fig. 4 illustrates that pulsing a resistor acts to increase its effective resistance since the average current through the resistor will be reduced according to the ratio of the pulse on-time, $T_{\rm on}$, to its period, T. In practice, charge that has been stored on parasitic capacitance of the switch and poly resistor will drain through the resistor even when the switch is off, which increases the average current through the resistor and therefore lowers its effective resistance. However, detailed SPICE simulations and prototype measurements reveal that the effective resistance can easily be increased by over an order of magnitude above the poly resistance value through proper choice of $T/T_{\rm on}$.

Note that the *RC* network for the proposed switched resistor loop filter does not correspond to that of a traditional charge pump PLL, but conventional Bode plot analysis can be applied to achieve a desired PLL bandwidth and phase margin as discussed later in this paper. As such, design of the switched resistor loop filter consists of choosing resistor and capacitor values to achieve the desired loop filter transfer function, and then choosing switch sizes with turn on resistances that are reasonably less in value than the resistors that they switch. As an example, in the prototype considered here, the switches were designed to have no more than 10% of the resistance of their corresponding poly resistor, as determined by SPICE level simulation. In addition, the effective amount of resistor multiplication achieved through resistor pulsing should be examined with SPICE level simulation. Overall, this is a much simpler procedure than designing an active circuit such as a charge pump and its accompanying bias current network.

One might argue that a switched resistor loop filter carries the disadvantage of requiring a regulated supply in order to isolate the switched resistor loop filter from supply variation and noise. However, regulators have now become common on modern ICs, and are generally required for other portions of the PLL such as

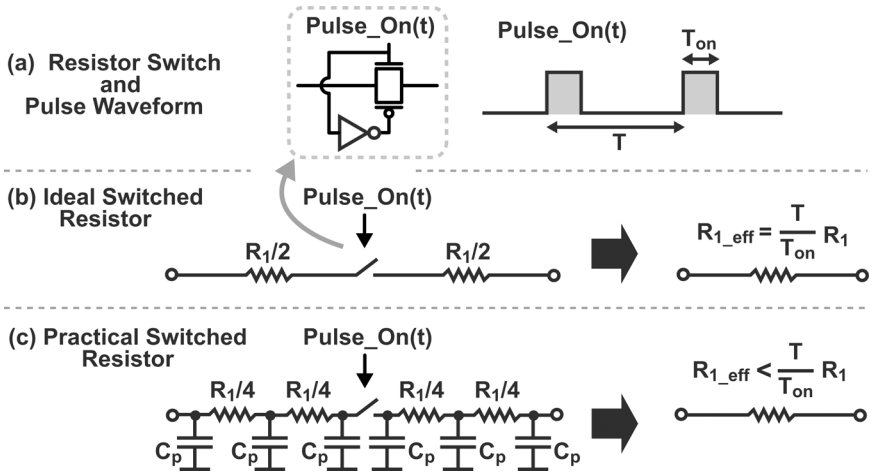

Fig. 4. Implementation of switched resistor using CMOS devices and poly resistors, along with impact of pulsed switching and parasitic capacitance on the effective resistance.

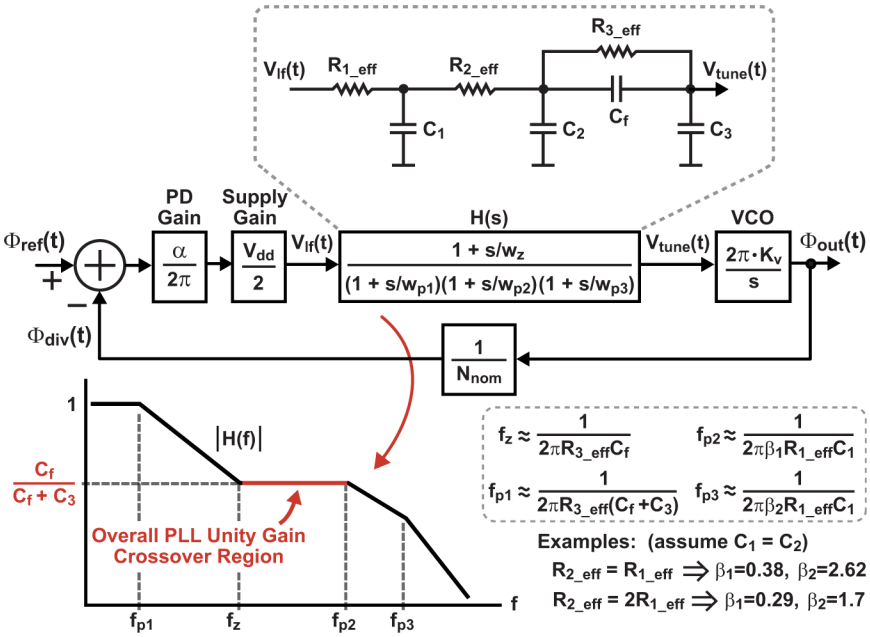

Fig. 5. Transfer function analysis of a switched resistor PLL in which the Bode plot of the loop filter, $H(f)$, is considered within the context of the overall PLL block diagram. Note that the values of β_1 and β_2 are calculated using the Quadratic formula by ignoring the influence of R_{3_eff}, C_f, and C_3 on poles f_{p2} and f_{p3}.

its VCO. As such, one can view the switched resistor approach as a means of trading a custom design effort on a charge pump for a more commonly available voltage regulator block.

IV. Loop Filter Design

To better understand design considerations for a switched resistor loop filter, this section explores its impact on the dynamics and noise performance of the overall PLL in which it is employed. We begin by presenting a simple dynamic model of a switched resistor PLL and associated transfer function analysis. We then examine the impact of pulsing on the resistor noise, and use this analysis to achieve a simple noise model of the switched resistor loop filter. Finally, we quantify the impact of the loop filter noise on the output phase noise of the PLL, and highlight the value of a high gain phase detector in lowering the impact of that noise.

A. Dynamic Analysis

To arrive at a dynamic model for the switched resistor PLL, we combine Figs. 3 and 4 to obtain the block diagram shown in Fig. 5. In this model, we assume steady-state operation of the PLL so that frequency detection is inactive and capacitor C_c can be ignored. Also, as further elaborated in the noise discussion to follow, it is assumed that the on-time, T_{on}, of the switched resistors are significantly shorter than the corresponding *RC* time constant of their settling characteristic. Finally, note that the phase detector model, which includes PD gain $\alpha/(2\pi)$ and supply gain $V_{dd}/2$, will be discussed in more detail in the following section.

Inspection of Fig. 5 reveals that the switched resistor loop filter has a similar transfer function to that of the commonly used lead-lag filter, but is constrained to have a DC gain of one. As with other PLL topologies using a lead-lag filter, the open

loop gain of the PLL should be chosen such that its unity gain crossover frequency is higher than the loop filter zero, f_z, and lower than the loop filter poles, f_{p2} and f_{p3}. Since the open loop unity gain crossover frequency is roughly the same as the closed loop bandwidth of the PLL, $f_{\rm bw}$, we have

$$\frac{\alpha}{2\pi}\frac{V_{dd}}{2}\frac{C_f}{C_f+C_3}\frac{2\pi K_v}{2\pi f_{\rm bw}}\frac{1}{N_{\rm nom}}\approx 1$$

$$\Rightarrow f_{\rm bw}\approx \frac{\alpha}{2\pi}\frac{V_{dd}}{2}\frac{C_f}{C_f+C_3}\frac{K_v}{N_{\rm nom}} \quad (1)$$

where K_v is the VCO gain in Hz/V, V_{dd} is the regulated supply voltage feeding the switched resistor network, $\alpha/2\pi$ is the PD gain, and $N_{\rm nom}$ is the nominal divide value. Since the loop filter only provides attenuation through the factor $C_f/(C_f+C_3)$, (1) reveals that a switched resistor loop filter must satisfy

$$\frac{\alpha}{2\pi}\frac{V_{dd}}{2}\frac{K_v}{N_{\rm nom}} > f_{\rm bw}$$

to be viable. Notice that a high phase detector gain, $\alpha/2\pi$ and reasonably high K_v values are desirable to help meet this constraint, and higher phase detector gain allows more flexibility in the choice of K_v.

When focusing on the issue of loop filter area, one should note that $R_{3\_\rm eff}$ will generally be quite large in order to create a sufficiently low zero, f_z, without requiring a large feedforward capacitor, C_f. As an example, in the prototype, the desired value of f_z is around 4 kHz given a PLL bandwidth of around 30 kHz. Assuming $C_f = 2.3$ pF, the value of $R_{3\_\rm eff}$ must be 16 MΩ in order to achieve this zero! By using resistor pulsing, a poly resistor of only 500 kΩ is used to achieve this 16 MΩ resistor. Note that the desired values of $R_{1\_\rm eff}$ and $R_{2\_\rm eff}$ will generally be much smaller, assuming C_3 is of the same order in value as C_1 and C_2.

When implementing such large effective resistance for $R_{3\_\rm eff}$, one must take care to avoid significant current leakage at the varactor input of the VCO. Any such leakage will cause a sawtooth voltage waveform to occur at the VCO input (i.e., the current leakage will cause a voltage ramp that is reset when R_3 is switched on), which will induce a spurious tone (and accompanying harmonics) at the PLL output with fundamental frequency corresponding to the rate at which R_3 is switched. In the prototype, R_3 was switched on at a rate of 1/4 the MEMS reference frequency of 5 MHz. As will be seen in Section VII, measured results of the prototype reveal that spurs due to this issue are insignificant in magnitude. However, we will discuss additional implications of the large value of $R_{3\_\rm eff}$ in the sections to follow.

B. Noise Analysis

As we will soon see, noise is the key issue in setting the area of a switched resistor loop filter, just as it is for the more traditional charge pump PLL. While many are familiar with switches being used with sample and hold circuits, the noise of a switched resistor within a PLL loop filter is not a familiar topic. As such, we will now perform analysis of the simplified switched resistor circuit shown in Fig. 6, and use our results to develop a noise model of the switched resistor loop filter as well as highlight the differences between it and a more traditional sample and hold

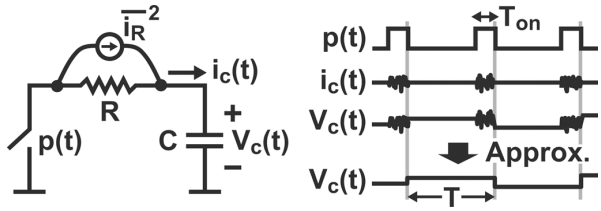

Fig. 6. Impact of resistor current noise on simple switched resistor network.

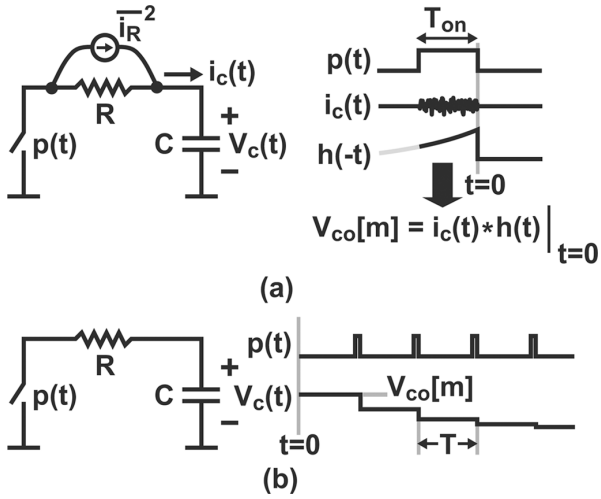

Fig. 7. Noise modeling for simple switched resistor network. (a) Impact of one noise pulse. (b) Impulse response due to one noise pulse.

circuit. We will see that our analysis agrees with that performed for active switched resistor filters in [17].

We begin with two simplifying assumptions. The first simplification is that we will ignore the influence of distributed parasitic capacitance in the switched resistor element. The second simplification is indicated in Fig. 6, where we see that the noise of the resistor only influences the capacitor during the time that the resistor is pulsed on, $T_{\rm on}$. Once the resistor switch is turned off, the capacitor voltage remains constant. Assuming that $T_{\rm on}$ is much shorter than the pulse period, T, we can simplify our analysis by ignoring the $T_{\rm on}$ transition region and instead assume that the capacitor voltage instantaneously changes its value in time increments of T.

Fig. 7 illustrates the analysis method we will use to quantify the impact of the pulsed resistor noise. The first step, shown in part (a) of the figure, is to compute the immediate impact of one pulse of resistor noise on the capacitor voltage. The second step, shown in part (b) of the figure, is to compute the resulting transient response (i.e., impulse response) on the capacitor voltage caused by the noise pulse. Upon completion of these steps, the noise spectral density of the capacitor voltage is then computed.

Proceeding with step 1 of our analysis, Fig. 7(a) indicates that the capacitor voltage is influenced by the pulsed noise through a convolution operation with the impulse response of the *RC* network to a current impulse, $h(t)$, where

$$h(t)=\frac{1}{C}e^{-t/RC} \quad \text{for } t\geq 0, \quad 0 \text{ otherwise}$$

Since our later analysis will only concern itself with the voltage value that the capacitor holds after the noise pulse has ended,

we only need to compute the convolution operation at the time which determines the final holding value. As indicated in the figure, this amounts to scaling the noise pulse waveform by $h(-t)$ (i.e., the time reversed impulse response of the *RC* network). Assuming independence of resistor noise at different sample times, we compute the variance of the capacitor holding voltage as

$$\begin{aligned}\mathrm{Var}(V_{co}[m]) &= \int_{-T_{\mathrm{on}}}^{0} \overline{i_R}^2 h^2(-t)dt \\ &= \int_{-T_{\mathrm{on}}}^{0} \frac{2kT_K}{R}\left(\frac{1}{C}e^{t/(RC)}\right)^2 dt \\ &= \frac{kT_K}{C}\left(1-e^{-2T_{\mathrm{on}}/(RC)}\right) \end{aligned} \tag{2}$$

where k is Boltzmann's constant and T_K is temperature in degrees Kelvin. Note that we have modeled current noise of the resistor as $\overline{i_R}^2 = 2kT_K/R$ rather than $4kT_K/R$ since our variance calculations assume double-sided rather than single-sided spectral densities.

An interesting observation follows from (2) by considering two cases of the *RC* time constant of the impulse response relative to T_{on}:

$$\mathrm{Var}(V_{co}[m]) \approx \begin{cases} \frac{kT_K}{C} & RC \ll T_{\mathrm{on}} \\ \frac{kT_K}{C}\frac{2T_{\mathrm{on}}}{RC} & RC \gg T_{\mathrm{on}} \end{cases} \tag{3}$$

As revealed by (3), the variance of the capacitor holding value corresponds to the familiar expression of kT_K/C in the case where the *RC* constant is much smaller than T_{on}. In such case, the resistance value itself becomes unimportant and only the capacitor value matters. However, if the *RC* time constant is much larger than T_{on}, then the resistor value does have influence. For a switched resistor loop filter, it is this second case that applies assuming that resistor pulsing is performed to boost the effective resistance value.

Another important observation related to (2) is that it corresponds to a discrete-time process as we consider the impact of a sequence of noise pulses. Since we can again assume independence of resistor noise at different sample times, we calculate the autocorrelation and then spectral density of this sequence [18] as

$$\begin{aligned} &E(V_{co}[m]V_{co}[n]) \\ &\quad = \begin{cases} \mathrm{Var}(V_{co}[m]) & n = m \\ 0 & n \neq m \end{cases} \\ &\Rightarrow S_{V_{co}}(e^{j2\pi fT}) \\ &\quad = \mathrm{Var}(V_{co}[m]) \end{aligned} \tag{4}$$

Therefore, (4) reveals that the (double-sided) spectral density of the discrete-time sequence $V_{co}[m]$ corresponds to the variance of this sequence as calculated in (2).

We now turn our attention to part (b) of Fig. 7 in which we compute the dynamic response of the capacitor holding value to *one* noise pulse at time index m. It is well known that the first order *RC* network considered here has an impulse response with exponential decay during the time that the resistor is turned on. Since we approximate the capacitor voltage as changing value only at time increments of T, we have

$$V_c(t)|_m = V_{co}[m]\sum_{n=0}^{\infty} e^{-T_{\mathrm{on}}n/(RC)}\mathrm{rect}(t-nT,T) \tag{5}$$

where

$$\mathrm{rect}\,(t,T) = 1 \quad \text{for} \quad 0 \le t \le T,\ 0\ \text{otherwise} \tag{6}$$

Inspection of (5) at time index $n = 0$ and noise pulse m indicates a capacitor holding value of $V_{co}[m]$, which matches our previous analysis involving the immediate impact of one noise pulse.

If we now consider (5) across all values of m, we see that the discrete-time process $V_{co}[m]$ is convolved with an impulse response that has both discrete and continuous-time components. The corresponding noise spectral density of the capacitor voltage is calculated as

$$\begin{aligned} S_{V_c}(f) &= \frac{1}{T}|\mathrm{sinc}\,(fT)|^2 \\ &\quad \times \left|\frac{1}{1-e^{-T_{\mathrm{on}}/(RC)}e^{-j2\pi fT}}\right|^2 S_{V_{co}}(e^{j2\pi fT}) \end{aligned} \tag{7}$$

where the initial $1/T$ scale factor is required since we are converting a discrete-time noise process to a continuous-time signal [18], [19] and the $\mathrm{sinc(fT)}$ function corresponds to the Fourier transform of the $\mathrm{rect}(t,T)$ function.

Under the assumption that $RC \gg T_{\mathrm{on}}$ and $f \ll 1/T$, and using the results from (3), we have

$$\begin{aligned} &S_{V_c}(f) \\ &\quad \approx \frac{1}{T}|T|^2\left|\frac{1}{1-(1-T_{\mathrm{on}}/(RC))(1-j2\pi fT)}\right|^2 \frac{kT_K}{C}\frac{2T_{\mathrm{on}}}{RC} \\ &\quad = T\left|\frac{RC/T_{\mathrm{on}}}{1+j2\pi fT(RC/T_{\mathrm{on}}-1)}\right|^2 \frac{kT_K}{C}\frac{2T_{\mathrm{on}}}{RC} \\ &\quad \approx \left|\frac{1}{1+j2\pi fTRC/T_{\mathrm{on}}}\right|^2 2kT_K TR/T_{\mathrm{on}} \\ &\quad = \left|\frac{1}{1+j2\pi fR_{\mathrm{eff}}C}\right|^2 2kT_K R_{\mathrm{eff}} \end{aligned} \tag{8}$$

Equation (8) reveals that the double-sided noise spectral density of the capacitor voltage with a pulsed resistor is well approximated by the same noise analysis that would be used for a non-pulsed resistor of value R_{eff}, which agrees with the analysis in [17]. However, this is only true when the *RC* time constant is long relative to T_{on}. To be more complete, the noise spectral density, for $f \ll 1/T$, is summarized for both *RC* time constant conditions as shown in (9) at the bottom of the next page. Equation (9) points out that for $RC \ll T_{\mathrm{on}}$, the noise spectral density of the capacitor voltage corresponds to kT_K/C noise scaled by the sample period T. In this case, the noise spectral density is not influenced by the resistor value, but is directly reduced as the sample frequency, $1/T$, is increased, which is a familiar relationship for those experienced with the properties of

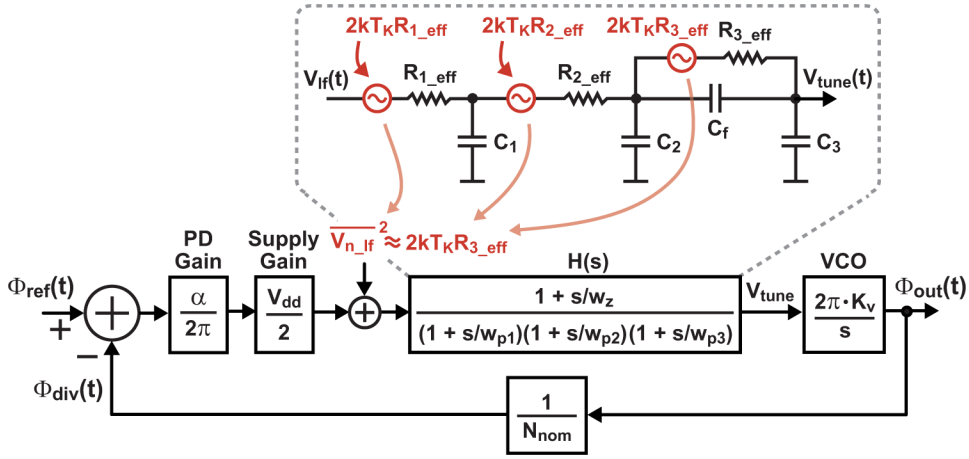

Fig. 8. Noise model of switched resistor PLL assuming double-sided spectral densities.

oversampled discrete-time analog-to-digital converters utilizing sample-and-hold circuits.

C. Noise Model

For a switched resistor loop filter, we will assume that $RC \gg T_{\rm on}$ since we want to boost resistance value rather than implement a sample-and-hold circuit. While the analysis above was performed for a simple first order switched-resistor topology, we have found that its results can be applied to a more complicated switched-resistor circuit so long as the pulsed resistor is connected to capacitive impedance while it is being pulsed, and that the corresponding *RC* time constant remains significantly greater than $T_{\rm on}$. Intuitively, these two conditions lead to relatively constant current flow through the resistor during the time it is pulsed on such that the average current noise corresponds to that of a resistor with effective resistance, $R_{\rm eff}$, as described above.

Based on the analysis of the previous subsection, Fig. 8 displays the noise model of the proposed switched-resistor loop filter under the assumption of double-sided spectral density analysis. In effect, we simply use standard noise analysis for resistor components, but replace the actual resistor value R with its *effective* resistance after pulsing, $R_{\rm eff}$.

As pointed out in the dynamic analysis, $R_{3\_\rm eff}$ will be significantly greater than $R_{1\_\rm eff}$ and $R_{2\_\rm eff}$ for a switched resistor loop filter under the assumption that C_3 is of the same order in value as C_1 and C_2. At low frequency offsets, where the loop filter has the biggest impact on the PLL phase noise, we can approximate the input-referred loop filter noise as being dominated by $R_{3\_\rm eff}$ as shown in the figure. The phase noise contribution of the loop filter can then be estimated as

$$S_{\phi_{\rm out}}(f)|_{lf} = \left|\frac{H(f)K_v/f}{1+\alpha/(2\pi)V_{dd}/(2N_{\rm nom})H(f)K_v/f}\right|^2 \times 2kT_K R_{3\_\rm eff}. \quad (10)$$

At low frequencies, K_v/f will become large so that the above equation is further approximated as

$$S_{\phi_{\rm out}}(f)|_{lf} = \left|\frac{2\pi}{\alpha}\frac{2}{V_{dd}}N_{\rm nom}\right|^2 2kT_K R_{3\_\rm eff}. \quad (11)$$

Equation (11) reveals that choosing a low value of $R_{3\_\rm eff}$ provides a clear path to lowering the phase noise contribution by the loop filter. Unfortunately, lowering $R_{3\_\rm eff}$ leads to higher C_f in order to achieve the same loop filter zero, f_z. Further, (1) reveals that a higher C_f value also forces a higher value of C_3 to maintain the same PLL bandwidth, $f_{\rm bw}$. Therefore, we see that reduction of $R_{3\_\rm eff}$, which can be made relatively small in area through the use of resistor pulsing, leads to the undesirable tradeoff of increasing overall loop filter area due to increased capacitor size. Note that a similar tradeoff occurs in charge pump PLLs.

To avoid large loop filter area, let us consider the other parameters in (11). While V_{dd} is constrained by the CMOS process and available supply voltages, and $N_{\rm nom}$ is constrained by the ratio of desired VCO frequency to reference frequency, the PD gain, $\alpha/(2\pi)$, offers an intriguing degree of freedom. In particular, high PD gain reduces the impact of loop filter noise, thereby allowing a reduction in loop filter area. The next section will introduce a high gain phase detector topology suitable for use with a switched resistor loop filter.

$$S_{V_c}(f) \approx \begin{cases} T\left|\frac{1}{1-e^{-T_{\rm on}/(RC)}e^{-j2\pi fT}}\right|^2 \frac{kT_K}{C} \approx T\cdot kT_K/C & \text{for } RC \ll T_{\rm on} \\ \left|\frac{1}{1+j2\pi f R_{\rm eff}C}\right|^2 2kT_K R_{\rm eff} & \text{for } RC \gg T_{\rm on} \end{cases} \quad (9)$$

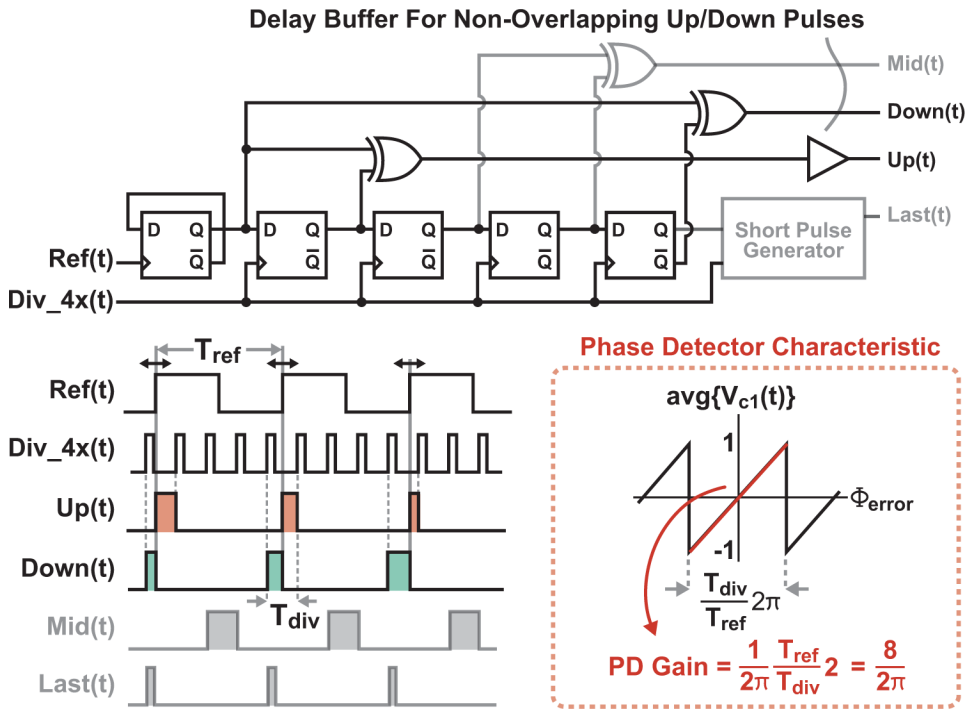

Fig. 9. Proposed high gain phase detector and pulse generator.

V. High Gain Phase Detector and Frequency Detector Circuits

The previous section revealed that high PD gain is desirable both in terms of providing flexiblity in choosing the dynamic parameters of the PLL (such as K_v), and in achieving reduced loop filter area by reducing the impact of loop filter noise on the output phase noise of the PLL. The benefits of high PD gain have previously been exploited in integer-N PLLs using sampled phase detectors [20]–[22]. In this section we present a high gain PD topology which can accomodate both integer-N and fractional-N synthesizer applications assuming a switched resistor loop filter is employed.

A. High Gain PD

Fig. 9 illustrates the proposed high gain PD, which also accomodates non-overlapping pulse generation for the switched resistor loop filter network. The key idea is to leverage a higher divider output frequency to narrow the pulse range of the *Up* and *Down* pulses, and form these pulses in such a manner that their pulsewidth changes in opposite directions as the phase error is changed. To explain the benefit of the reduced pulse range for achieving high PD gain, let us consider the impact of the *Up* and *Down* pulses on $V_{c1}(t)$ within the switched resistor network shown in Fig. 3. For this network, a stream of *Up* pulses of any width lead to a DC average of V_{dd} when the *Down* pulses have zero width, and a stream of *Down* pulses of any width lead to a DC average of 0 in when the *Up* pulses have zero width. The circuit in Fig. 9 creates the *Up* and *Down* pulses in a manner which causes their pulse widths to span across these two extremes over a reference phase range of $2\pi T_{\rm div}/T_{\rm ref}$. Assuming a normalized output range of -1 to 1, the PD gain, $\alpha/(2\pi)$, is calculated as

$$\frac{\alpha}{2\pi} = \frac{2}{2\pi T_{\rm div}/T_{\rm ref}} = \frac{2T_{\rm ref}/T_{\rm div}}{2\pi} \tag{12}$$

Note that an alternative view of the proposed high gain PD is to consider the net charge transfer that occurs with changes in phase, which is proportional to the instantaneous current flow through resistor R_1 during *Up* and *Down* pulses (see Fig. 3). As the *Up/Down* pulse range is reduced, the value of $R_{1\_\rm eff}$ is kept constant by actually *reducing* the value of R_1 due to the switched resistor multiplication property discussed earlier. Therefore, assuming a fixed capacitor value for C_1 and reduction of R_1 to maintain a constant loop filter transfer function, we see that the net charge transfer with changes in phase *increases* as the *Up/Down* pulse range is reduced, which implies an increase in PD gain.

Equation (12) reveals that the phase detector gain is increased as the divider output frequency, $1/T_{\rm div}$, is made higher than the reference frequency, $1/T_{\rm ref}$. The highest practical divider frequency will be a function of the VCO frequency, the divider topology, and the divider range requirements demanded by the dithering action of the Sigma-Delta modulator (for fractional-N synthesizers). For the prototype system shown in Fig. 1, the divider frequency was set to be four times the reference frequency, which leads to a PD gain of $8/(2\pi)$.

In practice, the DC average set by the PD output in the switched resistor loop filter ranges between ground and V_{dd} rather than the normalized range of -1 to 1 assumed when deriving the PD gain above. As indicated in the dynamic model shown in Fig. 5, we account for this issue by including a Supply Gain block of value $V_{dd}/2$. One should note that a charge pump

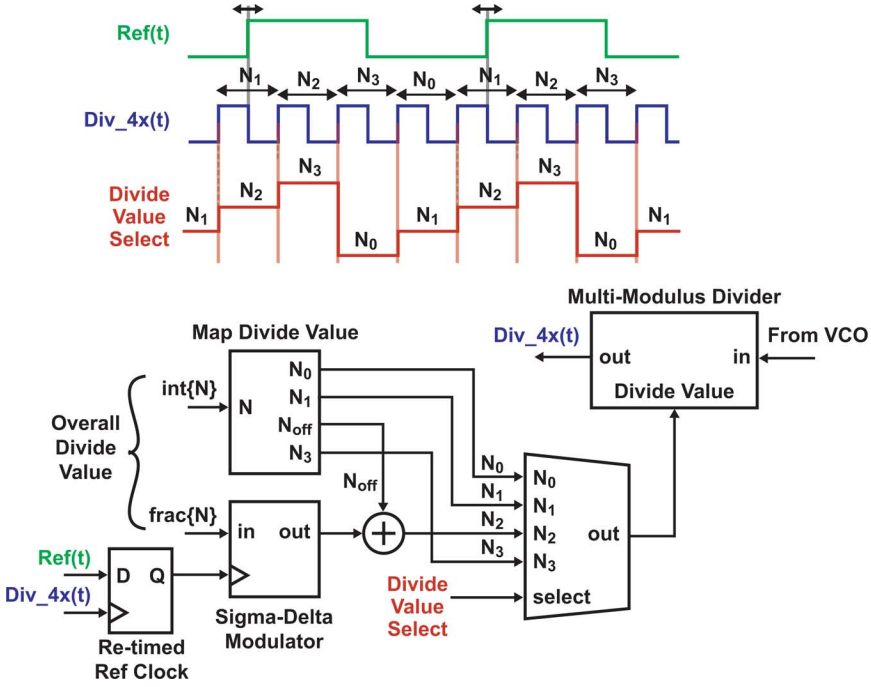

Fig. 10. Control of divider when its output frequency is four times that of the reference frequency.

PLL has an analogous gain term in the form of the charge pump current.

A subtle feature of the proposed PD design in Fig. 9 is that it prevents mismatch between the *Up* and *Down* switch paths of the switched resistor loop filter from impacting linearity of the phase comparison path. This is in contrast to the tristate PFD used within charge pump PLLs, for which great care is often taken to achieve matching between the *Up/Down* charge pump currents [10]. To explain, the proposed PD design essentially corresponds to an XOR-based design in which the *Up* and *Down* pulse widths move in equal and opposite directions as the phase error changes, so that mismatch between the *Up* and *Down* switch paths can slightly impact gain but not nonlinearity in the phase comparison path. In contrast, the tristate design, as indicated in Fig. 2, varies only the *Up* pulse in one phase error region and only the *Down* pulse in the other region, so that nonlinearity occurs as the phase error transitions between these two regions when mismatch is present. Therefore, the proposed PD lowers design complexity for the switched resistor loop filter since mismatch is of little concern. We will discuss other issues which impact nonlinearity of the phase comparison path later in this paper.

The use of a higher divider frequency requires a slightly more complicated divide value control circuit than encountered for traditional synthesizers. Fig. 10 displays such a control circuit for the case where the divider output is four times the frequency of the reference as chosen for the protoype [23]. Here we see that an overall divide value, N, must be mapped into four sub-divide values such that $N = N_0 + N_1 + N_2 + N_3$. For a fractional-N synthesizer, only one of these sub-divide values need be dithered by the Sigma-Delta modulator.

In addition to offering high PD gain, the proposed PD structure shown in Fig. 9 provides a simple means of producing non-overlapping pulses for the switched resistor network. However, as indicated in the figure, it is desirable to achieve a small pulsewidth for the *Last* pulse, which controls R_3, in order to achieve the large 16 MΩ value of R_{3_eff} for the prototpye without requiring a large area implementation for R_3.

An elegant way to achieve short pulse widths is to leverage the frequency divider to produce them. Fig. 11 shows a commonly used multi-modulus divider structure that consists of a cascade of divide-by-2/3 stages [24]. Each divider stage has a *modout* output whose pulsewidth corresponds to the period of its input. Since the frequency is progressively lowered each stage, the overall divider output pulsewidth can be chosen to be different values based on which divider stage is tapped. As shown in Figure 9, the high gain PD can take advantage of the short pulses of the divider output through digital logic to create the desired *Last* pulses with short duration.

B. Frequency Detection

The high gain PD structure discussed above needs to be augmented with a frequency acquisition circuit. To provide a better understanding of this issue, Fig. 12 illustrates the impact of having a large enough frequency error such that cycle slipping occurs in the PLL. In such case, the phase sweeps across its available range, which leads to a sweeping of the VCO control voltage through the capacitive coupling network of the switched resistor loop filter. Since the capacitor coupling network attenuates signals traveling through it, we see that only a narrow range of VCO control voltages is swept across. A frequency acquisition circuit must act as an additional influence on the VCO control voltage such that the swept range shown in the figure includes the voltage setting for the desired VCO frequency.

Fig. 13 shows a conceptual view of the proposed frequency detection circuit, which operates by comparing the number of

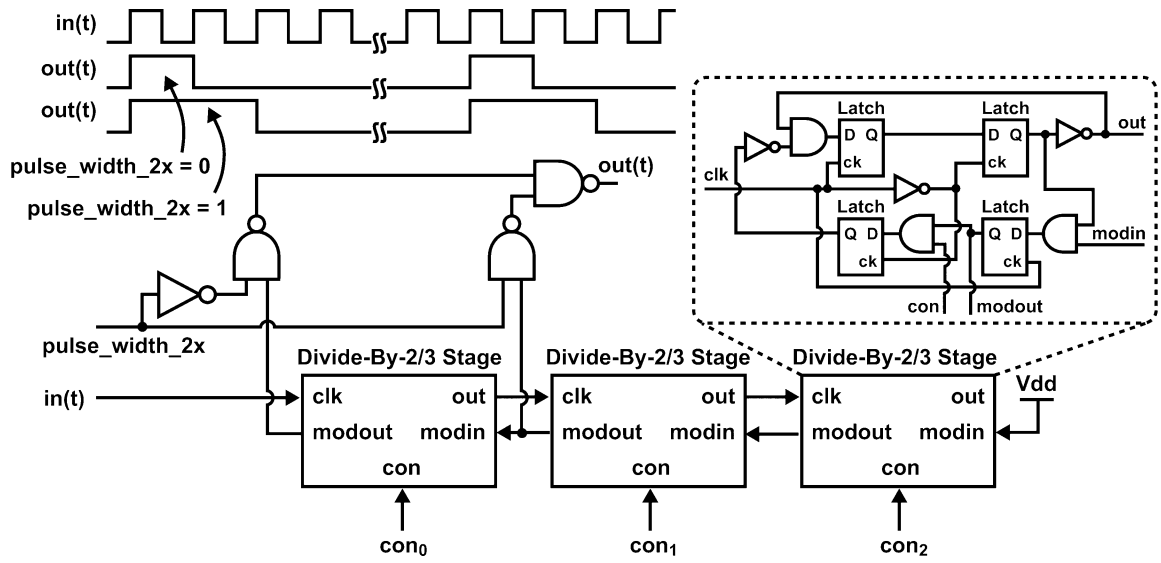

Fig. 11. Achieving short pulse generation directly from a commonly used multi-modulus divider [24].

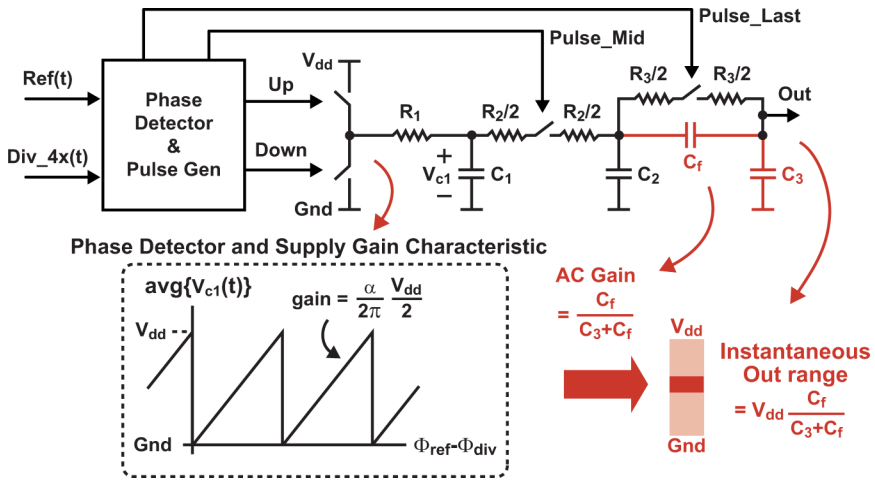

Fig. 12. The need for additional circuits for initial frequency acquisition.

divider edges for every reference edge. Assuming four times higher divider frequency, the divider edge count will always be four for each reference edge once the PLL is locked. However, if the output frequency is too high or too low, then the divider count will take on values that are higher or lower than four, respectively. Under such conditions, the auxiliary capacitor, C_c, is charged either high or low and then connected to capacitor C_3. By doing so, the voltage across C_3 is immediately bumped up or down, respectively, such that the VCO control voltage moves closer to its desired value.

A simplified circuit implementation of the proposed frequency detector is shown in Fig. 14. In this case, we see that the phase detector structure is extended to provide sensing of whether four divider edges occur for every reference edge, and extra logic is added to appropriately control the switches on capacitor C_c when frequency error is detected.

Fig. 15 displays a CppSim [25] behavioral simulation of key signals in the switched resistor PLL during frequency acquisition. As seen by the figure, the proposed frequency acquisition method provides an efficient adjustment of the VCO control voltage in the proper direction until the phase detector is able to lock the PLL. At this point, the auxiliary capacitor, C_c, is automatically disengaged from the loop filter so that the frequency detection circuit has no influence on the PLL during steady state operation.

VI. The Issue of Nonlinearity

A drawback of the proposed switched resistor loop filter is the fact that it introduces nonlinearity into the phase comparison path. This is not an issue for integer-N synthesizers, but it will lead to folding of the Sigma-Delta quantization noise when applied to fractional-N synthesizers. Fig. 16 highlights the key signals involved in this issue. As we will see, variations in phase error, which are encoded as relative changes in width of the *Up* and *Down* pulses, impact the VCO control voltage in a nonlinear manner.

To provide a more quantitative understanding of this nonlinearity issue, let us consider a simple case where we focus solely on voltage V_{c1} across capacitor C_1 of the first *RC* section. Since resistor R_2 gates charge to the following stages in

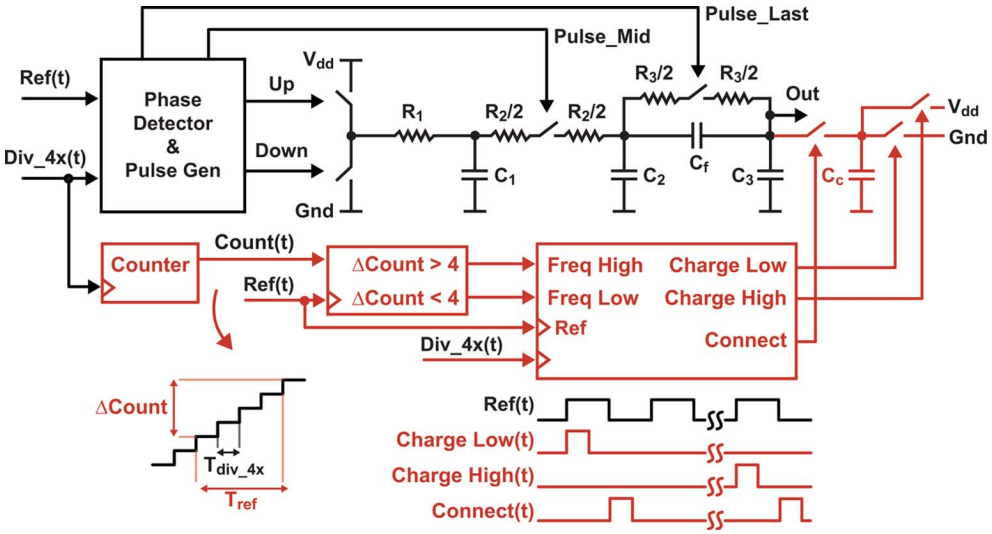

Fig. 13. Conceptual view of proposed frequency detection logic.

a non-overlapping manner relative to the *Up* and *Down* pulses, we can ignore the transients on V_{c1} and instead focus on the hold values, $V_{c1}[k]$, that are produced upon completion of the *Up/Down* pulse activity. Given a pulsewidth deviation of ΔT on the *Down* pulse, and $-\Delta T$ on the *Up* pulse, the relationship between current and previous hold voltages across capacitor C_1 is

$$V_{c1}[k] = -V_{dd}e^{-\frac{1}{R_1C_1}\frac{T_{\rm div}}{2}}e^{\frac{1}{R_1C_1}\Delta T} + e^{-\frac{T_{\rm div}}{R_1C_1}}V_{c1}[k-1] + V_{dd} \quad (13)$$

The first term of (13) reveals that ΔT has a nonlinear impact on $V_{c1}[k]$. However, in the case where $\Delta T/(R_1C_1)$ is small, we can approximate

$$e^{\Delta T/(R_1C_1)} \approx 1 + \frac{\Delta T}{R_1C_1} \quad \text{for} \quad \Delta T \ll R_1C_1. \quad (14)$$

This last expression reveals that the nonlinear impact of the switched resistor loop filter is reduced as its first stage *RC* time constant is increased relative to the amount of phase perturbation, ΔT (expressed here in time rather than radians). As such, we see that Sigma-Delta quantization noise folding is reduced as the PLL bandwidth is reduced (which increases the *RC* time constant) and as the Sigma-Delta order is reduced or the VCO frequency is increased (each of which decreases the amount of phase deviation represented by ΔT).

For the prototype considered in this paper, a PLL bandwidth of 30 kHz was chosen with a VCO output frequency in the range of 720 to 910 MHz and MEMS reference frequency of 5 MHz. Using a detailed CppSim behavioral model of the PLL with a VCO frequency of 800 MHz, Fig. 17 displays calculated versus simulated phase noise contributions of second and third order MASH Sigma-Delta quantization noise within the closed loop PLL. For reference, the overall phase noise of the system is also shown, which will be further elaborated on in the following section. As revealed by Fig. 17, noise folding is quite minor for the second order case, but is significant for the third order case. However, when compared to the other noise sources in this prototype (as indicated in Fig. 17), either Sigma-Delta order can be used without issue. This observation was confirmed through phase noise measurements of the prototype, which included implementations of both of these Sigma-Delta topologies.

Note that in addition to the issue described above, there are other potential sources of nonlinear noise folding for the switched resistor PLL, as also encountered with traditional charge pump fractional-N synthesizers [26], such as transients in the regulated supply voltage. In the case of the prototype presented here, measured results did not reveal a detectable impact from this issue.

VII. Prototype and Measured Results

Fig. 18 shows the 0.18 um CMOS die with MEMS die wirebonded on top corresponding to the programmable MEMS oscillator system shown in Fig. 1. To achieve accurate temperature measurement of the MEMS resonator, the on-chip temperature sensor was placed in the portion of the CMOS die underneath the MEMS die. As indicated in the figure, the CMOS die area is 1.64 mm by 1.5 mm. By utilizing conventional wafer grinding techniques to thin the CMOS and MEMS dies [27], the stacked CMOS/MEMS die structures are placed in standard 0.75 mm thick plastic QFN packages.

Referring to Fig. 3, key passive components of the loop filter were chosen as $C_1 = 20$ pF, $C_2 = 19$ pF, $C_3 = 35$ pF, $C_f = 2.3$ pF, $R_1 = 4.47$ kΩ, $R_2 = 13.4$ kΩ, and $R_3 = 500$ kΩ. The *LC* VCO, which operates between 720 MHz and 910 MHz depending on the selection of 16 switchable capacitors, has a varactor tuning gain in the range of $K_v = 65$ MHz/V to 165 MHz/V, which is adequate to maintain its desired operating frequency in the presence of thermal variations. The entire fractional-N PLL, including the loop filter but excluding the *LC* VCO and buffer, has an area of 0.09 sq. mm. The *LC* VCO and its buffer have an area of 0.25 sq. mm., and the output divider has an area of 0.02 sq. mm.

The current consumption of the entire chip corresponding to Fig. 1 is measured to be 3.2/3.7 mA (typical) at 1.8/3.3 V supply

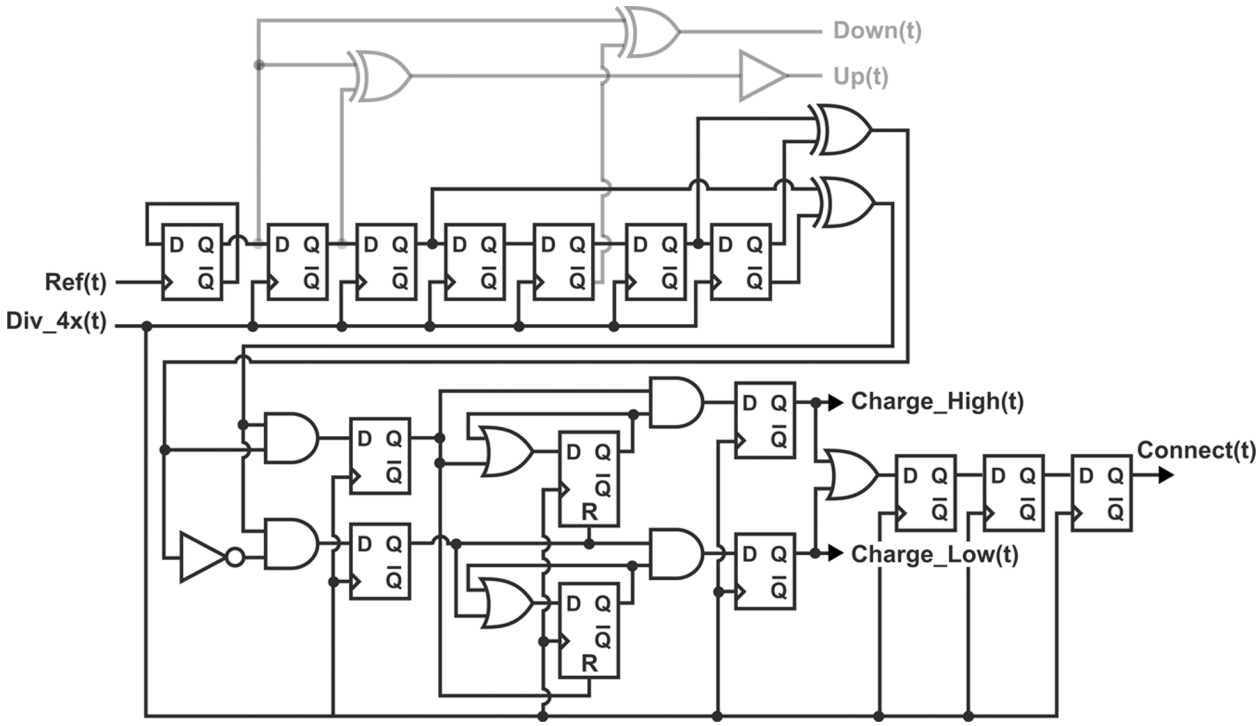

Fig. 14. Simplified circuit implementation of the frequency detector logic.

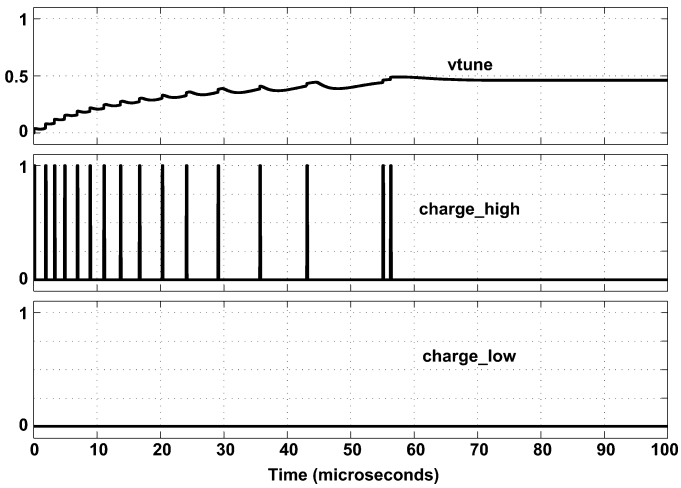

Fig. 15. CppSim behavioral simulation of frequency locking with proposed frequency detection approach (see Fig. 3 for signal definitions).

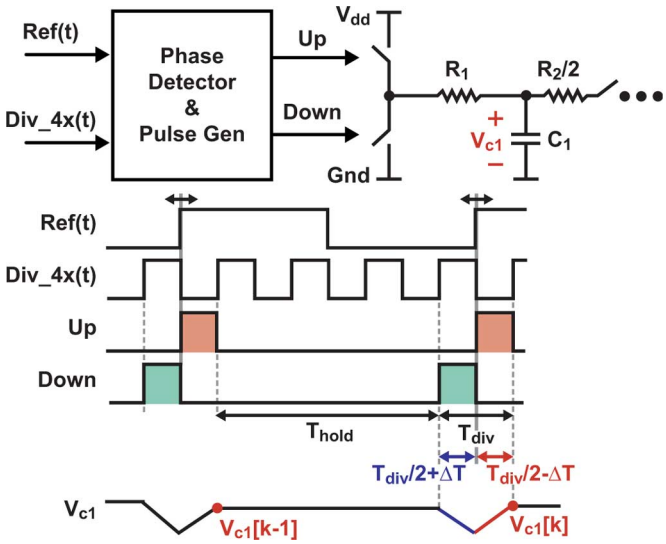

Fig. 16. Nonlinearity issue for switched resistor loop filter.

assuming 20 MHz output and no load. Of this total current consumption, the VCO and buffer is estimated to consume 1.3 mA and the rest of the PLL is estimated to consume 0.7 mA based on SPICE simulations. Note that on-chip voltage regulators set the internal supply voltage of the VCO and its buffer, as well as the other PLL blocks, to be 1.5 V under all external supply voltage conditions.

Fig. 19 displays measured frequency stability for 6600 parts across a temperature range of -40 to 85 degrees C after single temperature calibation was performed of the on-chip temperature sensor and compensation circuits indicated in Fig. 1. The figure reveals better than ± 30 ppm stability across this 125 degree temperature range. Note that the uncompensated MEMS oscillator exhibits frequency variation of approximately -30 ppm per degrees C.

Fig. 20 displays measured phase noise of the prototype with a 100 MHz output frequency. The phase noise plot reveals that the PLL bandwidth is approximately 30 kHz, the reference spur at 5 MHz offset is -65 dBc, and integrated phase noise (1 kHz to 40 MHz) is 16.7 ps rms. The plot reveals a fractional spur at 500 kHz, and a spur at 2.5 Mhz due to the second harmonic of switching R_3 at 1/4 the 5 MHz reference frequency. Harmonics of the reference spur above 5 MHz (i.e., 10, 15, 20 MHz, etc.) are somewhat accentuated due to an on-chip charge pump that supplies the MEMS bias voltage. Note that the slight phase noise

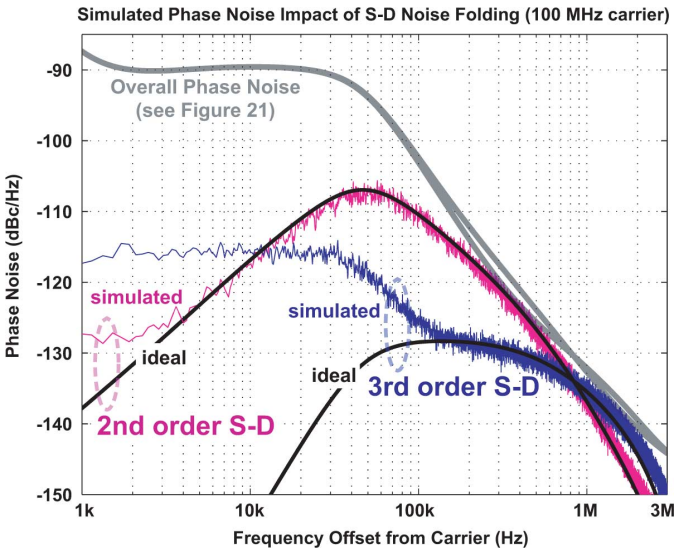

Fig. 17. Impact of switched resistor nonlinearity in Sigma-Delta quantization noise for second and third order Sigma-Delta MASH topologies.

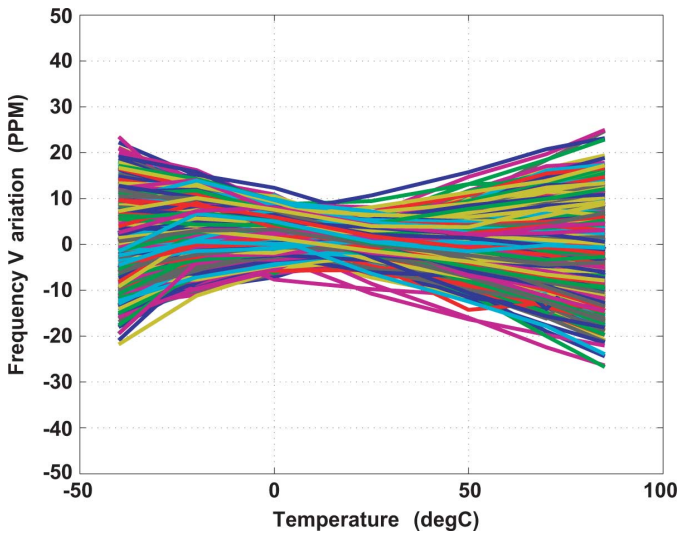

Fig. 19. Measured frequency variation across a temperature range of −40 to 85 degrees C for 6600 parts.

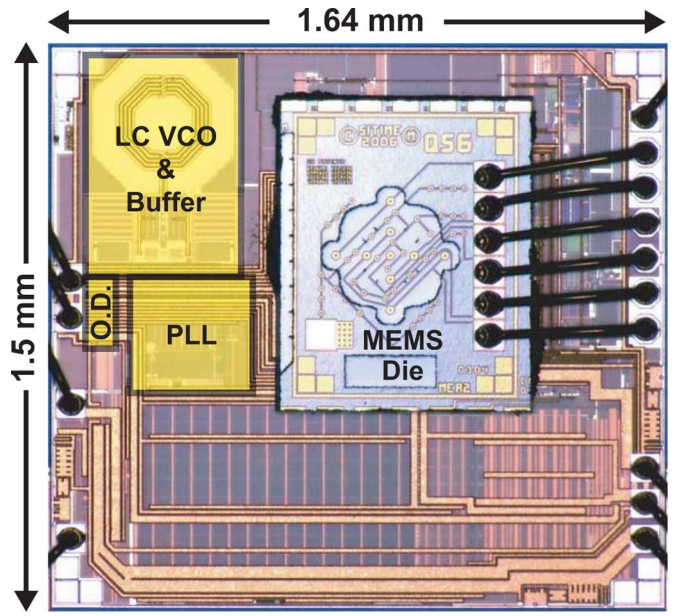

Fig. 18. Prototype IC consisting of the CMOS die with MEMS die attached.

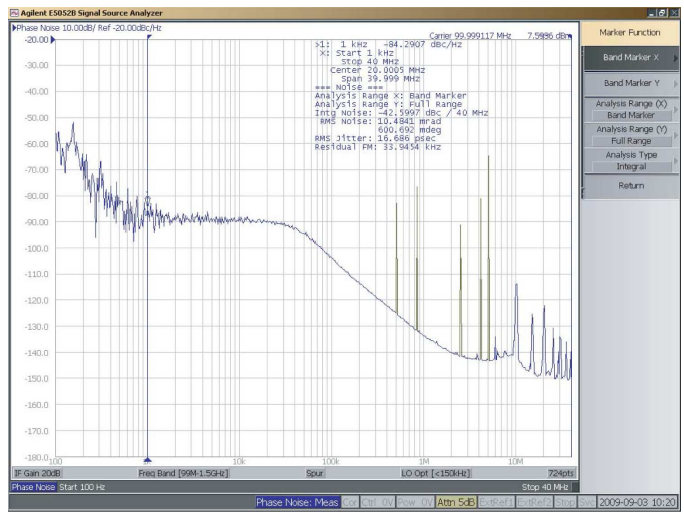

Fig. 20. Measured phase noise at 100 MHz output frequency. Note that divider dithering by the second order modulator of the fractional-N synthesizer and temperature compensation of the MEMS frequency are both active in this measurement.

hump at 10 MHz is caused by noise from the on-chip voltage regulator of the programmable output divider and drive path.

Overall, the phase noise performance is adequate for a wide variation of applications, including most serial applications, embedded systems and FPGAs, audio, USB 1.1 and 2.0, cameras, etc. Table I provides a summary table of measured performance of the prototype.

Finally, Fig. 21 provides calculated phase noise contributions of the key PLL components under closed loop PLL conditions. As revealed by this figure, the loop filter noise is far from being a significant contributor despite its very low area.

VIII. Conclusion

This paper presented a fractional-N synthesizer structure based on a switched resistor loop filter which achieves low area,

TABLE I
SUMMARY OF MEASURED PERFORMANCE OF THE PROTOTYPE

Specification	Typical Value
Supply Voltage	1.8/3.3 V
Supply Current (no load, 20 MHz output)	3.2/3.7 mA
CMOS Die Area	2.46 mm^2
Overall PLL Area (including LC VCO)	0.36mm^2
Internal Supply Voltage of PLL	1.5V
Overall PLL Current Consumption	2.0mA
PLL Bandwidth	30kHz
Reference Spur (100 MHz output)	-65dBc
Integrated Phase Noise (100 MHz output) (integration range: 1kHz to 40MHz)	16.7ps
Frequency Stability (-40 to 85 deg C) (single temperature calibration)	< +/-30 ppm

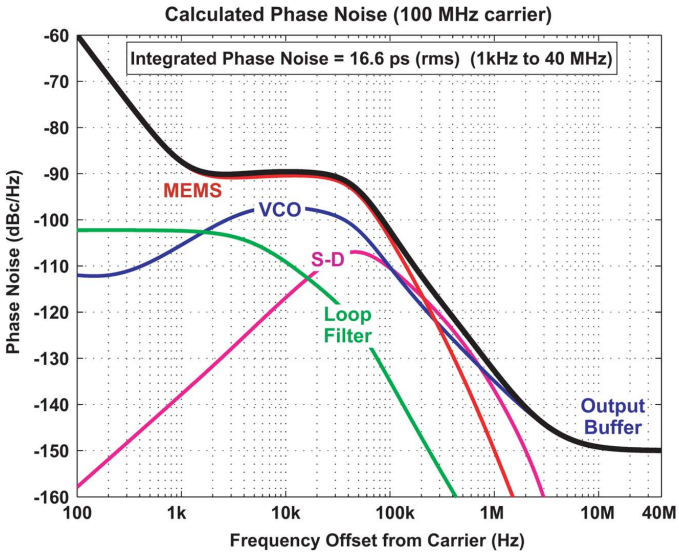

Fig. 21. Calculated closed loop impact of various PLL noise components on overall output phase noise of prototype.

low power, and low analog design complexity. The switched resistor structure eliminates the need for a charge pump and its associated design complexity, and reduces the loop filter area by boosting resistance values through resistor pulsing. To reduce the impact of loop filter noise, a high gain phase detector topology was introduced which also provides efficient non-overlapping pulse generation for the switched resistor network. A switched capacitor frequency detection circuit augments the high gain PD to achieve reasonably fast frequency acquisition without impact to steady state noise.

The proposed fractional-N synthesizer structure was utilized as a key component to realizing a programmable MEMS-based oscillator that provides an efficient clock solution for many electronic applications. By enabling programmability and a simple approach to process and temperature compensation, the resulting clock reference provides low lead times and a low cost path to achieve simplified supply chain and inventory management for frequency references demanding better than ± 30 ppm stability.

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From 1996 to 1997, he worked at Hughes Communication Business Unit on low frequency RF control circuits. From 1998 to 2005 he was with Exar Corporation where he worked on a broad range of CMOS integrated circuits including video ADC's for CCD image sensors, frequency synthesizers, and CDR circuits. From 2005 to 2009 he was with SiTime Corporation where he helped design their first three generations of MEMS based synthesizer products. He is currently working for Globalfoundries on GHz transceivers in 28 nm CMOS.

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Fred S. Lee (M'07) received the B.S., M.Eng., and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, MA, in 2002 and 2007.

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Dr. Lee received the DAC/ISSCC Student Design Contest Award in 2004 and the ISSCC Jack Kilby Best Student Paper Award in 2007.

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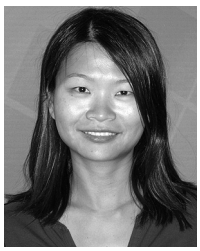
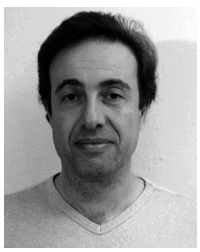
Since then, he has held logic design and CAD positions in various companies such as Synergy Semiconductor, Cadence Design Systems, Centillium Communications, and Actel Corporation. He is currently a logic designer at SiTime Corporation.



Cathy Lee was born in Hong Kong. She received the B.S. degree in electrical and computer engineering from University of Texas at Austin in 1994, and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, in 1995.

From 1995 to 1998, she was a design engineer at Crystal Semiconductor/Cirrus Logic, Austin, TX, where she worked on a high speed 6-bit flash A/D converter for hard disc drive read channels. From 1998 to 2006, she was with Maxim Integrated Products, Sunnyvale, CA, where she developed and introduced various products including switched capacitor filters, 16-bit SAR ADCs, Audio DACs, and analog video cable equalizers for CCTV. She then joined Amalfi Semiconductor, Los Gatos, CA, in 2006, where she designed power control circuits for CMOS RF power amplifiers used in cell phones. In 2008, she joined SiTime, Sunnyvale, CA, where she developed circuits for low noise and temperature stable MEMS clock chips. She is currently working on isolator products at Silicon Laboratories, Sunnyvale, CA.



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As an employee of IBM and AMD, he worked on digital and analog circuits in areas of supercomputing and Ethernet networks from 1987 to 2000. From 2000 to 2002 he managed a circuit design team at Intel Corporation working on an AGP8X graphics interface. Since 2002, as an employee of National Semiconductor, Marvell, and SiTime, he specialized in design of switched capacitor ADCs, such as SAR, pipeline and Sigma-Delta ADCs. Currently he is working at Invensense Corporation, where he is responsible for development of various circuits related to MEMS interfaces. He is an inventor of 11 patents that cover various circuit design techniques in areas of filter and ADC design.

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Bruno W. Garlepp (S'93–M'97) was born in Bahia, Brazil, in 1970. He received the B.S.E.E. degree from the University of California, Los Angeles, in 1993 and the MS.E.E. degree from Stanford University, Stanford, CA, in 1995.

In 1993, he joined the Hughes Aircraft Advanced Circuits Technology Center, Torrance, CA, where he designed high-precision analog ICs for A/D applications and RF circuits for wideband communications. In 1996, he joined Rambus Inc., Mountain View, CA, where he designed high-speed CMOS clocking and I/O circuits for synchronous chip-to-chip interfaces. In 2000, he joined Silicon Laboratories, Austin, TX, where he designed high-performance CDR and clock synthesis ICs for SONET applications. In 2003, he returned to Rambus Inc. where he designed multi-gigahertz signaling interfaces for serial data communications and led a team investigating multi-tone techniques for multi-gigahertz serial links. In 2007, he joined SiTime Corp., Sunnyvale, CA, where he directed the design of synthesizer and timing ICs based on silicon MEMS resonators. In 2010, he re-joined Silicon Laboratories to explore and begin development of new product opportunities at their design center in Sunnyvale, CA.