

A 2.5-Gb/s Multi-Rate 0.25- μm CMOS Clock and Data Recovery Circuit Utilizing a Hybrid Analog/Digital Loop Filter and All-Digital Referenceless Frequency Acquisition

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Abstract—A 0.25- μm CMOS, multi-rate clock and data recovery (CDR) circuit that leverages unique analog/digital boundaries in its phase detector and loop filter to achieve a fully integrated CDR implementation with excellent performance, compact area, and low power dissipation is presented. Key circuit blocks include a phase-to-digital converter that combines a Hogge detector with a continuous-time first-order Sigma-Delta analog-to-digital converter, and a hybrid loop filter that contains an analog feedforward path and digital integrating path. In addition, an all-digital frequency acquisition method that does not require a reference frequency, quadrature phases from the VCO, or a significant amount of high-speed logic is presented. A nice byproduct of the frequency acquisition circuitry is that it also provides an estimate of the bit error rate (BER) experienced by the CDR. The CDR exceeds all SONET performance requirements at 155-, 622-, and 2500-Mb/s as well as Gigabit Ethernet specifications at 1.25 Gb/s. The chip operates with either a 2.5- or 3.3-V supply, consumes a maximum of 197 mA across all data rates, and fits in a 5 \times 5 mm package.

Index Terms—Analog-to-digital, bit error rate (BER), clock and data recovery (CDR), frequency acquisition, hybrid loop filter, integrated loop filter, mixed-signal, multi-rate, phase-locked loop (PLL), phase-to-digital, referenceless, Sigma-Delta, SONET.

I. INTRODUCTION

THERE has recently been a growing interest in developing new mixed-signal architectures that minimize their analog content in favor of expanded digital content. Indeed, reducing

analog content offers the advantage of higher immunity to the degraded analog characteristics of new CMOS processes such as increased leakage current and a reduced $g_m r_o$ product, and benefits from the high-density, low-power operation and standardized design flow achievable with digital circuits. However, there are advantages when using analog circuits for some signal processing tasks, and so a key issue is determining where the appropriate boundaries should lie between analog and digital implementations of a given architecture. Here we explore this issue in the context of designing a high-performance, multi-rate clock and data recovery (CDR) circuit for SONET applications in 0.25- μm CMOS.

Fig. 1 displays a classical analog CDR circuit and its function within a high-speed optical data link. The data link consists of a transmitter that outputs a high-speed, nonreturn to zero (NRZ) data stream, which is transported down a high-bandwidth optical fiber and then received by the optical receiver shown in the figure. The receiver converts the optical data stream into an electronic signal using a photodiode and transimpedance amplifier, and then uses the CDR to extract a clock signal which is aligned to the data stream in frequency and phase. The clock signal is used to first re-time the data stream and then clock it into a high-speed digital ASIC chip that performs desired processing operations.

Classical CDR solutions use an analog voltage-controlled oscillator (VCO) to generate the output clock signal, and an analog feedback loop to set the VCO frequency and phase. The analog feedback loop leverages an analog phase detector and loop filter to measure and smooth the instantaneous phase error between the input data stream and output clock. This approach typically has a very limited frequency capture range, so that the output clock needs to be very close in frequency to its desired value in order for the phase error feedback loop to function correctly. A common technique is to first align the VCO frequency to a multiple of an input reference clock signal such that a low-frequency error is obtained before engaging the phase detector feedback loop [1]. However, it is often preferred to avoid the need for the externally supplied reference frequency, so that analog techniques have been proposed to perform referenceless frequency acquisition [2]–[6].

The analog architecture shown in Fig. 1 poses many design challenges when trying to achieve a fully integrated and robust

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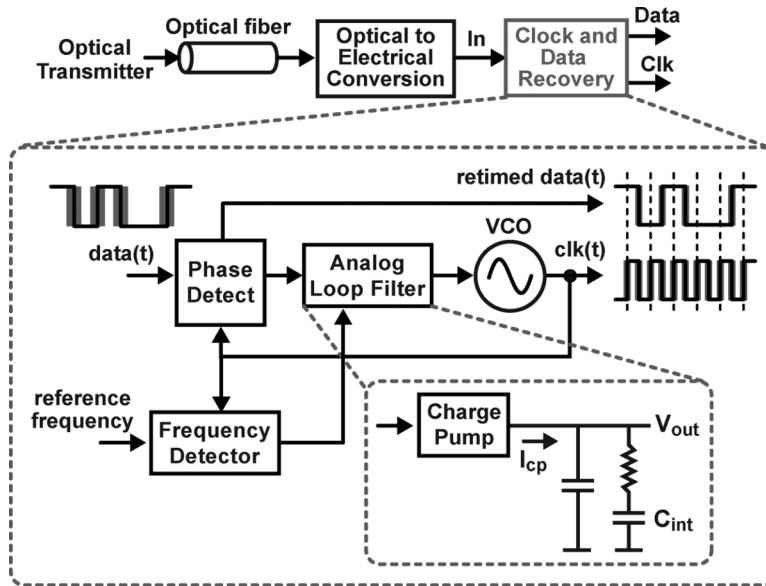


Fig. 1. Classical analog CDR and its place within a high-speed optical link.

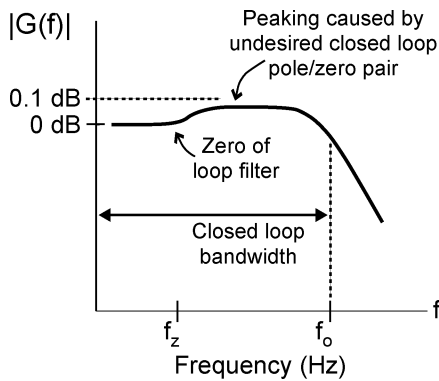


Fig. 2. Jitter transfer function of the analog CDR.

CDR implementation which satisfies SONET jitter transfer specifications at different data rates. A key challenge for this structure is in realizing a fully integrated and configurable loop filter that provides the desired closed-loop jitter transfer function of the CDR shown in Fig. 2. The closed-loop bandwidth of the jitter transfer function must be set according to the desired data rate—operation at 155 Mb/s, 622 Mb/s, and 2.5 Gb/s requires closed-loop bandwidth values of roughly 62.5 kHz, 250 kHz, and 1 MHz, respectively. Due to the presence of a closed-loop pole/zero combination, peaking occurs in the transfer function which must be reduced to less than 0.1 dB to meet SONET requirements. To achieve this peaking requirement, the zero value must be reduced to a low value by choosing a high value for the loop filter capacitor C_{int} . The requirement for a large capacitor value severely complicates efforts to achieve a compact and fully integrated implementation of the loop filter. In addition, the shown analog filter topology is highly sensitive to temperature and process variations as well as leakage currents that cause the VCO frequency to drift in the absence of incoming data transitions.

In this paper, we propose a CDR architecture that utilizes a hybrid analog/digital loop filter and purely digital frequency

acquisition to achieve a fully integrated, highly configurable, low-jitter CDR architecture in 0.25- μm CMOS that supports multi-rate operation at 155-Mb/s, 622-Mb/s, Gigabit Ethernet, and 2.5-Gb/s data rates. Rather than requiring a large capacitor to meet jitter peaking requirements, the proposed filter structure simply requires a moderate number of digital bits within a compact digital accumulator structure. The required range of jitter transfer function bandwidths and zero values for the various data rates is achieved through simple digital control circuitry. The proposed digital frequency acquisition approach removes the need for an external reference frequency and is implemented with minimal circuitry operating at high frequencies.

We begin by discussing background information on the key issues facing digital implementation of the VCO and phase detector within the CDR, and the drawbacks of current analog approaches in achieving referenceless frequency acquisition. We then propose several circuit architectures that alleviate such issues in 0.25- μm CMOS by leveraging unique boundaries between digital and analog circuit implementations for the phase detector and loop filter, and by using an algorithmic approach to referenceless frequency acquisition. We then present a dynamic and noise model for the proposed CDR, show measured results, and summarize the key points in the conclusion of the paper.

II. BACKGROUND

To avoid the above-mentioned problems stemming from an analog loop filter implementation, a good starting point would be to consider an all-digital implementation of the CDR as shown in Fig. 3. In this case, we might consider recently proposed techniques for “all-digital” frequency synthesizers [7] to achieve digital implementations of the phase detector, loop filter, and VCO.

Focusing first on the VCO, we can leverage the switched-capacitor network within an LC oscillator to achieve a digitally controlled oscillator (DCO) as indicated in Fig. 3 and proposed

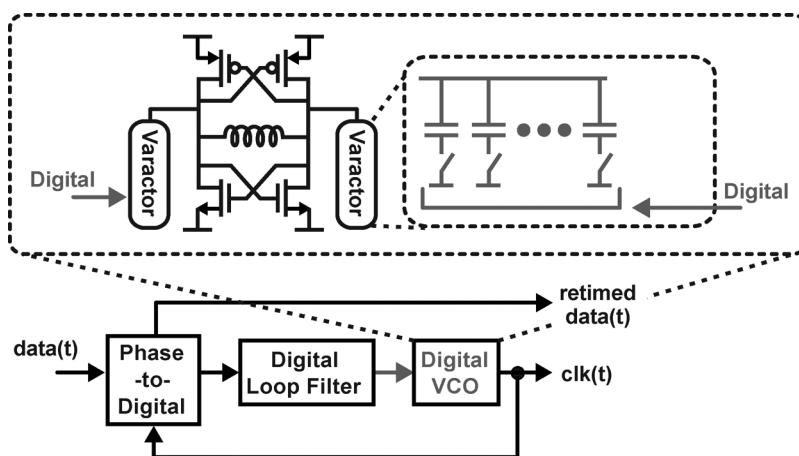


Fig. 3. An "all-digital" CDR implementation.

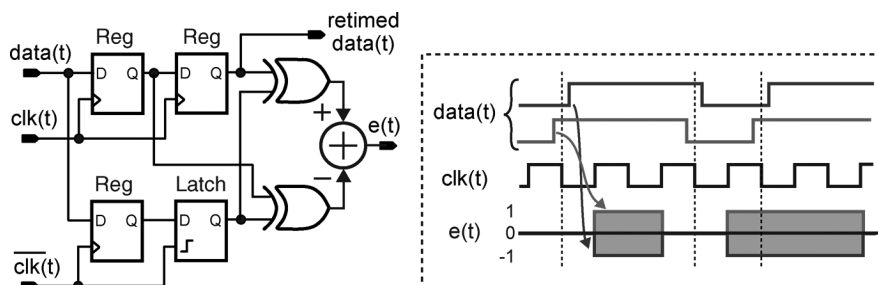


Fig. 4. Bang-bang phase detector and associated signals.

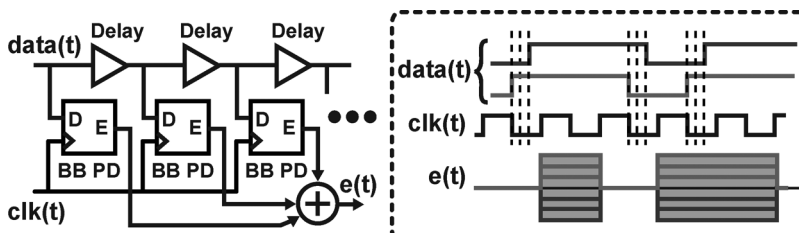


Fig. 5. Multi-level bang-bang and associated signals.

in [8]. However, this approach is best suited for fine geometry processes such as 130-nm and 90-nm CMOS since it requires extremely small capacitor values and significant digital circuitry to achieve fine frequency resolution and good phase noise. Unfortunately, such processes are at a cost disadvantage compared to older processes such as 0.25- μm CMOS due to the relatively small volumes offered by the SONET market. Therefore, instead of following an all-digital approach for this application, we instead turn to the hybrid analog/digital approach described in [9]. We provide more details on this VCO structure in the next section.

As for the phase detector, a simple approach for achieving a digital implementation is to employ the commonly used bang-bang circuit shown in Fig. 4 [10]. In this approach, the resulting phase error signal is a three-level digital signal corresponding to whether a given data transition is early, late, or absent relative to the clock phase within a given clock period. While the resulting implementation is very simple and indeed digital, it unfortunately leads to nonlinear dynamics for the CDR and

complicates efforts to reliably meet the SONET jitter transfer specification [11].

We can effectively linearize the bang-bang detector response by introducing more levels in its phase error characteristic as shown in Fig. 5. Similar in structure to the time-to-digital structure employed in [7], this phase detector uses simple digital buffers to create delayed versions of the data transitions which are then compared to the VCO output clock phase using multiple bang-bang detectors. Unfortunately, this approach carries the penalty of high power consumption and high clock loading on the VCO output due to the large number of phase detector elements running at high frequencies.

In contrast to the above digital approaches, it is worthwhile to consider the commonly used analog Hogge detector shown in Fig. 6 [12]. This topology achieves an infinite resolution phase error signal encoded in the width of its output error pulses, so that linear CDR dynamics are obtained in a compact area with minimal complexity and low power dissipation. Of course, the catch is that this approach classically leads to an analog loop

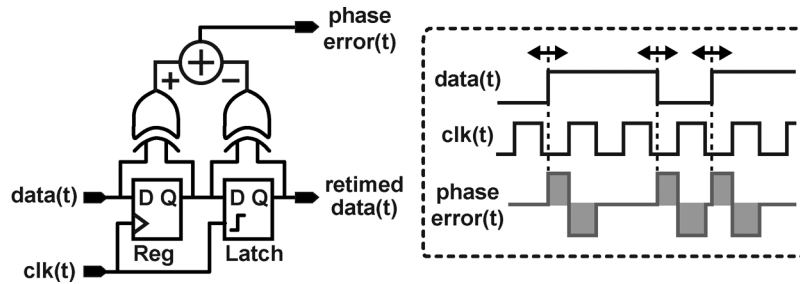


Fig. 6. Analog Hogge detector and associated signals.

filter and its associated challenges. In the next section we introduce a simple modification of the Hogge detector that achieves efficient, linear phase-to-digital conversion.

While phase detection is effective when initial frequency offsets are small, additional circuitry is required to perform frequency acquisition when initial frequency offsets are large. Several approaches have been proposed to achieve referenceless frequency acquisition for such systems using clever phase/frequency detector topologies [2]–[6]. These approaches use a frequency detector to sense the sign of the frequency offset based on the direction of phase movement of the data edges and then apply an analog signal to push the VCO frequency in the right direction to lower the frequency offset. While these methods have proven to be effective for proper analog adjustment of the VCO over a narrow frequency offset range, they have the disadvantages of often requiring quadrature VCO phases at the full clock rate and must be modified to interface with a VCO with digital frequency control. We describe an alternative frequency detection method in this paper which avoids such issues.

III. PROPOSED HYBRID CDR ARCHITECTURE

In contrast to a primarily analog or digital CDR structure, we propose a mixed-signal architecture which leverages several unique hybrid analog/digital circuit blocks to implement the phase detector, loop filter, and referenceless frequency acquisition with compact area and low power dissipation. We discuss these blocks in more detail in this section.

A. Phase Detector

Fig. 7 displays a simplified view of our proposed phase-to-digital converter, which combines a classical Hogge phase detector with a continuous-time first-order Sigma-Delta analog-to-digital converter (ADC) [13]. This structure offers linear phase detection (such that the SONET jitter transfer specification can be readily achieved), compact area and low power dissipation, and a purely digital output signal as desired. Interfacing between the Hogge phase detector and Sigma-Delta structure is accomplished by feeding their output currents (produced by charge pumps I_{pd} and I_{sd}) into capacitor C_{int} such that the voltage across the capacitor corresponds to the integrated error between the Hogge and Sigma-Delta outputs. This voltage signal is amplified by a low-gain, high-bandwidth amplifier and then fed into the input of the Sigma-Delta quantizer. The quantizer output then toggles in a manner to continually keep the voltage of capacitor C_{int} at a midrange value so that the average error between the quantized output

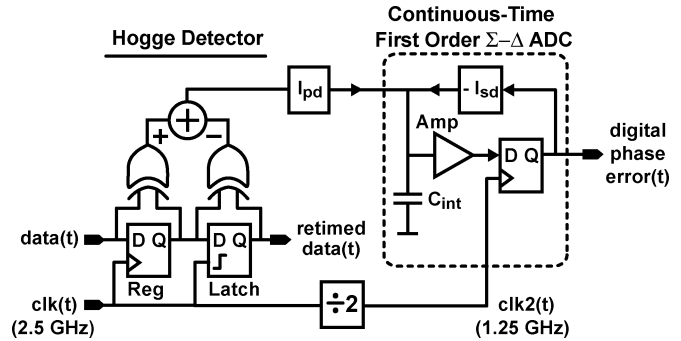


Fig. 7. Simplified diagram of proposed phase-to-digital converter.

and the Hogge detector is zero. While first-order Sigma-Delta modulators are notorious for having dead zones and large tones in their quantization noise spectrum, these issues are alleviated by the scrambling action of the random pulse stream from the Hogge detector and the insensitivity of the CDR performance to tones in its jitter spectrum since only the overall rms jitter matters, not its corresponding spectral profile. A subtle point is that the noise shaping action of the Sigma-Delta ADC removes the need for waveform shaping of the Hogge detector output, as proposed in [14], [15], to achieve low CDR jitter across a wide range of input data patterns.

The Sigma-Delta quantizer shown in Fig. 7 is prone to metastable behavior due to the fact that its input is often close to its trigger point during each clock transition. Such metastable behavior can cause the digital output signal to take on poorly behaved voltage levels, and also causes inaccuracy in achieving zero average error between the overall digital output signal and the Hogge analog output. To lower the number of metastable events, the voltage across capacitor C_{int} is amplified before being presented to the quantizer input, and a half-rate clock of 1.25 GHz, rather than 2.5 GHz, is used to clock the quantizer. The integrating input of the Sigma-Delta modulator acts as an anti-alias filter, so that lowering the ADC sample rate to 1.25 GHz does not cause aliasing problems.

Operating the Hogge detector at 2.5 Gb/s is challenging in 0.25- μm CMOS. Key issues are achieving a low phase offset between the input clock and data signals (in order to achieve high jitter tolerance), and achieving a linear phase error characteristic over a wide phase error range. To address these issues, the classical Hogge detector is modified as shown in Fig. 8. To achieve low phase offset, a buffer is inserted between the input data signal and the leftmost XOR gate input, and an intermediate latch

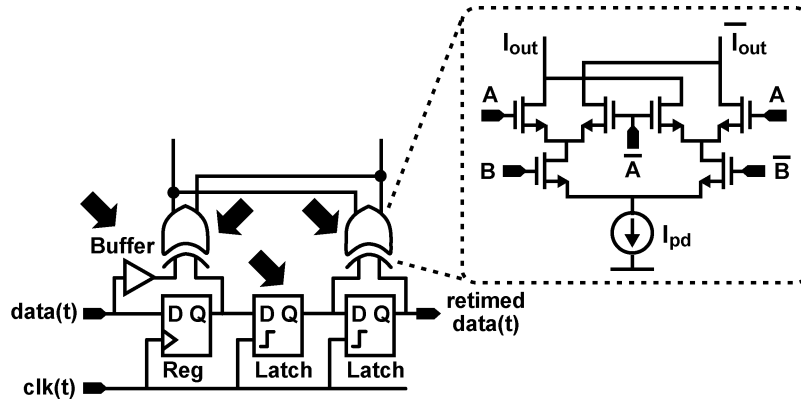


Fig. 8. Modified Hogge detector implementation to achieve low phase offset and wide linear range.

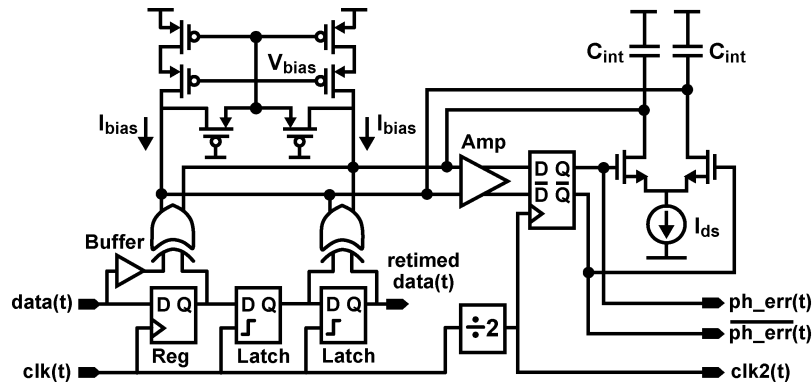


Fig. 9. Detailed diagram of proposed phase-to-digital implementation.

is inserted between the original register and latch. The buffer is designed to have a delay that compensates for the clock-to- Q delay of the first register. The function of the intermediate latch is to achieve equal loading for the register and latches which feed into the XOR gates. To achieve a wide range phase error characteristic with sufficient linearity, the Hogge charge pump, I_{pd} , is embedded within both of the XOR structures as shown in Fig. 8. By doing so, the output of the XOR gates can be directly fed into the capacitor C_{int} , which presents a low impedance at high frequencies. Therefore, a small voltage swing is achieved at all nodes which experience the frequency doubling behavior of the XOR gates, so that Miller effect issues are minimized for nodes transporting the highest frequency signals.

Fig. 9 shows a more detailed view of the overall proposed phase-to-digital converter. The quantizer charge pump consists of a simple differential pair with bias current I_{ds} , and a pMOS bias network is included to provide the required common-mode current of the combined Hogge detector and quantizer output currents. The pMOS bias network consists of cascoded current sources whose gate bias voltage is set by the common-mode feedback of two pMOS devices operating in their linear region (and thereby acting as large resistors). Appropriate layout techniques were applied to achieve good matching between each side of the pMOS bias network since mismatch would contribute to phase offset in the overall phase detection operation (in addition to phase offset caused by mismatch between the clk-to- Q delay of the leftmost register in the figure and the buffer driving the leftmost XOR gate). Such phase offset would reduce

the jitter tolerance of the CDR. Overall, the figure reveals that the proposed phase-to-digital converter adds only a few blocks compared to the basic analog Hogge design, so that high-speed phase-to-digital conversion is achieved without a significant increase in power dissipation or area compared to the classical Hogge structure.

B. VCO

Rather than using the “all-digital” VCO structure suggested in [8], we instead leverage the popular hybrid analog/digital VCO topology [9] shown in Fig. 10. In this approach, the digital switched capacitors are augmented with a classical analog varactor. Coarse frequency tuning is then performed by the digital switched capacitors, and fine frequency tuning by the analog varactor. In this design, the digital switched-capacitor array provides discrete frequency adjustment from 2.35 GHz to 2.8 GHz in order to allow operation at the required SONET FEC and non-FEC rates across all process and temperature variations, and is organized as a combination of binary and unitary codes which are segmented into coarse, medium, and fine sections. The analog varactor provides continuous frequency adjustment across 2% tuning range. Since the overall capacitance is dominated by the digital capacitors (which are designed to have high Q), the Q of the analog varactor has minimal impact on the VCO phase noise performance. In addition, since the effective K_v of the analog varactor can be made small while still achieving a reasonably wide frequency range, the impact of

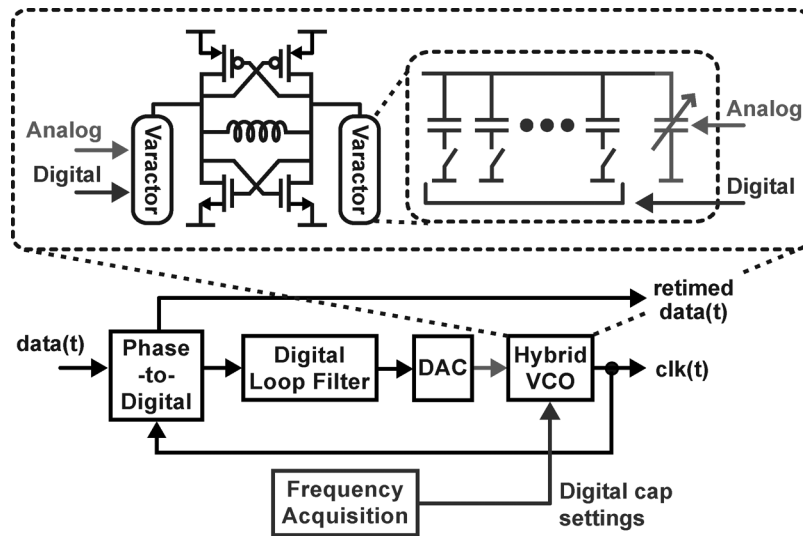


Fig. 10. Hybrid analog/digital VCO and its associated control.

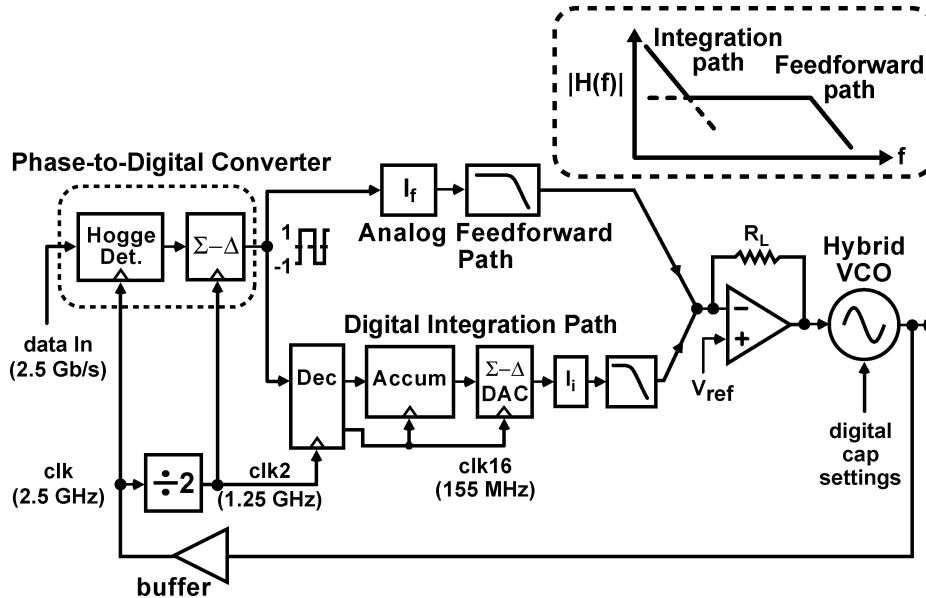


Fig. 11. Proposed hybrid analog/digital loop filter.

noise on the analog control input of the varactor is substantially reduced compared to classical analog VCO topologies.

The hybrid analog/digital topology shown in Fig. 10 offers excellent VCO phase noise and is highly amenable to integration in $0.25\text{-}\mu\text{m}$ CMOS since it avoids the need for the very small capacitor sizes required in the digital approach suggested in [8]. Of course, it has the drawback of requiring an analog signal from the loop filter, and we have already pointed out the disadvantages of using an analog loop filter topology. As indicated by Fig. 10, a digital loop filter can be used by directing its output into a digital-to-analog converter (DAC) with sufficient resolution and bandwidth. While the inclusion of this DAC would seem to undermine our goals of achieving compact area and low power dissipation, we will next describe a method to partition the loop filter into digital and analog sections such that implementation of the DAC operation is achieved without such problems.

C. Loop Filter

Fig. 11 shows the proposed hybrid analog/digital loop filter structure and its relationship to the other CDR circuit blocks. Rather than using the classical analog RC network shown in Fig. 1, the proposed structure implements an equivalent transfer function with a dual-path structure whose feedforward path is analog and integration path is digital [16].

The analog feedforward path simply consists of a charge pump I_f followed by a low-pass RC network with a bandwidth of approximately 40 MHz. This filtering is only required for suppression of the phase-to-digital quantization noise, and has minimal impact on the closed-loop dynamics of the CDR (which are set to have approximately 1-MHz bandwidth at 2.5-Gb/s operation). The analog feedforward path offers the advantage of achieving high resolution and high bandwidth without requiring a power-hungry, high-resolution, high-speed DAC to feed the analog input of the VCO.

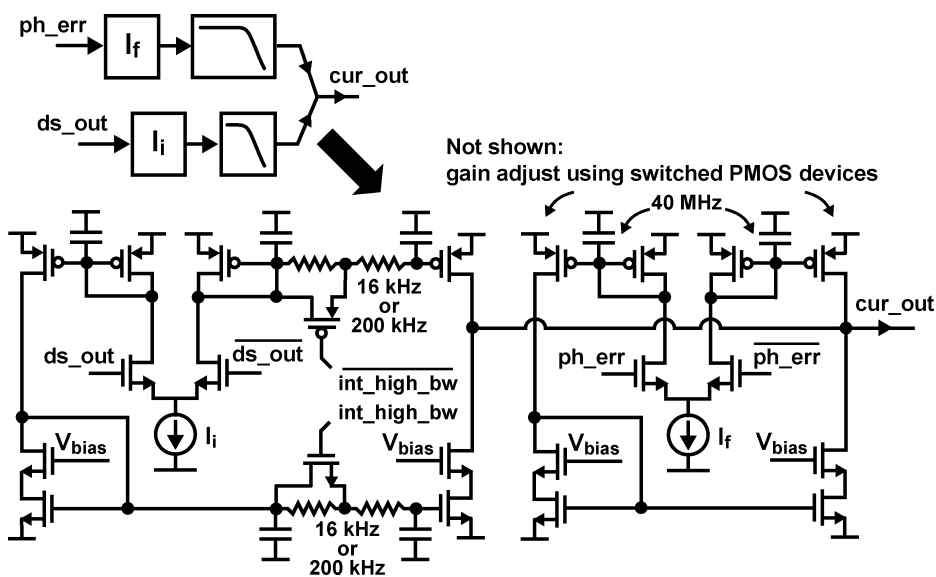


Fig. 12. Implementation of feedforward and integrating path charge pumps and RC filters.

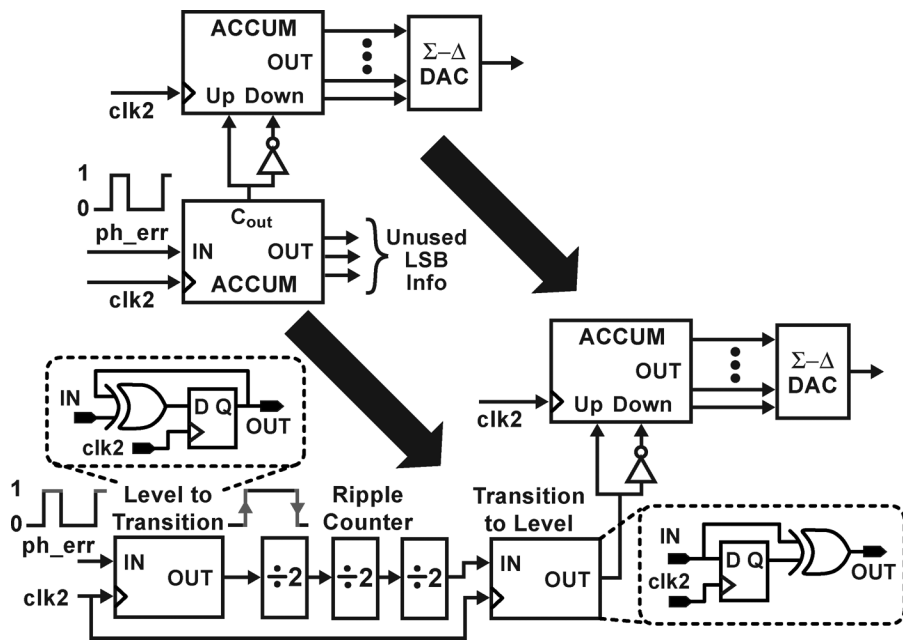


Fig. 13. Segmentation of accumulator into a ripple counter based LSB section and classic up/down counter MSB section.

The digital integration path consists of a decimator, digital accumulator, and a low-speed Sigma-Delta DAC. The decimator lowers the operating frequency of the phase-to-digital output to 155 MHz so that low-power, full-swing CMOS logic can be used to implement the digital accumulator and DAC (note that [17] incorrectly stated this frequency to be 77 MHz). The accumulator accepts the decimated phase error waveform and effectively accumulates the phase error with gain corresponding to the number of bits in the accumulator (which is 15 bits for 2.5-Gb/s operation). The Sigma-Delta DAC is an entirely digital, first-order, Sigma-Delta modulator that outputs a one-bit signal. The DAC output is smoothed by passing it into a charge pump and low-pass RC filter similar to what is used for the analog feedforward path but with a much lower bandwidth of 16 to 200 kHz. Fig. 12 shows a detailed view of the charge pumps and RC filters used within the feedforward and integrating paths.

While the digital accumulator and Sigma-Delta DAC are very common structures, the decimator is implemented in a unique fashion that we will explain in two steps. Fig. 13 displays our proposed concept of implementing the least significant portion of the digital accumulator with a ripple counter structure. The advantages of using a ripple counter are its simple structure and fast operating speed. However, it operates by counting *transitions* rather than the binary levels normally accepted by digital accumulators. This issue is resolved by adding simple level-to-transition and transition-to-level circuits at the input and output of the ripple counter, respectively, as described in [18]. A subtle point is that the least significant portion of the accumulator, as shown for either implementation in Fig. 13, essentially acts as a first-order digital Sigma-Delta modulator in conveying the phase error information to the most significant portion of the accumulator.

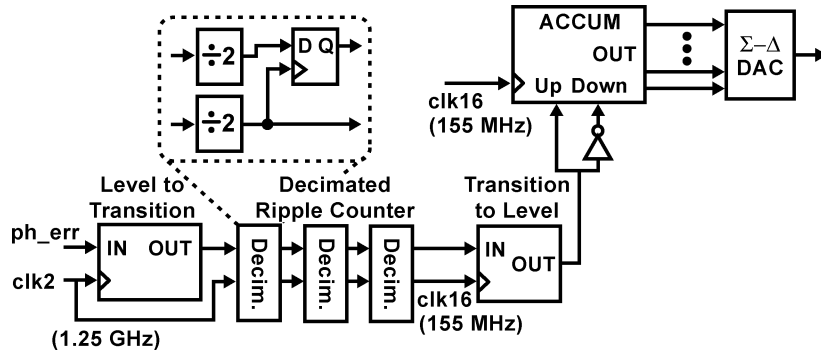


Fig. 14. Proposed decimation structure and corresponding accumulator.

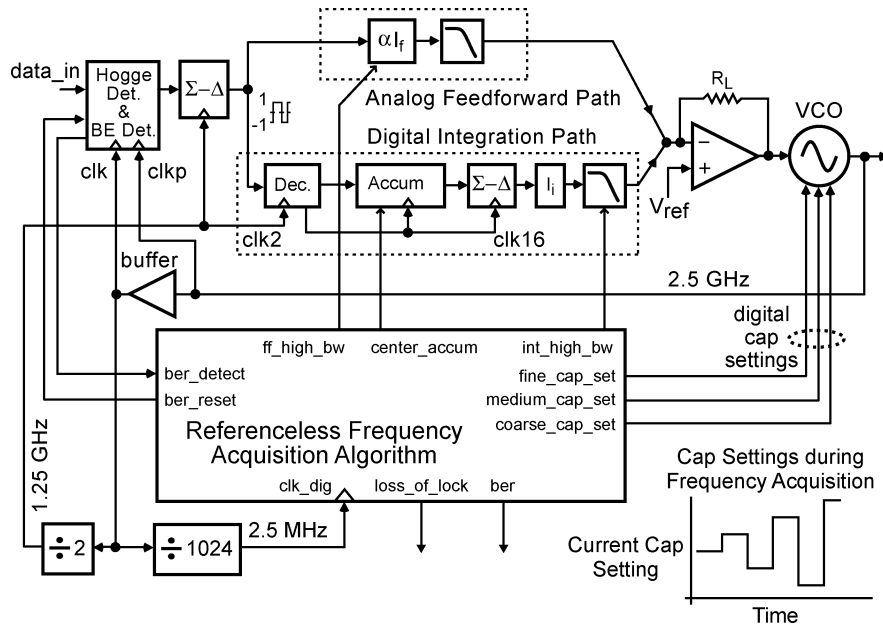


Fig. 15. Block diagram of proposed CDR with digital referenceless frequency acquisition circuits included.

The structure in Fig. 13 performs the desired accumulation operation, but does not give benefit as a decimator since it does not lower the effective operating frequency of the most significant portion of the accumulator. Fig. 14 shows how a modified version of the ripple counter accumulator leads to the desired decimation behavior. We simply insert re-clocking registers at each ripple counter stage which are clocked at progressively lower clock frequencies. The resulting structure lowers the operating frequency of the most significant portion of the accumulator and the Sigma-Delta DAC to 155 MHz, which allows straightforward implementation with standard cell logic.

D. Digital Frequency Acquisition Method

We now turn our attention to control of the digital capacitor settings of the VCO, which is achieved through the proposed digital frequency acquisition structure shown in Fig. 15. The advantages of this structure are that it performs frequency detection over the entire frequency range of the LC VCO (i.e., ±8.7% in the prototype IC), does not require quadrature VCO phases, has a purely digital implementation, and requires only a minimal number of high-speed gates. A low-speed (2.5 MHz) digital block is used to control the switch settings of the capacitor

array within the LC tank of the VCO based on information captured from a bit error detector incorporated within the phase detector. Rather than trying to determine the sign of the frequency error, the approach simply makes a binary decision with respect to whether frequency lock has been achieved at a given capacitor setting. If it is determined that frequency lock has not been achieved, then the frequency is progressively stepped up and down about the initial setting until a given setting achieves frequency lock.

Frequency steps taken during frequency acquisition must be small enough to ensure frequency locking for at least one setting. Fortunately, this value turns out to be fairly coarse in this application, so that there is a reasonably small number of possible capacitor settings that must be searched. Increasing the closed-loop bandwidth of the CDR (by increasing the mirrored charge pump current in the feedforward path via signal *ff_high_bw*) during frequency acquisition further increases the frequency lock-in range, and thereby reduces the number of capacitor settings that must be searched. The prototype system has 336 relevant capacitor settings, which leads to a worst case acquisition time of 2.7 ms (at 2.5-Gb/s data rate) if all settings must be visited.

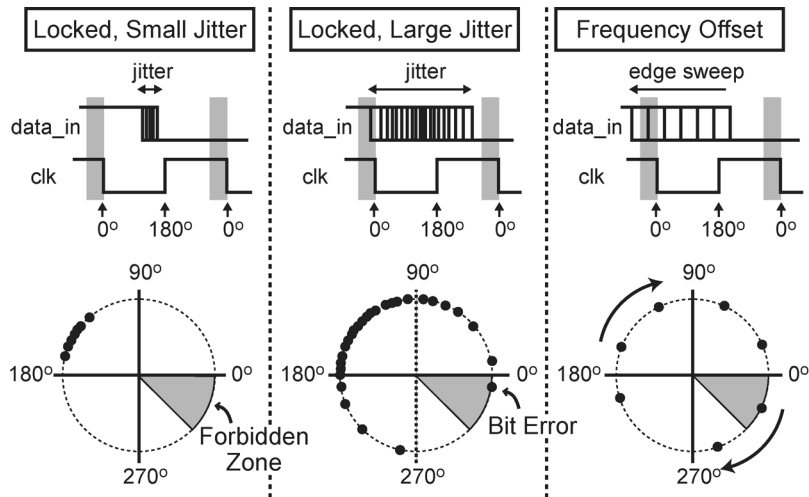


Fig. 16. Phase space view of data edge variation.

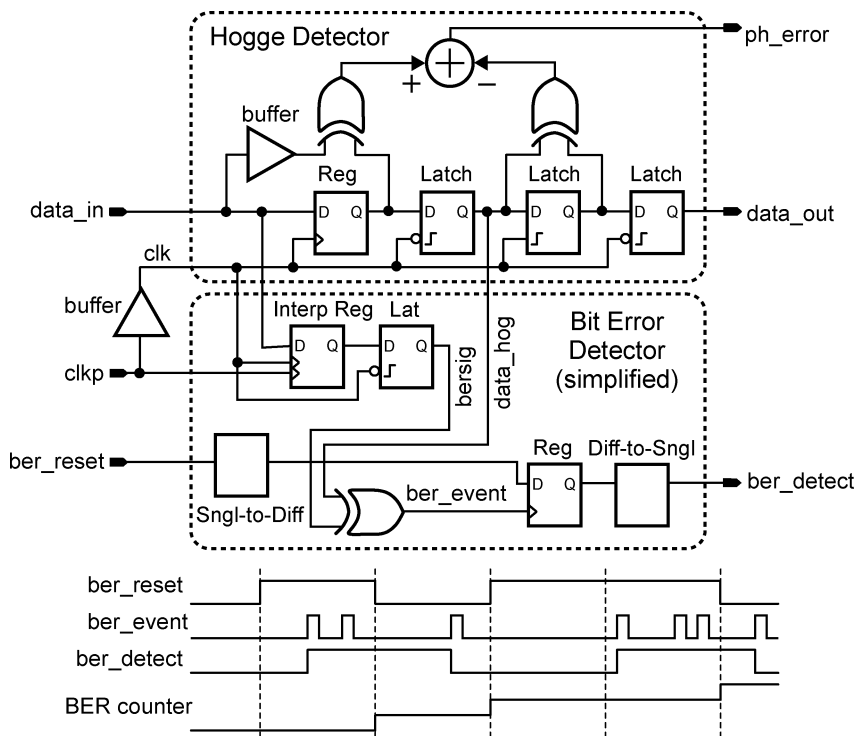


Fig. 17. Hogge detector with bit error sense.

A key idea of the proposed technique is to infer frequency lock conditions based on the observation of bit errors when retiming the data. We use a heuristic method to determine such errors based on the concepts illustrated in Fig. 16. Consider the region we call the forbidden zone as shown in the figure, and note that we assume that there is a slight offset of the data edges away from their optimal placement at 180°. Assuming that the retiming edge of the clock is at 0°, we declare data edges that enter the forbidden zone as bit error events. Under conditions of frequency lock and reasonably low jitter levels, no such bit error events occur. In such case, we can infer that the CDR is in frequency lock.

For larger levels of jitter, we can also infer the lock condition of the CDR if the number of bit error events due to jitter

is substantially smaller than what occurs when there is a frequency offset. In such case, it is necessary to count bit error events over time and then choose an appropriate threshold to decide if such events indicate a loss of lock condition. Calculation of such thresholds is achieved through statistical analysis in which bit error events are viewed as a Bernoulli process [19]. For the presented system, the frequency detection algorithm was designed to lock onto data with bit error rates (BERs) as high as 1e-3, and to stay locked with BER as high as 2e-3.

Fig. 17 displays the proposed bit error detector which implements the forbidden zone—it consists of a few logic gates that augment the previously presented Hogge phase detector. The presence of the extra gates has minimal impact on clock loading and power dissipation. Low-speed signals *ber_reset*

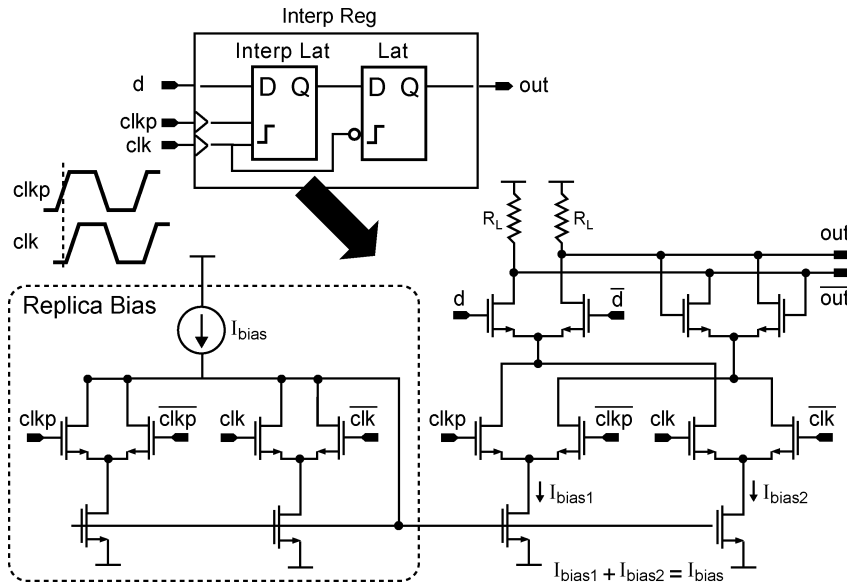


Fig. 18. Latch with interpolated clock.

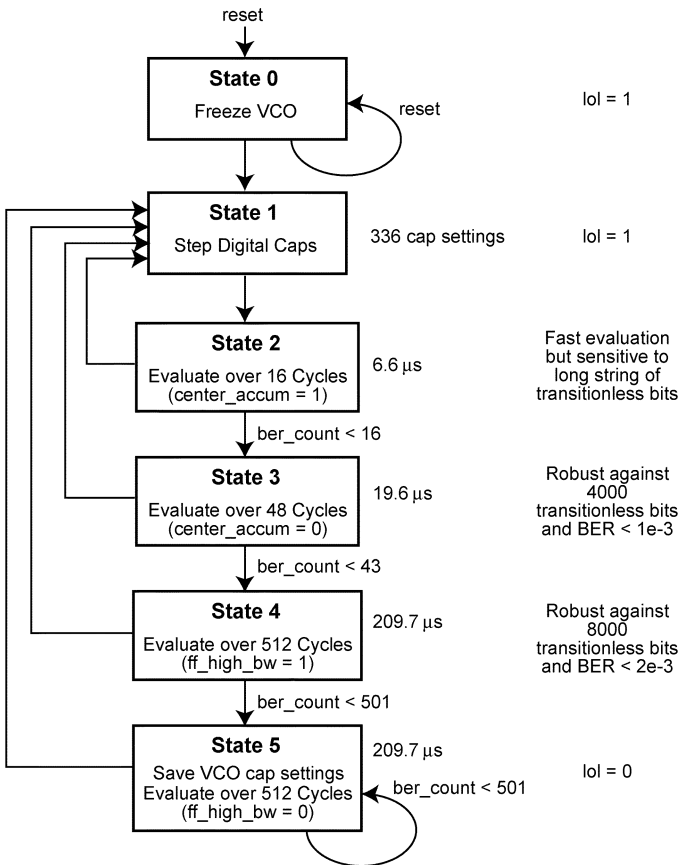


Fig. 19. State diagram of referenceless frequency acquisition algorithm.

and *ber_detect* utilize a level sensitive protocol to avoid metastability problems when interfacing to the high-speed circuits in the bit error detector.

The size of the forbidden zone is a function of the delay between *clkp* and *clk*, which are related by the buffer delay shown in Fig. 15. Unfortunately, this delay is rather long since the buffer drives all of the phase detector circuitry and therefore has

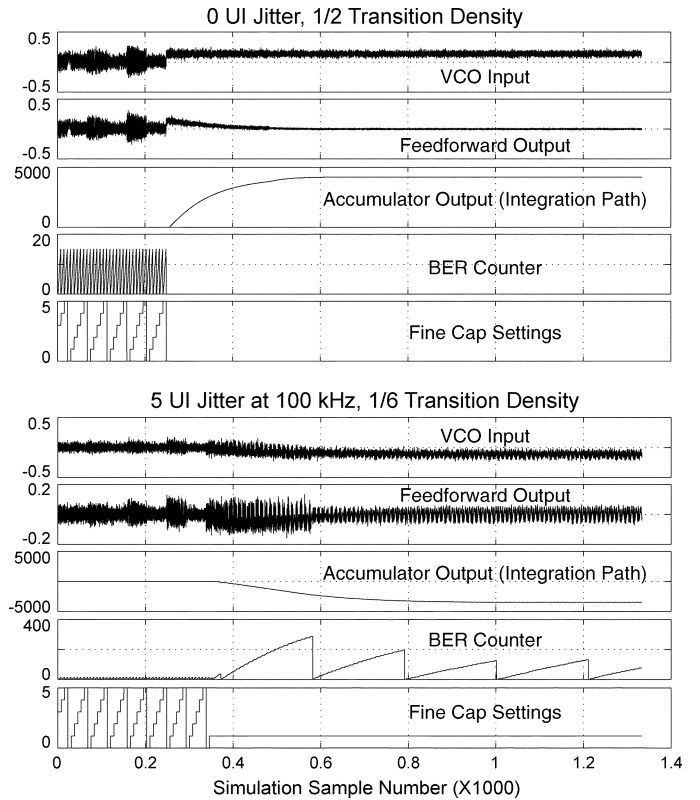


Fig. 20. Behavioral simulation of digital referenceless frequency acquisition.

relatively slow edges. We effectively shorten the delay used to realize the forbidden zone by a factor of two by interpolating between the two *clk* signals using the circuit shown in Fig. 18. The resulting decrease in the forbidden zone leads to improved jitter tolerance at 2.5-Gb/s data rate while still providing an adequately large zone to sense bit errors. Additional circuits, which are not shown, are used to increase the delay time used to form the forbidden zone at lower data rates so that its relative size compared to the increased clock period remains large enough to adequately capture bit error events (ideally, the relative size of

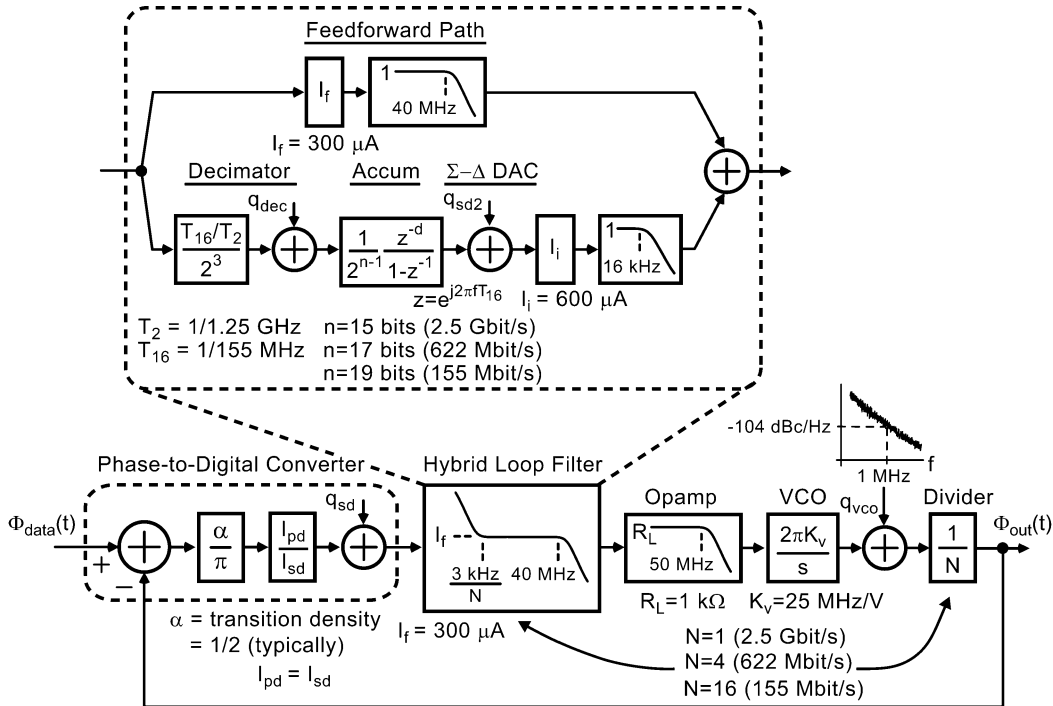


Fig. 21. Linearized model of multi-rate CDR.

the forbidden zone compared to the clock period should remain constant across all data rates).

A state diagram of the referenceless frequency acquisition algorithm is shown in Fig. 19. A key issue addressed by the algorithm is to balance the conflicting goals of quickly evaluating whether a given digital capacitor setting is invalid (so that all capacitor settings can be visited in a short time) while not unduly rejecting the right capacitor setting in the process. To accommodate this tradeoff, the time for observing bit errors is lengthened as more confidence is gained that a given capacitor setting is valid. The time values and threshold levels were chosen based on detailed statistical analysis described in [19].

Fig. 20 displays simulation results of a detailed C language behavioral model of the system shown in Fig. 15 during frequency acquisition under low and high input jitter conditions. The fine cap settings waveform displays a sweeping progression of cap values as different frequency settings are tested. Note that the medium and coarse cap settings are not shown, but are varied as shown in Fig. 15 every *cycle* of the fine cap sweep. Under low input jitter conditions, we see that the BER counter goes to zero upon reaching the proper cap setting. In the case of high jitter, the BER counter continues to experience activity after frequency lock, but the resulting accumulated values are correctly deemed to be too low to imply loss of frequency lock. The bit error counting interval becomes longer when lock is achieved, which explains why the BER counter rises in value later in the simulation. Note that the BER counter values illustrated in Fig. 20 can be used to estimate the BER of the incoming data stream [20], as shown later in this paper.

IV. MODELING

Fig. 21 shows a detailed linearized model of the CDR. Note that the impact of a high-speed divider, which was not

previously mentioned for brevity, is included to show how the closed-loop bandwidth is changed for different data rates. Signals q_{sd} , q_{dec} , and q_{sd2} correspond to the quantization noise of the phase-to-digital converter, decimator, and integrating path DAC, respectively. While these noise sources are ideally first-order noise shaped, their actual spectral profiles have significant tone content and are not well suited to analytical expression. The impact of these various quantization noise sources was therefore determined through detailed behavioral simulation, and turn out to be slightly less significant in influencing the overall CDR jitter than the VCO noise indicated in the figure. Finally, a subtle point is that the gain of the accumulator is $1/2^{n-1}$ rather than $1/2^n$, where n is the number of accumulator bits, due to the fact that the range of the accumulator is $\pm 1/2^{n-1}$ just as the range of the feedforward and integrating path charge pumps is ± 300 μ A and ± 600 μ A, respectively.

V. MEASURED RESULTS

The prototype CDR circuit exceeds all SONET performance specifications at 2.5-Gb/s, 622-Mb/s, and 155-Mb/s data rates, as well as Gigabit Ethernet specs at 1.25-Gb/s data rate. Fig. 22 displays a die photo of the CDR in 0.25- μ m CMOS, which includes several circuit structures not discussed here, including a fully integrated limit amplifier and a loss-of-signal detector. Table I summarizes the key performance metrics of the prototype IC.

In presenting the measured performance of the prototype IC, we focus on 2.5-Gb/s operation for the purpose of conciseness. Fig. 23 displays measured eye diagrams of the recovered data output of the prototype IC under best and worst case conditions—the eyes are wide open and the jitter is minimally impacted by the change in PRBS pattern and input signal am-

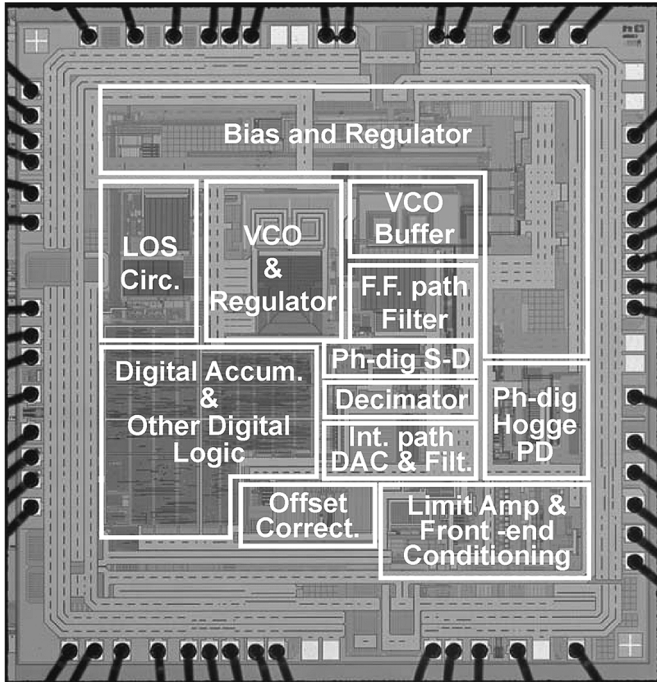


Fig. 22. Die photo of chip.

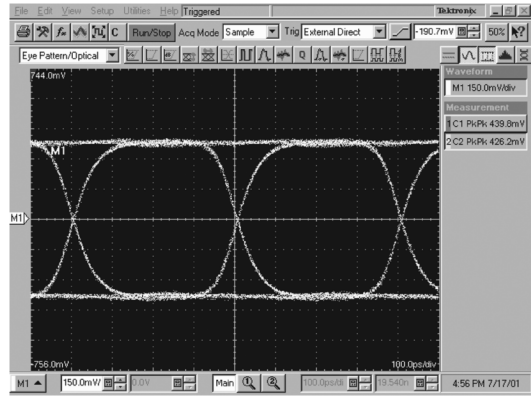
TABLE I
SUMMARY OF CDR PERFORMANCE AT 2.5 Gb/s

Specification	Typical	Max/Min	OC48 Spec.
Supply Voltage	3.3 or 2.5 V	3.5/2.4 V	
Current Consumption	170 mA	< 180 mA	
Package Area	25 mm ²		
Jitter Generation	1.2 ps	< 2 ps	< 4 ps rms
Minimum Input Swing	10 mV	10 mV	
Jitter Transfer Bandwidth	1.4 MHz	< 2 MHz	< 2 MHz
Jitter Peaking	0.03 dB	< 0.1 dB	< 0.1 dB
Jitter Tolerance (> 1 MHz)	> 0.55 UI	> 0.3 UI	> 0.15 UI

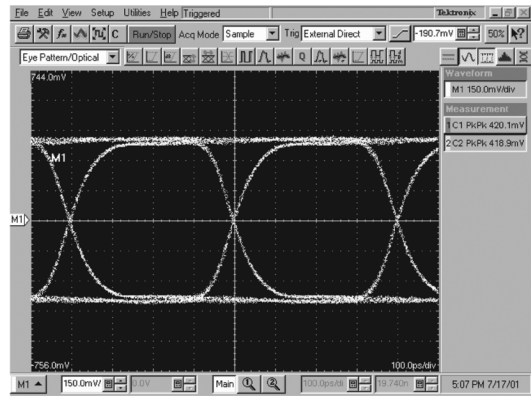
plitude. Note that the recovered data output retains the same voltage swing despite a change in input swing from 10 mV_{pp} to 2 V_{pp} due to the fact that the output signal is produced by an on-chip, clocked register fed by the retimed data output of the Hogge detector shown in Fig. 9. Also, as mentioned above, the prototype IC includes a front-end limit amplifier before the Hogge portion of the phase-to-digital converter to enable bit error rates of less than 10⁻¹² to be achieved for input signal amplitudes ranging from 10 mV_{pp} to 2 V_{pp}.

Fig. 24 displays the measured jitter transfer and tolerance performance of the CDR. The CDR exhibits jitter peaking less than 0.03 dB, which is considerably less than the SONET requirement of 0.1 dB. The measured jitter tolerance significantly exceeds SONET standards at all frequency offsets (note that the limited tolerance at low-frequency offsets is an artifact of the limited range of the test equipment).

Fig. 25 displays measured frequency acquisition of the CDR with an initial frequency value of 2.5 GHz and final value of 2.4 GHz. In this case, the frequency acquisition time was about 1.5 ms. In general, the proposed frequency acquisition algorithm has been verified to achieve correct frequency lock across the



(a) Best Case



(b) Worst Case

Fig. 23. Measured eye diagrams of the recovered data output from the CDR at 2.5 Gb/s. (a) Best case yields rms jitter of 1.2 ps with a PRBS7, 2 V_{pp} differential input signal and an ambient temperature of 25 °C. (b) Worst case yields rms jitter of 1.4 ps with a PRBS31, 10 mV_{pp} differential input signal and an ambient temperature of 100 °C.

Measured Jitter Tolerance and Transfer at 2.5Gb/s

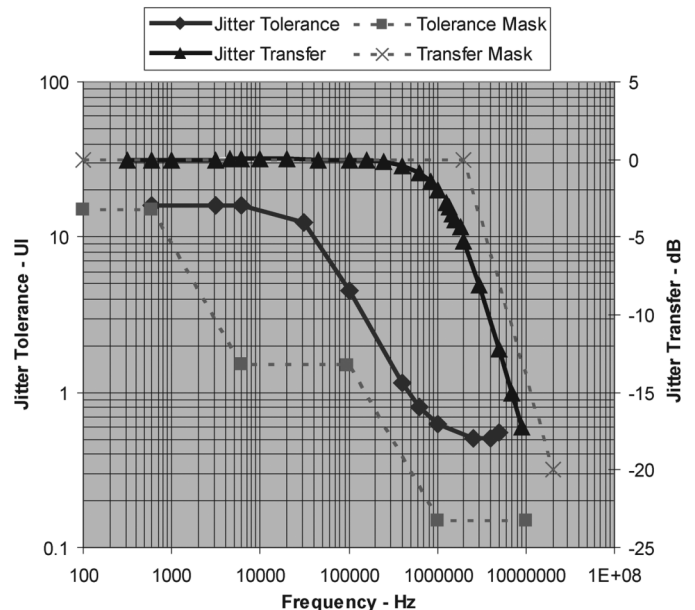


Fig. 24. Measured jitter transfer and jitter tolerance at 2.5 Gb/s.

entire ±8.7% tuning range of the LC VCO used in the prototype chip.

Fig. 25 also displays measured results of using the bit error counts from the frequency acquisition algorithm to create a BER

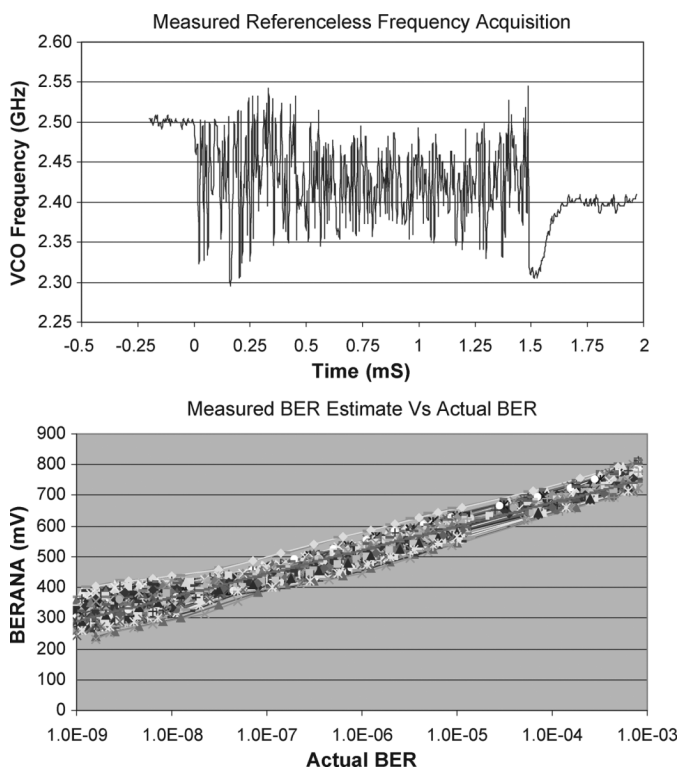


Fig. 25. Measured frequency locking example and BER estimation at 2.5 Gb/s.

monitor for the chip. The various curves correspond to measurements taken across worst case split lot corners, a temperature range of -40°C to 85°C , and a voltage supply variation of 1.62 to 3.63 V. Given the extreme conditions exercised in these measurements, we see that the approach leads to quite accurate prediction of the actual BER.

VI. CONCLUSION

A mixed-signal CDR architecture was presented in this paper which leverages unique boundaries between analog and digital circuits to realize a high-performance design with compact area and low power dissipation. In particular, the proposed architecture achieves a linear, compact, and low-power phase-to-digital converter and a fully integrated loop filter that simultaneously achieves a wide bandwidth filter response and an easily configurable, low-frequency zero without the need for a large capacitor value. In addition, an all-digital, referenceless frequency acquisition approach was presented that takes advantage of the ability of digital circuits to perform complex algorithms to achieve frequency acquisition without the need for quadrature VCO phases or significant high-frequency circuits, and to also enable estimation of the BER rate of the CDR. The overall CDR architecture achieves multi-rate operation supporting 155-, 622-, 1250-, and 2500-Mb/s data rates in $0.25\text{-}\mu\text{m}$ CMOS, provides high-performance operation greatly exceeding SONET requirements, fits into a small 5×5 mm package, and dramatically simplifies board design due to the elimination of sensitive noise entry points at package pins by achieving full integration of the loop filter.

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