A 78 dB SNDR 87 mW 20 MHz Bandwidth Continuous-Time $\Delta\Sigma$ ADC With VCO-Based Integrator and Quantizer Implemented in 0.13 μm CMOS

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Abstract—The use of a VCO-based integrator and quantizer within a continuous-time (CT) $\Delta\Sigma$ analog-to-digital converter (ADC) structure is explored, and a custom prototype in a 0.13 μm CMOS with a measured performance of 81.2/78.1 dB SNR/SNDR over a 20 MHz bandwidth while consuming 87 mW from a 1.5 V supply and occupying an active area of 0.45 mm^2 demonstrated. A key innovation is the explicit use of the oscillator's output phase to avoid the signal distortion that had severely limited the performance of earlier VCO-based ADCs, which had made use of its output frequency only. The proposed VCO-based integrator and quantizer structure enables fourth-order noise shaping with only three opamp-based integrators.

Index Terms—Analog-to-digital conversion, quantizer, ring-oscillator, VCO-based, voltage-controlled oscillator (VCO), $\Delta\Sigma$.

I. INTRODUCTION

A S wireless communication continues to advance, next generation transceiver architectures must contend with a variety of implementation challenges, including multi-standard support and wide bandwidth to meet the demand for higher data rates. An attractive architecture to achieve these goals on the receiver side is shown in Fig. 1, which comprises an LNA and IQ Mixer feeding into a wide bandwidth, high resolution analog-to-digital converter (ADC) that has minimal antialias filtering requirements. Channel selective filtering can then be performed in the digital domain, which greatly simplifies multi-standard support. To achieve good receiver sensitivity and blocking performance with minimal antialias filtering, the ADC must have wide dynamic range and excellent SNDR characteristics.

A promising ADC structure to fulfill the above requirements is the continuous-time (CT) $\Delta\Sigma$ topology with multi-bit quantizer, shown in basic form in Fig. 2. The benefit of $\Delta\Sigma$ modulation is that it allows much higher effective resolution than provided by the multi-bit quantizer on its own due to the noise
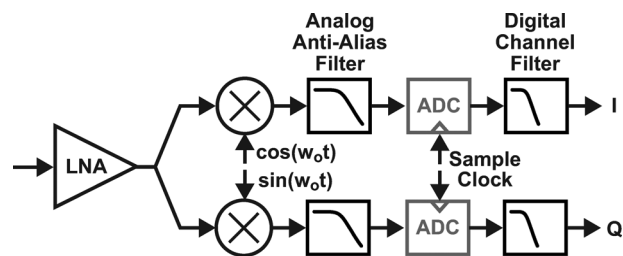

Fig. 1. A wideband wireless transceiver leveraging a wideband A/D to achieve multi-mode operation.
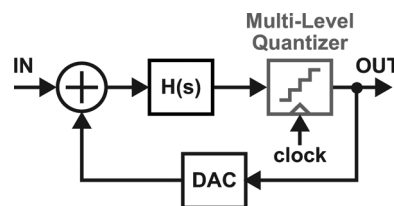

Fig. 2. A basic continuous-time Sigma-Delta ADC structure.

shaping achieved through feedback [24]. The advantage of a CT structure is that the sampling operation is performed by the multi-level quantizer *after* the input signal has passed through a lowpass filter $H(s)$. In effect, $H(s)$ acts as an antialias filter, which greatly reduces the amount of pre-filtering needed before feeding the input signal into the ADC. Since considerable power and area are often spent on such filtering in common receiver architectures, reduction of this filtering requirement is a key benefit of this structure.

Due to these advantages, the mixed-signal community has been actively researching CT $\Delta\Sigma$ ADC structures [12]–[15], [19]–[21], [26]–[31]. Our contribution to this effort is to highlight the benefits of using a VCO-based quantizer to implement the multi-bit quantizer within the CT $\Delta\Sigma$ structure. While other works have demonstrated the use of VCO-based quantization in $\Delta\Sigma$ structures [3]–[5], [7], [32], [33], we will point out that the nonlinear voltage-to-frequency characteristic of a practical VCO-based quantizer presents a significant challenge in achieving high SNDR with wide bandwidth [3]–[7], [32], [33]. We will show that using phase as the key quantizer output signal rather than frequency virtually eliminates the impact of such nonlinearity, and thereby opens the door to high SNDR

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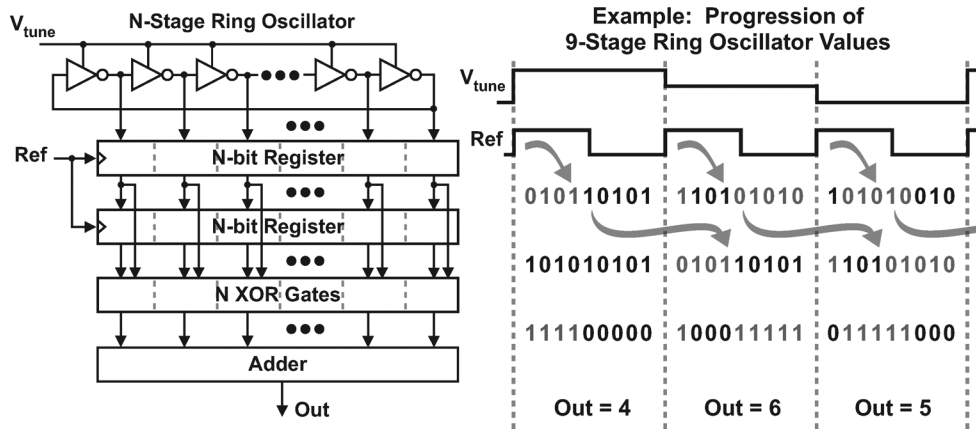
Fig. 3. An efficient VCO-based quantizer implementation for high frequency sample rates.

performance. Using this technique, our ADC prototype demonstrates 78 dB SNDR over a 20 MHz bandwidth with relatively low area of 0.45 mm^2 and power consumption of 87 mW in 0.13 um CMOS.

We begin in Section II with a brief review of key issues related to VCO-based quantizers designed for high speed sampling applications, including a basic implementation, its benefits compared to classical multi-bit quantizers, and a simple frequency domain model. We also quickly review recent work in utilizing such a VCO-based quantizer within a CT $\Delta\Sigma$ ADC structure and the performance that was achieved. In Section III, we introduce the proposed architecture, illustrate the advantage of using phase rather than frequency as the key quantizer variable, and discuss the implications of this choice for the overall ADC topology. Detailed behavioral simulations indicate the achievable SNDR for the proposed ADC structure assuming reasonable circuit non-idealities, and reveal that the impact of the VCO-quantizer nonlinearity is insignificant when using phase as the key output variable. Circuit implementation details of the key ADC blocks are provided in Section IV, and the actual measured performance of the ADC prototype discussed in Section V. Section VI provides a brief discussion of potential architectural improvements, and Section VII closes with a summary of the key points of the paper.

II. BACKGROUND

VCO-based quantization has become a topic of great interest due to the unique and attractive signal-processing properties it offers in the design of oversampling converters. This section describes the basic operation of a VCO-based quantizer, and reviews the structure's merits over classical multi-bit quantization.

A. Basics of Implementation

Fig. 3 shows an efficient VCO-based quantizer implementation amenable to very high sample rates [3], [7], [32], [33]. The key concept is to count the number of edges that travel through an N-stage ring oscillator within each period of a reference clock, which vary in rate according to the analog tuning input, V_{tune}. While numerous methods of counting the edges exist [3]–[9], the method illustrated in Fig. 3 processes samples

of the quantized oscillator phase obtained by directing the outputs of each delay stage into a set of registers that are clocked by the reference clock. The quantized phase values are then XOR'd with the phase values of the previous samples, producing a binary sequence with a series of 1's corresponding to the number of edges that traversed the oscillator between reference clock edges. A final count value is obtained by adding the number of 1's together, which provides a digital representation of the analog input, V_{tune}. The topology assumes that the number of edges traveling through the oscillator during one reference period never exceeds the number of ring oscillator stages. Stated a different way, the ring oscillator frequency range should be designed such that it remains less than half of the reference clock frequency. Note that this constraint could be broken if extra logic kept track of phase wrapping, but this would result in a more complicated structure.

To understand the advantages of the VCO-based quantizer over a classical multi-bit quantizer, Fig. 4 illustrates the significant details of each topology. The classical topology operates in the voltage signal domain, and achieves multiple quantization levels by dividing a reference supply voltage, Vdd, into Vdd/N increments via a resistor ladder with N sections. As Vdd/N shrinks with increasing number of quantization steps, the likelihood of generating metastable events on one or more comparators at a given sample time increases. Since the quantizer output bits drive the feedback DAC unit elements in a $\Delta\Sigma$ ADC, such metastable events can be a corrupting influence on the performance of the feedback DAC, and thereby degrade the SNR of the overall ADC. This issue, along with possible mismatch and offset concerns, typically leads to the use of low offset pre-amps for the classical quantizer which often consume relatively large area and power in order to achieve low offset voltages and high speed operation.

In contrast, a VCO-based quantizer, as shown in Fig. 4(b), works with time as its key signal, and achieves multiple quantization levels by leveraging the variable delays of the voltage-controlled ring oscillator stages. The oscillator effectively translates the input voltage to a time signal through its voltage-to-frequency characteristic—high input voltages translate to higher oscillator frequencies and, therefore, shorter delays, and low input voltages translate to lower oscillator
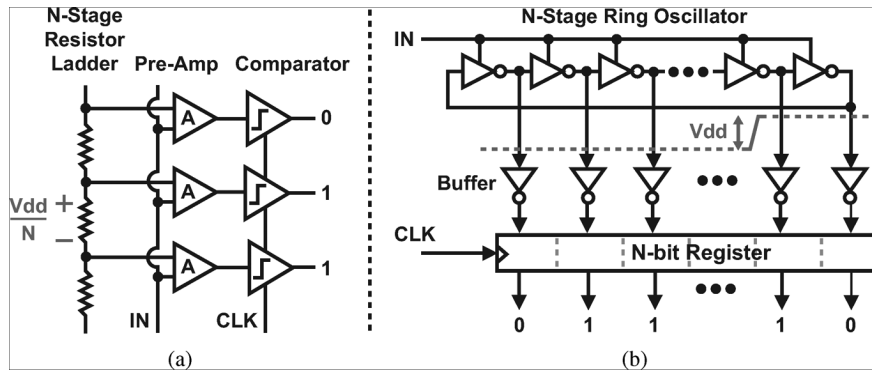
Fig. 4. Comparison of (a) classical multi-bit quantizer versus (b) VCO-based quantizer.

frequencies and, therefore, longer delays. A quantized version of the voltage input is then obtained by counting the number of edges that transition in a given reference clock period.

The VCO-based quantizer offers area and power consumption advantages over its classical counterpart when seeking high sample frequencies. As shown in the figure, the output voltages of the oscillator delay stages will, to first order, saturate to either supply or ground with the exception of the delay stage output that is in transition. Within reasonable limits, this unique output signal property remains true as the number of delay stages increases. As a result, the number of quantization levels can be increased without similarly increasing the likelihood of generating metastable events on the comparators. Also, the full swing signal levels offered by the delay stage outputs allow replacement of the relatively large, power consuming pre-amps that are often used in classical quantizers with inverters that simply isolate the ring oscillator from charge glitches incurred as the register is clocked. Indeed, the entire VCO-based quantizer can be very compact and achieve high speed operation without requiring high power consumption.

In terms of mismatch, the VCO-based quantizer offers a subtle advantage due to the manner in which edges propagate through the delay stages in consecutive periods. As shown in Fig. 5, the VCO-based quantizer dynamically shuffles through delay stages in a barrel shift fashion as the measurement of edges in each reference period progress. In the case where *frequency* is the output variable of the quantizer, such as in the topology shown in Fig. 3, the benefit of this action is that mismatch in delay across the stages is effectively first order noise shaped [7]. Indeed, the barrel shift pattern and the resulting noise shaping property are identical to the output pattern generated by the data weighted averaging (DWA) DEM algorithm described in [37]. This shaping action greatly alleviates concern for mismatch in the design of the quantizer. As we will discuss in Section III, one negative tradeoff in using *phase* as the key output variable will be a loss of this first order shaping of delay mismatch.

B. Modeling

Fig. 6 shows the equivalent frequency domain model of the VCO-based quantizer from Fig. 3. The ring oscillator is modeled as an integrator from voltage input to output phase, the sampling register (i.e., Quantizer) is modeled as a scale factor
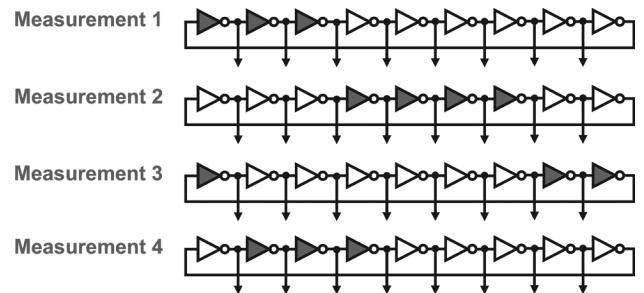

Fig. 5. Movement of edges within ring oscillator across consecutive measurement intervals corresponding to reference edges.
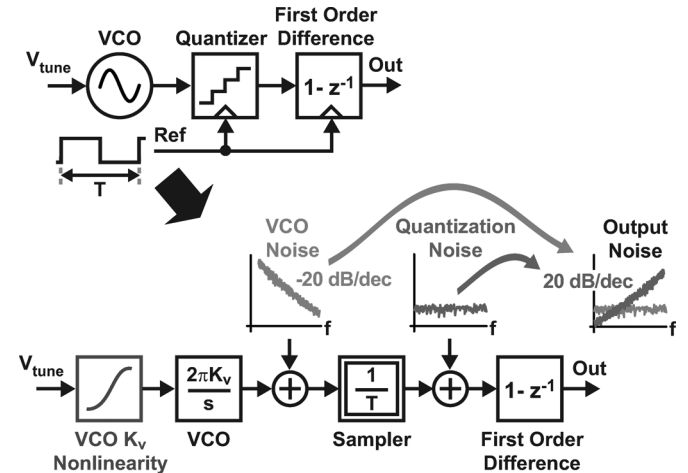

Fig. 6. A basic continuous-time Sigma-Delta ADC structure.

according to the sampling frequency, $1/T$, and the XOR operation between current and previous phase samples is modeled as a first order difference operation. In general, the XOR operation does not yield a first order difference operation for arbitrary inputs, but does so in this case since the VCO phase monotonically increases as a function of time.

A crucial insight from Fig. 6 is that the key output variable is proportional to the frequency of the oscillator (i.e., number of edges per reference period). To see this relationship, note that the input voltage, V_{tune}, changes the oscillator frequency. The quantizer essentially samples the oscillator phase, which corresponds to the *integral* of frequency. The first order difference
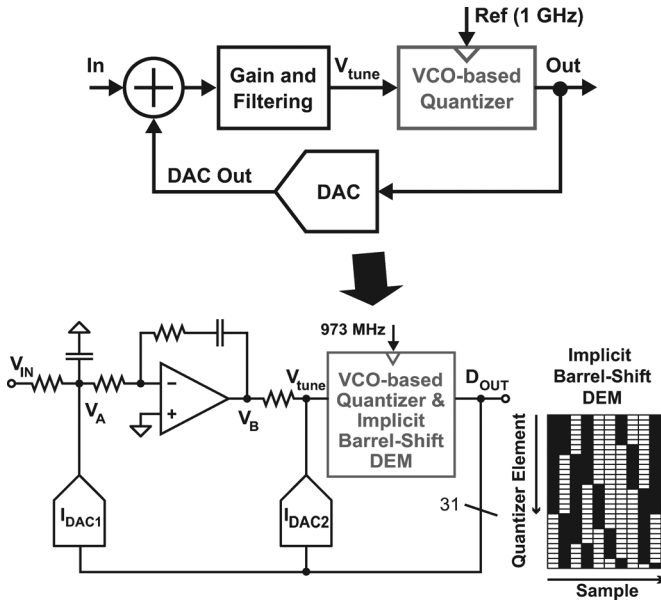
Fig. 7. A basic CT ΔΣ ADC structure using a VCO-based quantizer and a recent implementation [7].

then converts the sampled phase back to a scaled version of frequency.

As indicated in Fig. 6, there are three key non-idealities presented by the VCO-based quantizer: Kv nonlinearity, VCO phase noise, and quantization noise. Kv nonlinearity corresponds to the nonlinear voltage-to-frequency characteristic of the oscillator and VCO phase noise corresponds to the accumulated effect of thermal (and 1/f noise) in the devices that comprise the delay stages. For the sake of simplicity, the VCO phase noise is shown to have a −20 dB/decade slope, but in reality a steeper slope will occur at low frequency offsets due to the impact of 1/f noise, and a noise floor will occur at high frequency offsets. Finally, quantization noise is a byproduct of any quantizer implementation, and is typically modeled as white noise. Since frequency is the key output variable (as assumed in Fig. 6), a salient feature of the VCO-based quantizer is that the first-order difference operation will shape the quantization noise to high frequencies. VCO phase noise then becomes the dominant noise source at low frequency offsets.

C. Embedding the VCO-Based Quantizer Within a Continuous-Time ADC

In principle, the VCO-based quantizer can be used directly as a basic ADC structure, and has been shown to be useful in applications where only modest SNDR performance is sufficient [3], [6], [8], [32], [33]. As revealed by Fig. 6, the structure lends itself best to oversampled applications that use decimation filters to remove much of the high frequency quantization noise, leaving Kv nonlinearity and VCO phase noise as the primary sources of non-ideality.

To further improve SNDR performance, it is useful to place the quantizer within a feedback loop, as shown in the CT ΔΣ ADC structure of Fig. 7. The presence of open loop gain prior to the quantizer acts to reduce the impact of both the Kv nonlinearity and VCO phase noise of the quantizer.

A recent implementation, shown in the bottom half of Fig. 7 [7], utilized the aforementioned approach to achieve 72 dB SNDR in 10 MHz bandwidth (and 67 dB in 20 MHz bandwidth). Since the VCO-based quantizer provides first order noise shaping, the overall ADC was able to achieve third order noise shaping with only a second order loop filter (where the two poles are formed by the current DAC into capacitance at node V_A, and an opamp integrator). Also, the barrel shifting property of the VCO-based quantizer shown in Fig. 5 was used to achieve implicit first-order shaping of the DAC unit elements, obviating the need for an explicit dynamic element matching (DEM) circuit [10]. While the architecture achieved 86 dB in SNR in the 10 MHz bandwidth, the SNDR was limited to just 72 dB due to the Kv nonlinearity of the VCO. As such, the Kv nonlinearity stands as the chief bottleneck to achieving higher SNDR.

III. PROPOSED APPROACH

The previous section revealed that Kv nonlinearity poses a severe challenge toward achieving high converter SNDR for applications that embed the VCO-based quantizer within a CT ΔΣ ADC structure. To overcome this obstacle, we propose using phase rather than frequency as the key output variable of the quantizer. To illustrate this idea, consider the two first-order ΔΣ structures shown in Fig. 8. The top portion of the figure shows a classical VCO-based quantizer as discussed in Section II, and the bottom portion shows a feedback loop in which the quantizer phase is compared to a reference phase, and the resulting error is fed back through a DAC to the input of the feedback loop. Effectively, this feedback loop corresponds to a first-order CT ΔΣ ADC loop, and contains an integrator with infinite DC gain (as supplied by the VCO). Interestingly, it can also be viewed as a phase locked loop (PLL) in which phase error is quantized.

Note that the characteristics of the output code generated by the proposed phase-output VCO-based quantizer will depend on the ratio of the nominal oscillation frequency of the VCO and reference frequency (which should be set equal to each other) to the ADC sample rate (i.e., the quantizer clock frequency). For example, when the oscillation and reference frequencies are half of the ADC sample rate, as shown in Fig. 9(a), the XOR phase detector array outputs a conventional thermometer code with a fixed ordering corresponding to the magnitude of the quantized signal. However, when the nominal oscillation and reference frequencies are a quarter of the ADC sample rate, as shown in Fig. 9(b), the resulting thermometer code toggles about the midpoint of the code. In either of these cases, the barrel-shifting output pattern (as shown in Fig. 5) that had accompanied the frequency-output VCO-based quantizer (as shown in Figs. 3 and 8(a)) is lost. Unfortunately, the loss of barrel-shifting also leads to a loss in first-order shaping of the VCO delay stage mismatch and intrinsic DEM sequence generation for any DAC circuit that is directly connected to the quantizer (as done in [7], [10]). However, when high SNDR is desired, the improvement in ADC linearity achieved by using phase as the quantizer output variable outweighs this negative issue. For the prototype presented in this paper, the nominal oscillation and reference frequencies were chosen to be a quarter, rather than half, of the ADC sample rate
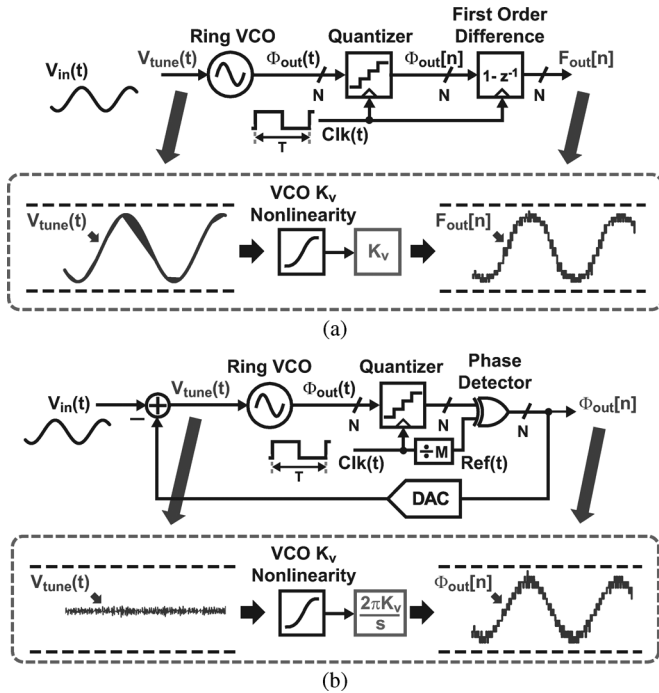
Fig. 8. (a) Classical use of frequency as the key signal versus (b) proposed approach of using phase as the key signal.

in order to simplify design of the oscillator and accompanying logic since lower speeds are easier to implement.

While both structures in Fig. 8 offer first order noise shaping of quantization noise, notice that the tuning voltage of the classical quantizer structure needs to swing over a very wide range in order to exercise the full dynamic range of the quantizer. However, since phase is the *integral* of frequency, the tuning voltage of the phase-based quantizer can be confined to a very small operating region while still enabling a complete exercise of its dynamic range. As such, the impact of the Kv nonlinearity is substantially reduced by using phase as the output variable. Behavioral simulations [34], as shown in Fig. 10, indicate that even in this simple first order example, harmonic distortion arising from this nonlinearity can be essentially eliminated under practical operating conditions of the ADC. Note that in practice, thermal noise, DAC mismatch, and other noise and error terms will add on top of the quantization noise floor and further degrade SNDR.

In order to achieve our performance target of around 80 dB SNDR, it is necessary to achieve higher order quantization noise shaping by extending the loop filter beyond first-order. The following sections will introduce the chosen fourth order loop-filter topology, as well as summarize the anticipated converter performance based on behavioral simulation analysis.

A. Implemented Fourth-Order CT $\Delta\Sigma$ Loop Filter

A fourth-order loop filter was chosen since it allows a generous margin in terms of quantization noise impact, with a SQNR of $\sim$95 dB achievable in 20 MHz BW. Traditionally, such a high-order loop filter would be implemented using a cascade of integrators and feed-forward paths, with summation of all signals occurring at the input of the quantizer as shown in

Fig. 11(a). This architecture has the advantage of enabling easy compensation of feedback loop delay by using an additional feedback DAC around the quantizer to obtain the desired loop filter impulse response [13].

Unfortunately, the proposed phase-based quantizer necessarily includes integration as part of its structure, which precludes direct implementation of the topology shown in Fig. 11(a). However, there is a relatively easy fix to this issue. As shown in Fig. 11(b), the presence of the quantizer integrator can be accommodated by replacing one of the feedforward paths with an additional DAC feedback path, modifying the feedforward coefficients, and performing signal summation at the input of the final integrator of the loop filter. At the same time, loop delay compensation can still be accomplished by differentiating the quantizer output, and then integrating the result using the same final integrator. In the case of the VCO quantizer, the derivative corresponds to its frequency, and is easily obtained by performing a first-order difference using XOR gates as described in Section II. Consequently, the loop delay compensating DAC will have its unit element mismatch noise shaped by the barrel shifting action illustrated in Fig. 5. Also, the delay compensating DAC is implemented as a return-to-zero (RZ) DAC in order to absorb the propagation delays of the quantizer and first-order difference logic [12].

A block diagram for the proposed fourth order loop filter with feedforward and feedback stabilization is shown in Fig. 12. The coefficients for the filter were chosen using the MATLAB $\Delta\Sigma$ Toolbox [11]. Since the toolbox returns coefficients for a DT filter, the equivalent CT loop filter coefficients were obtained by applying the "d2c" (discrete-time to continuous-time transformation) function available in the MATLAB Signal Processing Toolbox.

The loop filter schematic is shown in Fig. 13. Opamp-RC integrators were chosen over Gm-C integrators for their higher linearity and ability to more easily drive resistive loads. Each integrator comprises a fixed capacitance and a 5-bit binary weighted capacitor bank, which enables the RC time-constant to be tuned in 5% steps over the combined resistor and capacitor process variation of $+/-40\%$. An additional amplifier is eliminated by using passive resistors to perform the summation of the main signal path, feedforward path, and minor-loop feedback path. Since a parasitic pole formed by the summing node resistance and the wire and device capacitances from the VCO and feedback DACs can degrade loop stability, the summing node resistance is chosen low enough so that the additional phase lag from the parasitic pole is minimal.

B. Theoretically Achievable Performance

Evaluation of the theoretically achievable performance of the proposed CT $\Delta\Sigma$ ADC architecture was accomplished with the help of CppSim, a C++ behavioral simulator [17]. Fig. 14 shows the simulated output spectra of the ADC assuming a 900 MHz sample rate $(\mathrm{OSR} = 22.5)$ and a 2 MHz -2.5 dBFS input tone. The behavioral model includes a variety of non-idealities such as thermal noise of analog components, finite amplifier gain-bandwidth, VCO Kv nonlinearity, unit element mismatch, DAC ISI, and more. The values of these non-idealities were determined from detailed Spectre simulations of the various
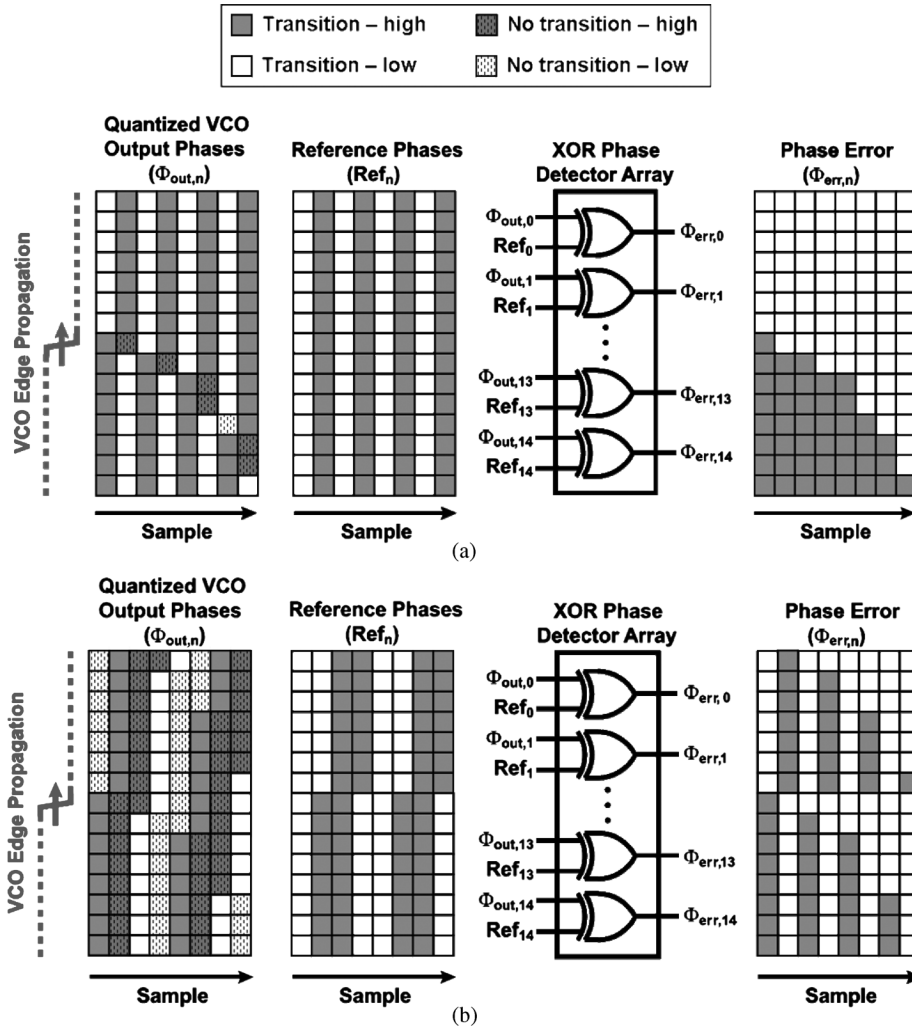
Fig. 9. Input and output thermometer-codes for the XOR-based phase detection scheme of the proposed phase-output VCO-based ADC assuming the same input Vin(t), but differing reference and nominal VCO oscillation frequencies of (a) Fs/2 and (b) Fs/4. In the quantized VCO output phase columns, the VCO edge propagates upwards and wraps around to the bottom. A gray square represents a transition to a high output state, while a white indicates a transition to a low state. A cross-hatched gray or white square indicates that the output state has not changed from the prior sample.

ADC component blocks. As these results reveal, Kv nonlinearity is insignificant even when targeted SNDR performance approaches 85 dB. A detailed explanation of the behavioral model can be found in [2], and the model can be downloaded at [34].

IV. CIRCUIT DETAILS

This section describes the key circuits used in the prototype ADC. The power intensive analog blocks are introduced first, with the most crucial element toward achieving high performance—the DAC—highlighted. The digital blocks are described next, with particular attention paid to the specific implementation of the phase-output VCO-quantizer.

A. Operational Amplifier

The 0.13 μm CMOS technology used for the prototype presents a few challenges to the design of amplifiers, including low supply voltage, high flicker noise content, and low intrinsic gain. At the same time, the opamp unity-gain bandwidth should be at least 4 times the ADC sample rate in order to minimize

quantization noise folding arising from amplifier nonlinearity [34]. Given the proposed architecture's nominal ADC clock frequency of 900 MHz, an amplifier unity-gain bandwidth of 3.5–4 GHz is needed.

Fortunately, multi-stage amplifiers comprising three or more stages (also called nested Miller amplifiers) have been successfully implemented in prior high-speed CT $\Delta\Sigma$ ADC architectures to achieve the opamp gain and bandwidth requirements [23]. An opamp similar to the 4-stage amplifier proposed in [12] was adopted, and is shown in Fig. 15. Here, high DC gain is obtained by cascading four nMOS differential pairs loaded by cascoded pMOS current sources. Stability is ensured by the inclusion of two feed-forward paths, which introduce left-half plane zeros that compensate for the additional poles of the cascaded gain stages. The last feed-forward stage that drives the class A output stage is essentially a two-stage opamp, and will primarily determine the unity-gain bandwidth and phase margin of the overall amplifier [35].

The three left-most differential input pairs shown in Fig. 15 use a device length that is 1.5-times greater than minimum
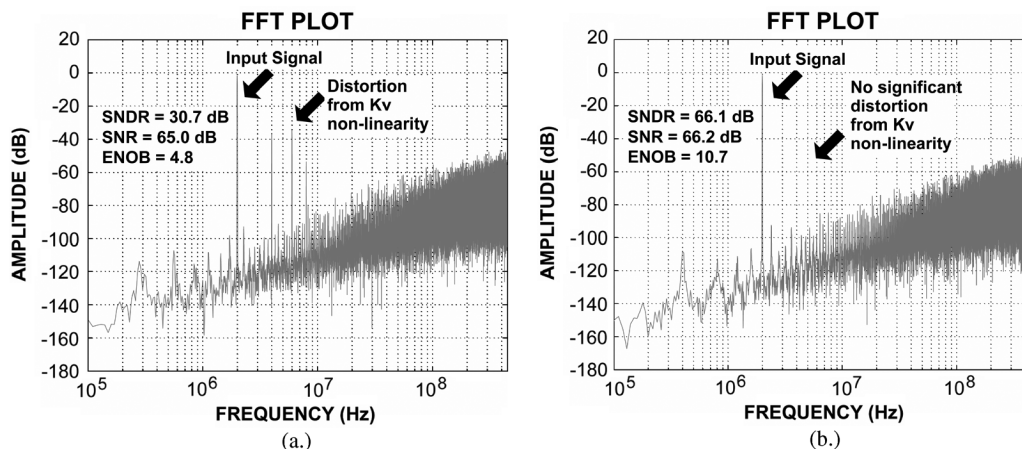
Fig. 10. FFTs from behavioral simulations of the VCO quantizer architectures shown in Fig. 8 assuming (a) frequency output, and (b) phase output. SNDR is calculated assuming a 20 MHz bandwidth, a −1 dBFS input signal at 2 MHz, a sample rate of 1 GHz, and a 31-stage ring-VCO structure with Kv nonlinearity modeled as a fourth order polynomial.

length in order to obtain higher intrinsic gain and lower flicker noise. However, the last feed-forward stage and the class A output stage use minimum length devices in order to achieve the desired high unity-gain bandwidth and phase margin. Device noise from these later stages is not a major concern as it is largely suppressed by the gain of the preceding stages.

In order to lower the noise from the first opamp in the loop filter, which will dominate over the noise of the following amplifiers, it consumes the most power at approximately 22.5 mW (the second and third opamps consume half as much). A 1.5 V supply was chosen over the nominal 1.2 V supply in order to relax the amplifier's headroom constraints, and thereby improve its overall linearity. This choice is acceptable since 1.5 V is still within the nominal long-term reliability specification of the fabrication process used for the prototype. Within the opamp structure, the power is essentially divided between the first stage input pair and the class A output pair. High currents in the class A stage are needed not only to drive the resistive loads at the output, but also to ensure that the parasitic pole induced by the effective output load capacitance does not significantly degrade the overall amplifier phase margin. This load capacitance is especially large for the first opamp due to the substantial capacitance of the opamp's input devices (>1 pF) and the wiring and device capacitance of the main DAC (>300 fF).

A summary of the simulated gain, bandwidth, noise, and power dissipation for the first opamp is shown in Table I. It should be noted that the opamp power dissipation was not optimized, and that a class AB output stage would be more power efficient [35]. Since the opamps consume the majority of the analog power, it is possible that such design refinements and optimizations could reduce the overall analog power by as much as 10–20%.

B. Main and Minor-Loop NRZ Feedback DACs

In principle, the main feedback DAC can be implemented by using either a non-return-to-zero (NRZ) or a return-to-zero (RZ) structure. Indeed, the RZ scheme appears to be more attractive than the NRZ scheme due to its robustness to switching transient mismatch errors. This benefit arises from the RZ DAC's

generation of both rising and falling transients within the sample period, which eliminates code dependency of any glitch energy from clock/data feed-through and charge injection as long as the output waveform settles. In contrast, the NRZ DAC output transitions only when sequential codes differ, resulting in code-dependent switching errors that cannot be shaped by DEM algorithms, which shape static mismatches.

The RZ signaling scheme does have, however, one crucial demerit that precludes its use in the main feedback DAC. The output pulses it generates cause large perturbations at the opamp input nodes, aggravating the impact of quantization noise-folding due to opamp nonlinearity. Consequently, an RZ DAC was deemed unattractive for the main feedback DAC topology, and an NRZ topology was chosen instead. However, as discussed in the next subsection, the RZ DAC is used within the minor loop feedback since any quantization noise folding arising from the VCO's Kv nonlinearity will be suppressed by the open loop gain of the loop filter.

A simplified view of the main feedback DAC (labeled DAC1 in Fig. 13) signal path is shown in Fig. 16, which includes plots generated from transistor-level simulations of the unit element output current and low-swing buffer voltage output switching waveforms. A summary of the DAC1 key metrics is shown in Table II.

Further details of the DAC1 structure are now discussed. Since the digital data from the DWA will arrive at arbitrary times within a sample period, T, a retiming flip-flop is used to re-align the data and generates full-swing (VDD to GND) differential data signals to drive the DAC switching buffers. A differential, regenerative TSPC structure was used for its simplicity, requiring only one clock phase [18]. Charge injection, clock/data feed-through, and other switching-related errors are minimized by connecting the buffer supplies (VDD,SW and VSS,SW) to two external voltage supplies to generate low-swing outputs, and sizing the pMOS devices to generate strong pull-up edges, and weak pull-down edges [13]. This particular signaling ensures that at least one of the switching devices is always saturated, enabling triple cascoding of the DAC unit element. At the same time, the scheme minimizes
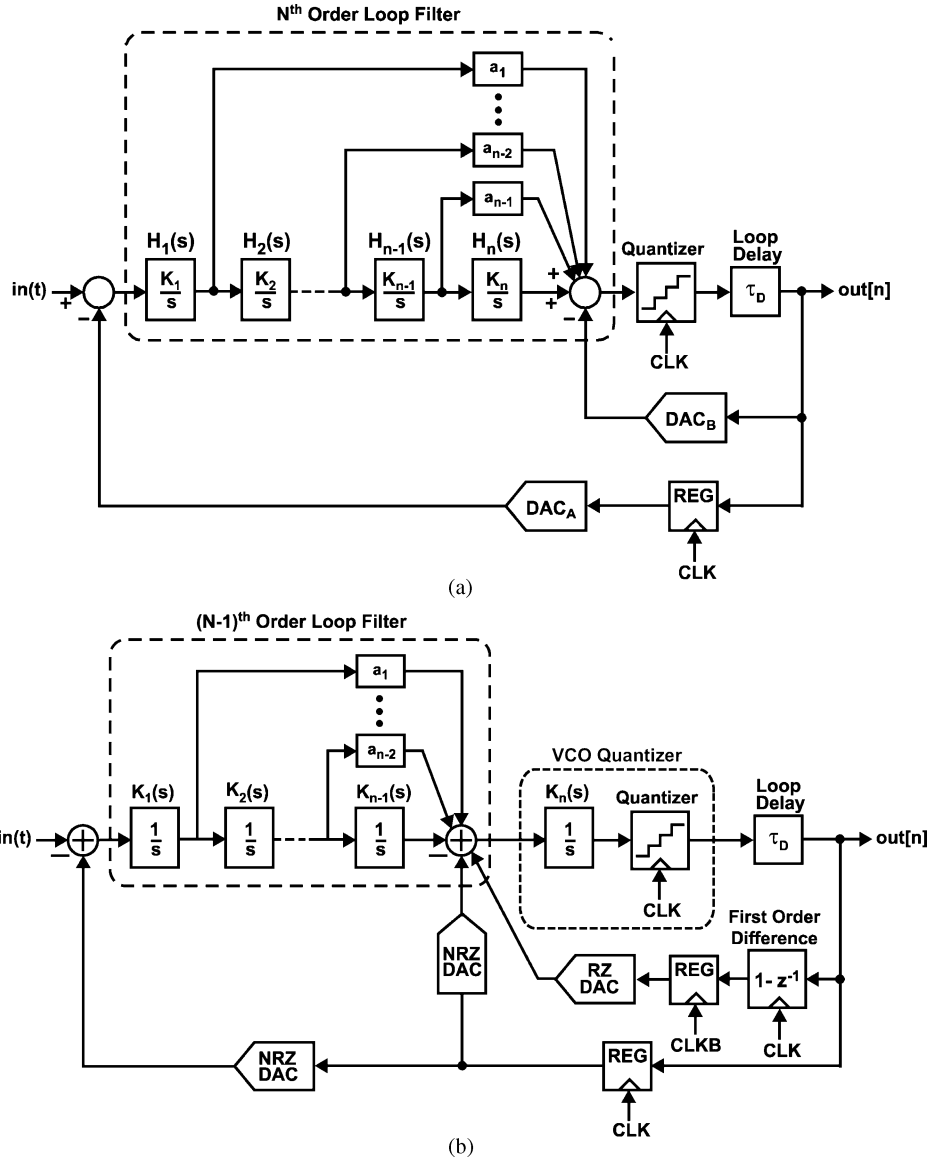
Fig. 11. Classical fourth order loop filter topology assuming (a) traditional quantizer versus (b) modified version of the topology to accommodate integration within the VCO phase quantizer.

perturbations caused by the discharging of the DAC unit-element tail node capacitance that would otherwise generate large current spikes at the output. However, the code-dependence of any switching transient mismatches will still be present, and will not be shaped by the DWA.

As was the case in the design of the amplifiers, flicker noise dominates the output current noise profile of a standard cascoded DAC. Using long tail devices ($L > 1$ μm) can help reduce the flicker noise contribution, but necessitates that the width be proportionately scaled to ensure device saturation, resulting in a large area penalty. A simpler and lower area solution is to degenerate with poly resistors [36], which do not exhibit significant flicker noise (see unit-element in Fig. 16). While the output resistance of the resistor is lower than that of the saturated NMOS, triple cascoding boosts the output resistance as achieved by driving the switching devices with the low-swing buffer described above.

The minor-loop NRZ DAC (labeled DAC2 in Fig. 13) has an identical topology to the main NRZ DAC depicted in Fig. 16, but does not have a degeneration resistor. Since the noise and mismatch error of the DAC are suppressed by the gain of the loop filter, a standard cascoded DAC structure using smaller devices and consuming less power can be adopted. As before, triple cascoding is enabled by limiting the voltage swings to the current steering pair such that one device is always saturated.

C. Delay Compensating RZ Feedback DAC

A schematic of the minor-loop RZ DAC structure (see Fig. 13) and the RZ pulse shaping logic is shown in Fig. 17. Thanks to the RZ signaling scheme's robustness to glitch energy, full swing logic can be used instead of limited swing drivers to control the DAC. Retiming latches are not needed so long as the input to the logic settles before the rising edge of CLKB. During the zero clock phase (CLK), the DAC current is
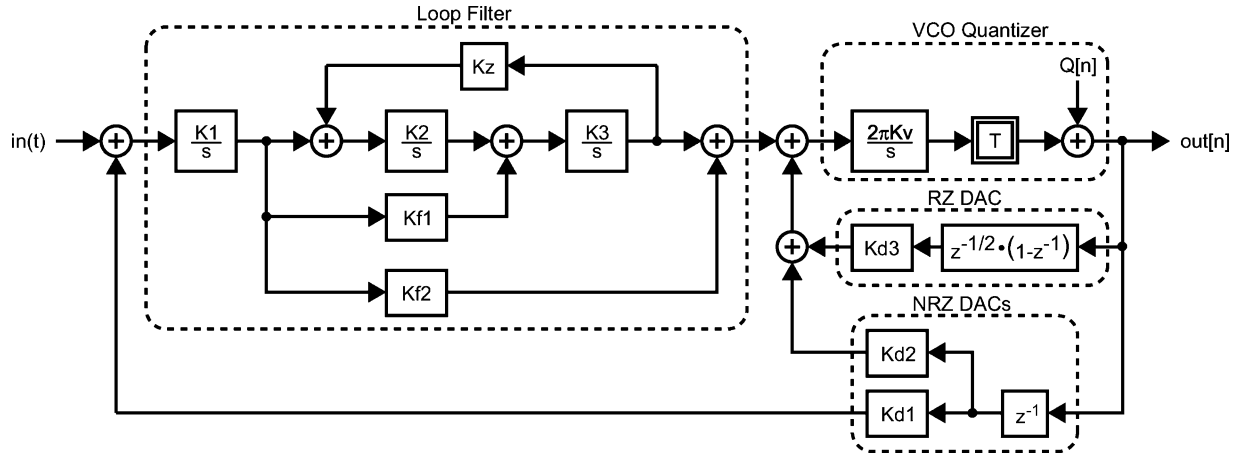
Fig. 12. Loop filter block diagram with VCO quantizer and feedback DACs indicated.
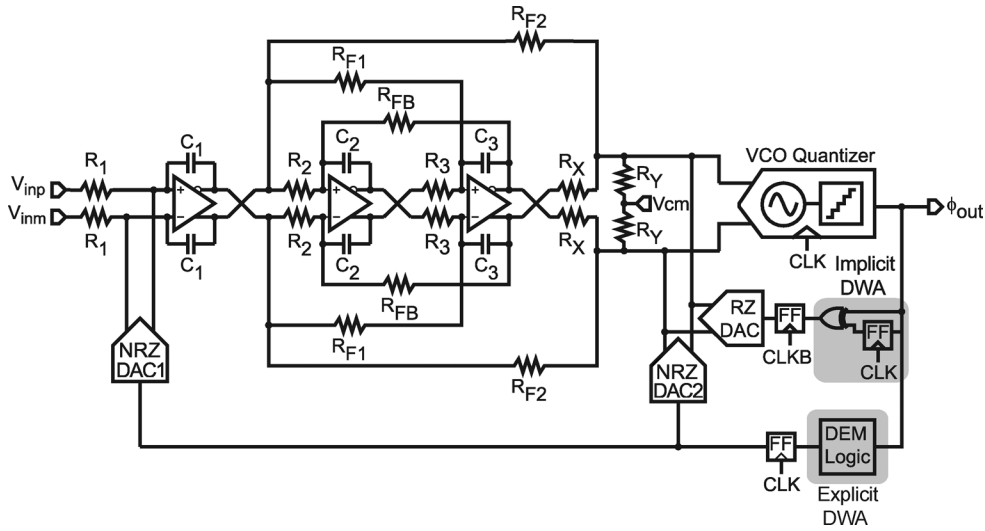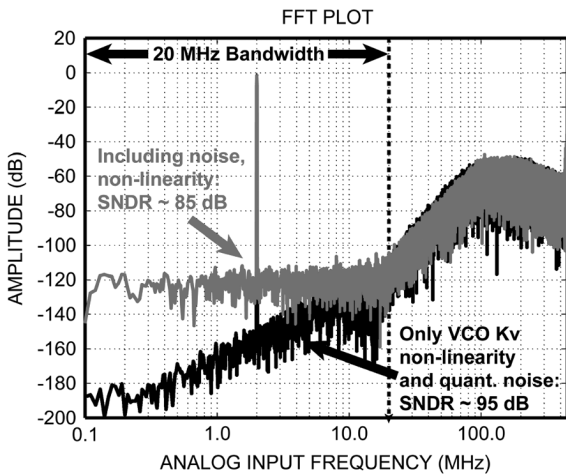

Fig. 13. Schematic of the proposed ADC.

Fig. 14. Simulated spectra of the proposed ADC which includes non-idealities of Kv nonlinearity, device noise, opamp finite gain and finite bandwidth, and DAC and VCO unit element mismatch.

TABLE I
PERFORMANCE SUMMARY OF THE FIRST OPAMP IN THE LOOP FILTER

DC Gain	63 dB
Unity-Gain Frequency	4.0 GHz
Phase Margin	55°
Input Referred Noise (in 20 MHz Signal BW)	11 µV (rms)
Power (V_{DD} = 1.5V)	22.5 mW

pMOS current steering devices are controlled by the clock phases CLK and CLKB. While both nMOS and pMOS current steering devices could be controlled by the data, resulting in lower DAC noise, the simpler structure shown in Fig. 17 was adopted since such noise is suppressed by the loop filter gain.

D. VCO Integrator and Quantizer

The highly digital nature of the proposed VCO integrator and quantizer can be appreciated through inspection of Fig. 18, which shows a 3-bit implementation for simplicity, although a 4-bit version was actually implemented. The VCO delay element is based on a current starved inverter, and enables pseudo differential control as well as frequency and Kv tuning to cover process variations [7]. The sense-amp flip-flop (SAFF) from

dumped to a third drain connected to an external voltage VCM, with a nominal value of $V_{DD}/2$. The nMOS current steering devices are controlled in a data-dependent matter, while the
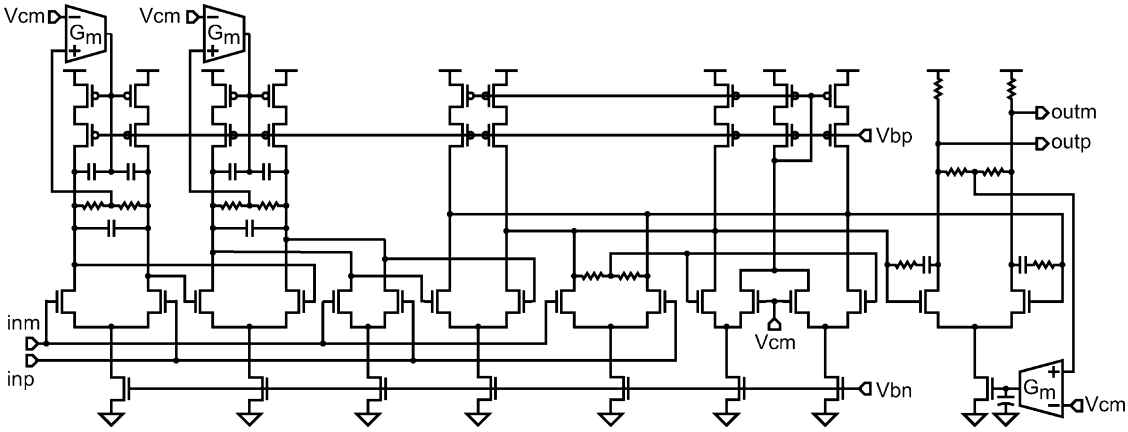
Fig. 15. A modified nested Miller compensated opamp, similar to that used in [12].
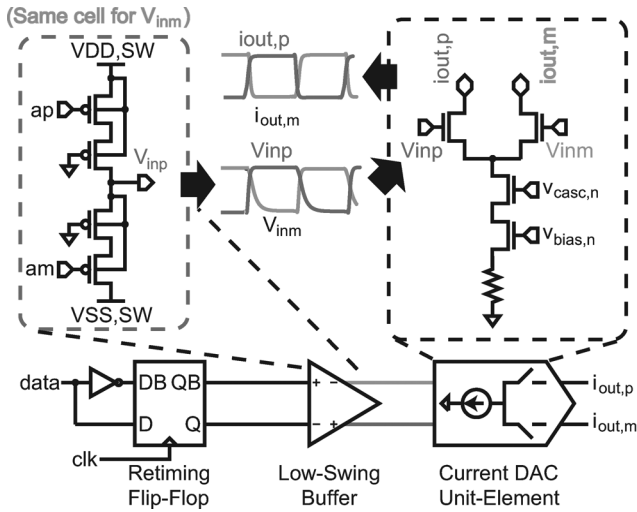
Fig. 16. The main NRZ DAC (DAC1 in Fig. 12) signal path and key circuit blocks.

Fig. 17. Loop-delay compensating RZ DAC schematic.

TABLE II
PERFORMANCE SUMMARY OF THE MAIN FEEDBACK DAC (i.e., DAC1)

Parameter	Value
I_{total}	10 mA
I_{LSB}	625 µA
Unit-Element Output Resistance	70 kΩ
Unit-Element Output Current Noise Power (in 20 MHz Signal-Bandwidth)	$1.1e^{-15}$ A^2
Total Input Referred Noise Power (Total Output Current Noise Power x R_{in}^2)	$1.7e^{-10}$ V^2
Power (V_{DD} = 1.5V)	15 mW

[18] quantizes the VCO output phase by comparing the continuous output level of a given VCO phase tap to the chip common mode voltage at half of the supply. Phase detection and first-order difference computation are achieved using static CMOS XOR gates and single-ended TSPC flip-flops.

The ring-VCO nominally oscillates at a frequency of 225 MHz, but can span from nearly 0 Hz to approximately 450 MHz when the control voltages are swept. The phase detector reference signals also have a frequency of 225 MHz, and are generated by dividing the 900 MHz ADC clock frequency by 4. The quadrature relationship between Ref_0 and Ref_1 can be obtained
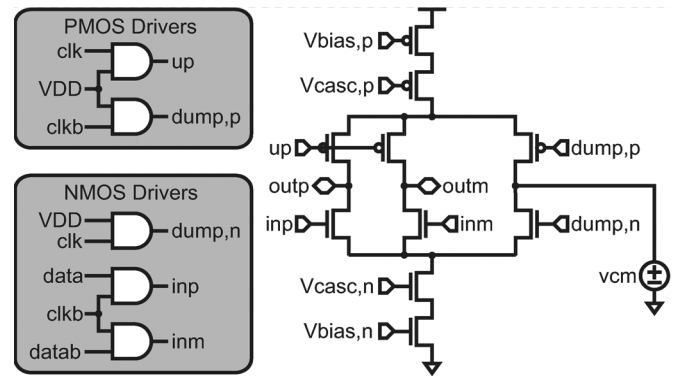
by simply delaying one reference signal relative to the other by one sample period of the 900 MHz clock via a register. Since the ADC clock rate is at least twice the maximum VCO oscillation frequency, the frequency output thermometer code generated by the first-order difference ($f_0[n]$ to $f_6[n]$ in Fig. 18) will automatically correspond to a DWA sequence. Consequently, the minor-loop RZ DAC will automatically benefit from shaping of the mismatch occurring in its unit elements [7], [10].

The output phase error is generated by XOR'ing each quantized VCO phase with one of two reference phases (or their complements). The resulting thermometer code ($\varphi_0[n]$ to $\varphi_6[n]$ in Fig. 18), is then proportional to the phase error. As mentioned in Section III, the phase output loses the barrel shifting property that had characterized the frequency output code. Consequently, DEM is explicitly performed on the phase output thermometer code.

E. Explicit First-Order DWA of VCO-Quantizer Phase Output

First-order DWA is chosen for its excellent DAC mismatch noise-shaping performance and easy implementation [31], [35], [37]. While increasing the OSR and the number of quantizer/DAC bits will reduce inband mismatch noise power for a given bandwidth, such an increase must be balanced by the subsequent increase in complexity, power consumption, and delay of the DEM. A sample rate of 900 MHz and 4-bit quantizer were chosen in the implementation of the prototype ADC as a compromise on these issues.
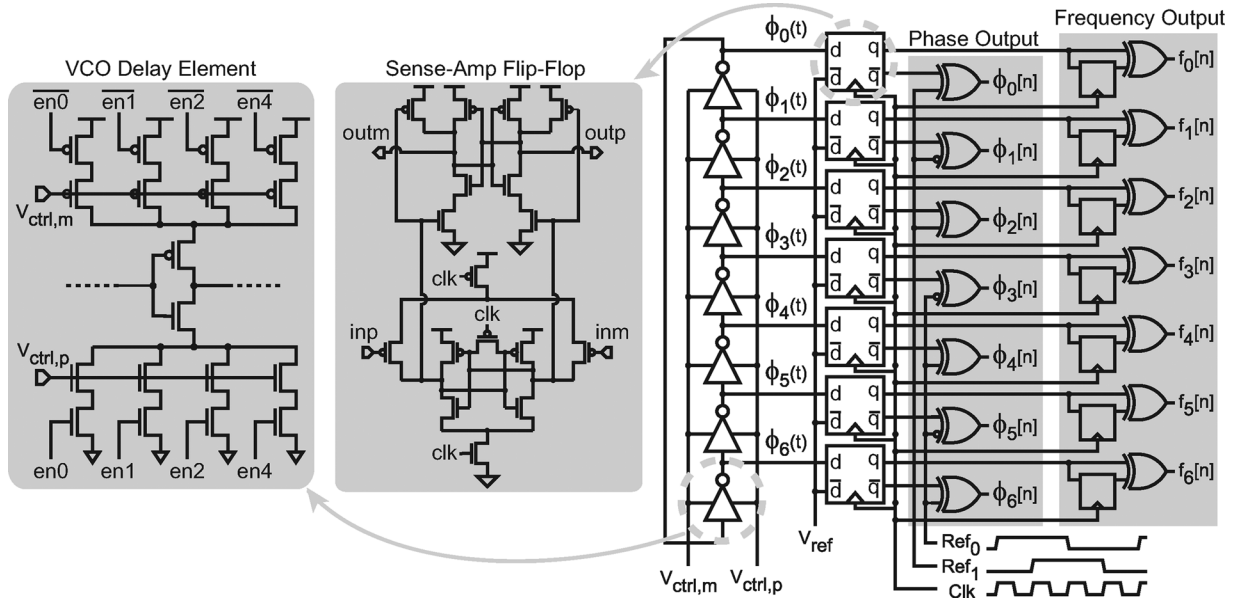
Fig. 18. The ring-VCO integrator and SAFF quantizer, phase detector, and frequency detector (first-order difference).
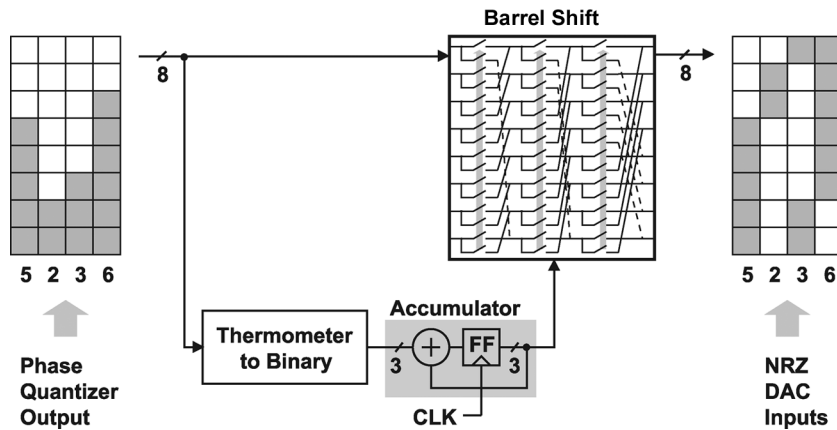

Fig. 19. Explicit DWA computation using a barrel shift, a thermometer-to-binary converter, and binary accumulator.

As shown in Fig. 19, the implemented DWA circuitry rotates the quantizer output thermometer code with the aid of a barrel shifter controlled by a binary accumulator. Note that the number of times that the *current* quantizer thermometer code needs to be shifted by is equal to the modulo-2^N accumulated sum of the *previous* quantizer output values. Consequently, the DWA can be split into two parallel paths, one which shifts the input thermometer code, and the other which records the previous quantizer value and updates the pointer. A fully static-CMOS implementation of the DWA in the 0.13 um technology was not able to satisfy the timing requirements with sufficient margin due to the wiring parasitics and device capacitances. Instead, a faster pseudo nMOS logic implementation using pMOS loads and powered by a 1.5 V supply were chosen [38], though at the cost of higher power consumption.

V. MEASURED RESULTS

The test setup used to evaluate the prototype ADC is shown in Fig. 20. Here, an analog signal source (Agilent E4430B) drives a 2 MHz tone into a passive bandpass filter (TTE KC7T-2M-10P),

which suppresses the harmonics and phase noise of the signal source. An RF transformer (Mini-Circuits ADT1-6T+) converts this spectrally purified tone into a differential signal that serves as the input to the prototype ADC. The ADC clock signal is generated by a high-speed pattern generator (HP 70843B), which can generate low-jitter, square waveforms ($<$1 ps, RMS in bandwidth of interest). The 4 digital output bits generated by the prototype ADC are stored into the memory of a high-speed sampling oscilloscope (Agilent DSA 80000B), and then downloaded to a PC for post-processing. Calibration of the prototype ADC is achieved via an on-chip serial interface connected to a PC. The tuning procedure involves programming the VCO coarse tuning bits and loop filter capacitor control bits to the nominal settings used in simulation, and then iteratively adjusting these bits until the desired noise shaping is observed in measurement.

A die-photo of the fabricated prototype ADC in 0.13 um CMOS is shown in Fig. 21, and a table summarizing the ADC performance is found in Table III. The active silicon area of the ADC is 0.45 mm^2, and the total chip area including 48 pads is
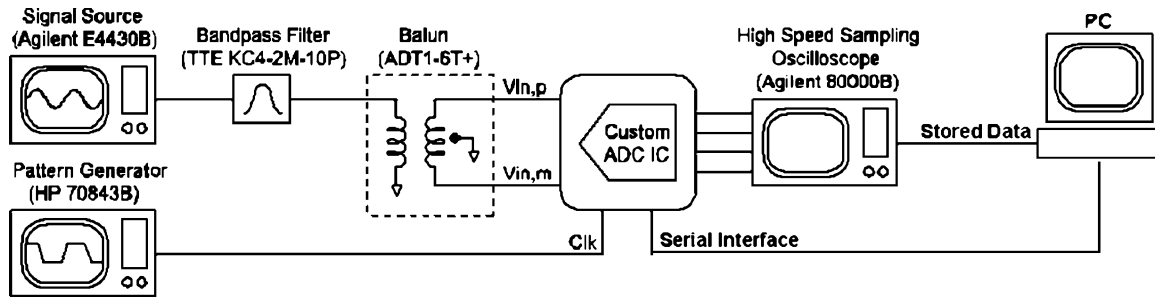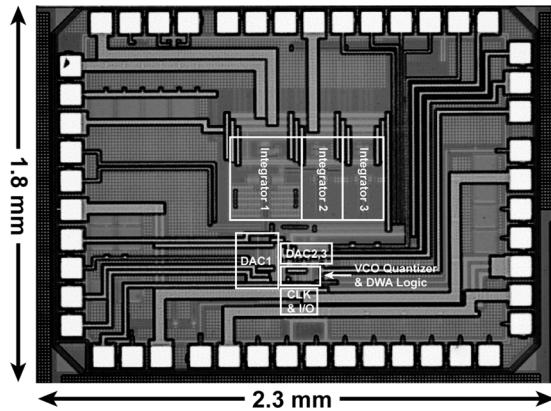
Fig. 20. Test site for evaluation of the prototype ADC.

Fig. 21. Die photo of the prototype ADC fabricated in a 0.13 um IBM CMOS process. The active area is 0.45 mm^2.

TABLE III
SUMMARY TABLE OF RESULTS

Specification	Value
Sampling Frequency	900 MHz
Input Bandwidth	20 MHz
Peak SNR	81.2 dB
Peak SNDR	78.1 dB
Analog Power	69 mW (1.5V)
Digital Power	18 mW (1.5V)
FOM	330 fJ/conv.
Active Area	0.45 mm^2
Technology	0.13 um IBM CMOS

2.3 mm $\times$ 1.8 mm. The prototype ADC dissipates roughly 87 mW from a 1.5 V supply, with the analog and digital supplies drawing roughly 46 mA and 12 mA, respectively. Although there is no direct way to measure the subsystem current, bias currents indicate that the DACs consume 15 mA, the operational amplifiers consume 30 mA, and the VCO consumes less than 1 mA. Simulations indicate that the data-weighted averaging logic comprises the majority ($>75\%$) of the digital power dissipation due to the use of pseudo nMOS logic in the thermometer-to-binary converter and accumulator, with the VCO phase quantizer flip-flops and clock generation and distribution circuits comprising the remainder.

The measured SNR and SNDR versus input amplitude curves are shown in Fig. 22. For these measurements, the input tone frequency is 2 MHz, the analog bandwidth is 20 MHz, and the sample rate is 900 MHz. For a -2.4 dBFS (approximately 1.5 V$_{pp,diff}$) input tone, the ADC achieves a peak SNR of 81.2 dB,

and a peak SNDR of 78.1 dB; this corresponds to a resolution of 12.7 ENOB, and a figure of merit (FOM) of approximately 330 fJ/conv, where the FOM is defined as

$$\text{FOM} \equiv \frac{\text{Power}}{2 \times BW \times 2^{\text{ENOB}}}$$

Fig. 22 shows a fast Fourier transform (FFT) of the ADC output for a 2 MHz input signal at -2.4 dBFS. Fourth-order quantization noise shaping is visible in the frequency range from 20 MHz to 70 MHz, and peaks locally at 70 MHz due to a parasitic pole, which degrades phase margin. Behavioral simulations suggest that the tones appearing in the 200–250 MHz range and centered at 225 MHz (Fs/4) are most likely due to the phase detector reference clock signal and the VCO output phases parasitically coupling into the VCO control node. Fortunately, these tones are far out of band and did not affect the resolution or stability of the ADC. Device noise from the second and third stage amplifiers, minor-loop DACs, and VCO quantizer are suppressed by the high gain of the preceding stages in the loop filter, and should therefore have a negligible impact on the noise floor. Consequently, both thermal and flicker noise in the overall ADC should be dominated by the first opamp and NRZ DAC1. Unfortunately, while the device thermal noise floor is evident in Fig. 22, flicker noise is not visible in the FFT due to its limited resolution below 100 kHz as a result of the finite memory storage of the high speed sampling scope.

The measured results shown in Fig. 22 compare well with the behavior simulation of the system shown in Fig. 14. The primary difference lies in the presence of even and odd order distortion tones, which were found to be present even in the absence of input signal power. This artifact is most likely caused by mismatches in the DAC unit element switching transients. Indeed, varying the supply voltage of the buffers that drive the DAC switches provided some empirical evidence of the mismatch, as any deviations accentuated switching related errors and consistently worsened measured inband distortion. Behavioral simulation also appears to confirm this suspicion as the inclusion of such mismatch, along with opamp nonlinearity, in the model generates inband distortion tones similar to those encountered in measurement, as can be seen in the simulated FFT of Fig. 23.

A comparison of the measured results of this work with other CT $\Delta\Sigma$ ADCs operating at a sample rate of 250 MHz or above is shown in Table IV. The 81 dB SNR and 78 dB SNDR of this work shows that VCO-based ADCs can be utilized in high performance applications, and that the nonlinearity of the VCO Kv transfer characteristic is not a limiting factor to achieving
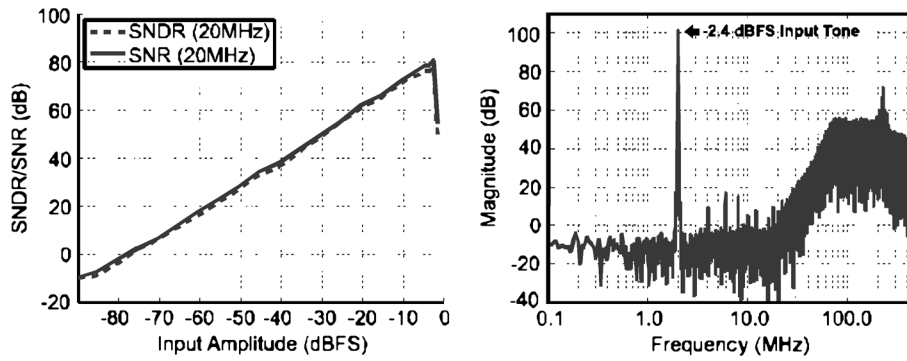
Fig. 22.　Measured SNR/SNDR versus input amplitude, and 100,000 point FFT plot generated from measured output of prototype ADC.
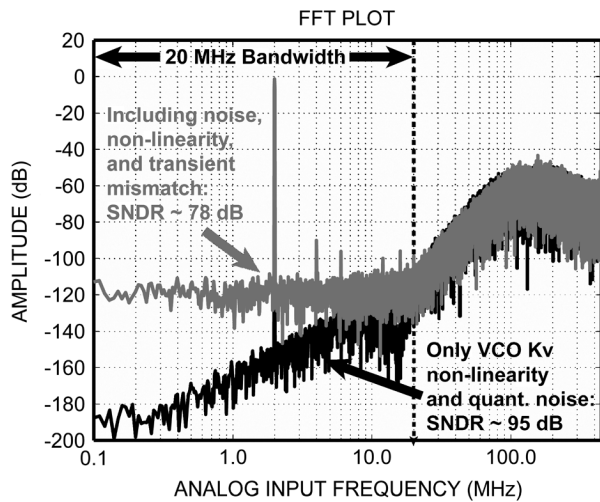

Fig. 23.　Behavioral simulation of prototype ADC including DAC transient mismatch and opamp nonlinearity effects, as well as all other noise and nonlinearity sources modeled in the behavioral simulation result shown in Fig. 14. Inclusion of the opamp nonlinearity reduces SNDR to 81 dB, and further inclusion of DAC transient mismatch reduces SNDR to 78 dB as shown.

TABLE IV
COMPARISON OF RECENT CT $\Delta\Sigma$ ADCs WITH SIMILAR
INPUT BANDWIDTHS AND TECHNOLOGY

Ref.	Fs (MHz)	BW (MHz)	SNR (dB)	SNDR (dB)	Power (mW)	FOM (pJ/Conv)
[19]	276	23	70	69	46	0.43
[15]	340	20	71	69	56	0.61
[14]	400	12	64	61	70	3.18
[20]	640	10	72	66	7.5	0.23
[12]	640	20	76	74	20	0.12
[31]	640	10	87	82	100	0.49
[21]	1000	8	63	63	10	0.54
[7]	950	20	75	67	40	0.55
This work	**900**	**20**	**81**	**78**	**87**	**0.33**

such performance. Continued device scaling should improve the power efficiency of the entire structure, as full-swing static CMOS can replace the power hungry pseudo nMOS logic, yielding greater than 50% reduction in digital power consumption. At the same time, a more optimized opamp design with a class AB output stage [35] can likely yield greater than 10% reduction in the overall analog power consumption.

VI. FUTURE DIRECTIONS

This section will suggest improvements to the proposed architecture that show promise of extending the converter's resolution to >13 ENOB while simultaneously achieving lower power consumption.

The measured results from the previous chapter suggested that the prototype ADC's resolution was most likely limited by transient mismatch from the main feedback DAC. Fortunately, a simple yet highly linear DAC structure that is robust to such error was proposed in [22], and is shown in Fig. 24(a). This dual return-to-zero (DRZ) DAC structure breaks the signal dependency of the transient mismatch errors in the NRZ DAC by forcing all switching devices to transition during each sample period. Indeed, the output waveform generated by the DRZ DAC essentially mimics two time-interleaved RZ DAC waveforms, which when summed together, resemble the equivalent NRZ waveform, but with the RZ switching transients evident at the rising and falling edges of the clock.

The proposed explicit DWA implementation encountered a bottleneck in the thermometer-to-binary conversion and binary accumulation, which limited the number of quantizion levels and required a more power-intensive pseudo nMOS implementation to meet timing. Fortunately, a faster DWA architecture with greater timing efficiency can be achieved by recognizing that the barrel shift's inherent accumulation of the DWA pointer precludes the need for a thermometer-to-binary converter and binary accumulator [31]. As shown in Fig. 24(b), simple logic compares adjacent thermometer bits to determine the location of the DWA pointer (denoted by the juxtaposition of a 1,0 transition), a ROM converts the pointer to binary to control the barrel shift, and logic detecting a thermometer code comprising all zeros or ones preserves the previous DWA pointer.

Given the potential for a higher number of quantizer/DAC bits enabled by the faster DWA implementation, as well as the greater robustness to transient mismatch offered by the DRZ DAC, it is useful to consider how the proposed ADC's performance will be affected. Table V shows the results of detailed behavioral simulations to determine the SNR/SNDR average and standard deviation over 50 Monte Carlo runs assuming a 4-bit and 5-bit quantizer/DAC implementation for the proposed ADC architecture. The simulated results are further disaggregated according to the specific DAC structure (NRZ or DRZ) to quantify the architecture's sensitivity to transient mismatch. It is as-
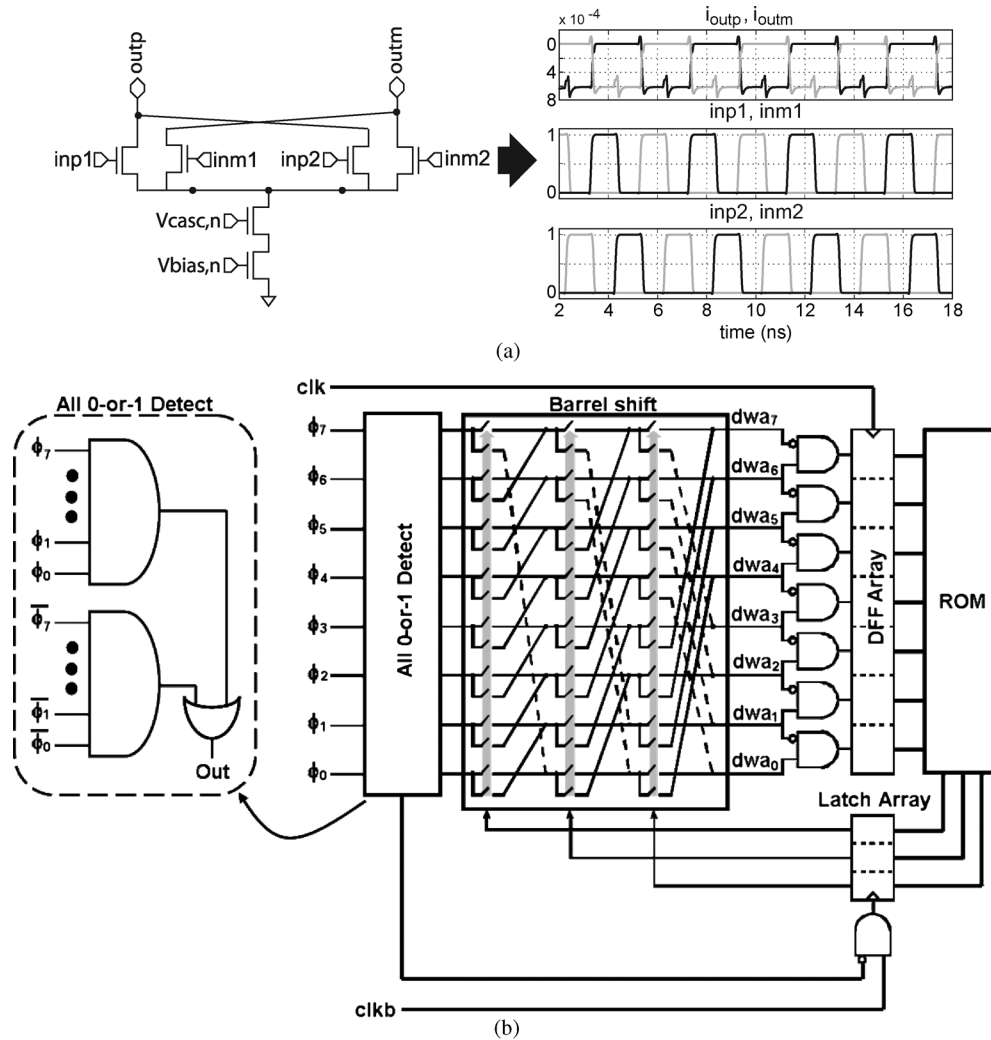
Fig. 24. Illustration of (a) the DRZ DAC [22], and (b) the faster DWA implementation.

TABLE V
SIMULATED SNR AND SNDR AVERAGE AND STANDARD DEVIATION (σ) OVER 50 MONTE CARLO RUNS ASSUMING A 4-BIT AND 5-BIT QUANTIZER AND NRZ/DRZ DAC

Parameter	4-bit		5-bit	
	NRZ	DRZ	NRZ	DRZ
SNR (dB)	82.9 ($\sigma = 3.9$)	83.0 ($\sigma = 1.1$)	87.0 ($\sigma = 0.6$)	86.9 ($\sigma = 0.5$)
SNDR (dB)	78.3 ($\sigma = 3.8$)	81.9 ($\sigma = 1.0$)	82.6 ($\sigma = 3.9$)	85.8 ($\sigma = 0.4$)

sumed in these simulations that the unit element and transient mismatches for the DACs are the same as those for the implemented 4-bit prototype ADC. Further information, including the exact behavioral model used to generate these results, can be found in [34]. As the simulations show, close to 14 ENOB can be obtained with a 5-bit quantizer and DRZ DAC implementation.

VII. SUMMARY

This work demonstrates a new CT $\Delta\Sigma$ VCO-based ADC architecture that achieves high resolution and wide input bandwidth by leveraging the VCO quantizer's phase output to avoid the Kv nonlinearity that had hampered higher SNDR in prior works. The prototype ADC achieves a peak SNR/SNDR of 81.2/78.1 dB over a 20 MHz bandwidth, and dissipates 87 mW from a 1.5 V supply. With measured performance that rivals architectures employing more area and power intensive classical multi-bit quantizers, VCO-based quantization offers a host of signal processing and implementation advantages that show great promise in enabling high performance CT $\Delta\Sigma$ ADC designs in future CMOS technologies.

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