A Low Jitter Programmable Clock Multiplier Based on a Pulse Injection-Locked Oscillator With a Highly-Digital Tuning Loop

Belal M. Helal, *Member, IEEE*, Chun-Ming Hsu, *Member, IEEE*, Kerwin Johnson, and Michael H. Perrott, *Senior Member, IEEE*

***Abstract*—This paper introduces a pulse injection-locked oscillator (PILO) that provides low jitter clock multiplication of a clean input reference clock. A mostly-digital feedback circuit provides continuous tuning of the oscillator such that its natural frequency is locked to the injected frequency. The proposed system is demonstrated with a prototype consisting of a custom 0.13 μm integrated circuit with active area of 0.4 mm^2 and core power of 28.6 mW, along with an FPGA, a discrete DAC and a simple *RC* filter. Using a low jitter 50 MHz reference input, the PILO prototype generates a 3.2 GHz output with integrated phase noise, reference spur, and estimated deterministic jitter of 130 fs (rms), −63.9 dBc, and 200 fs (peak-to-peak), respectively.**

***Index Terms*—Subharmonic, injection locked oscillator, pulse, PILO, deterministic jitter, reference spur, correlation, correlated double sampling, gated ring oscillator, GRO, time to digital converter, TDC, integer-N, phase locked loop, PLL.**

I. Introduction

THERE has recently been increasing interest in CMOS circuits that leverage injection-locked oscillators, including frequency dividers [1], clock and data recovery circuits [2], clock multipliers [3], and frequency synthesizers [4], [5]. In this paper, we focus on the area of clock multiplication for applications that require high-speed clocks with very low jitter such as high performance data links and ADCs, which typically rely on an integer-N phase-locked loop (PLL) for this function. We begin by considering the subharmonic injection locked oscillator shown in Fig. 1 [4], [5].

The oscillator consists of an *LC* tank, whose loss, R, is compensated by the active circuit, and a current source clocked at the reference frequency, which injects the *LC* tank with a stream of current pulses. Assuming that the natural running frequency of the oscillator is close to the Nth harmonic of the reference, the *LC* oscillator will lock onto that harmonic such that its average frequency becomes N times the reference frequency. As shown on the right side of the figure, injection locking forces the oscillator to track the reference frequency, and thereby suppresses the low frequency phase noise of the oscillator [6]. Much of these characteristics are similar to the action of an integer-N frequency synthesizer, but notice that no phase detector, loop filter, or divider is required in this system. Therefore, in principle, an injection-locked clock multiplier can provide a very simple, low power, and low noise means of achieving clock multiplication and can do so with a very short transient response [5].

In practice, there are several challenges in building the clock multiplier shown in Fig. 1. The first issue is that the naturally running frequency of the oscillator must be very close to the desired harmonic of the reference in order to achieve injection-locking. That has been traditionally achieved by first tuning the *LC* resonant frequency of the oscillator with a varactor such that its value is sufficiently close to the desired harmonic as determined with the aid of a frequency detector [3], [5]. The introduction of the injection source then leads to the desired locking behavior. However, since this approach must be done off-line, it cannot compensate for temperature variations, and in general will lead to a time-varying difference between the natural running frequency of the *LC* oscillator, f_o, and the desired injection harmonic, $N \cdot f_{\mathrm{ref}}$. This will generally lead to large reference spurs at the output of the *LC* oscillator which substantially degrade its jitter performance, and may even lead to loss of lock or skipping to a different harmonic if the difference between f_o and $N \cdot f_{\mathrm{ref}}$ becomes too large. The second issue is that, even in the case where $f_o = N \cdot f_{\mathrm{ref}}$, the current pulses that are injected into the oscillator will periodically disturb its amplitude. While the cyclostationary properties of the *LC* oscillator will ideally reject the impact of such amplitude disturbances on its phase since they occur at the peaks of the sine wave [7] (as shown in Fig. 1), a practical oscillator will experience phase deviations from this effect due to issues such as nonlinear capacitance in the tank (which causes voltage dependent distortion of the sine wave), change in the instantaneous oscillation frequency due to discharge of the injected charge over a few cycles, and sensitivity of the VCO buffer edge crossings to the instantaneous slope of its input.

In this paper, we will present a subharmonic injection locked clock multiplier that addresses each of the above issues [8]. In

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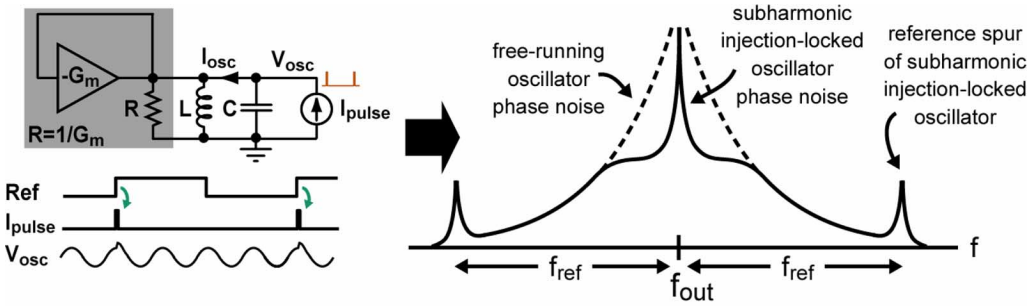

Fig. 1. Subharmonic injection-locked *LC* oscillator using current pulses.

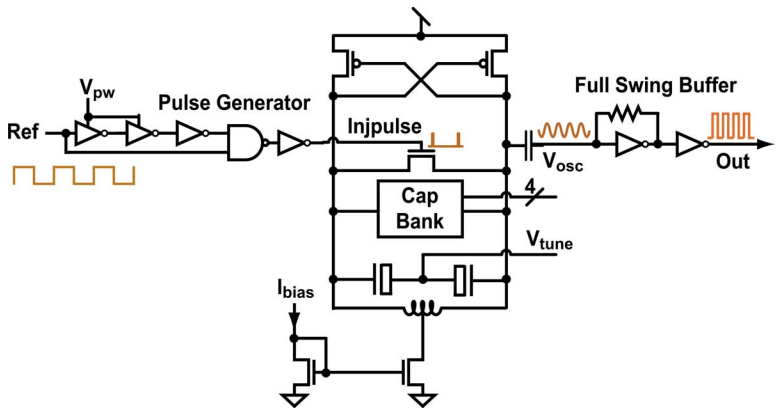

Fig. 2. Proposed PILO circuit.

particular, we will show that you can achieve *continuous* tuning of the *LC* oscillator while it is being injected so that its natural frequency, f_o, continuously tracks the desired harmonic, $N \cdot f_{\rm ref}$. In addition to providing robust operation of the clock multiplier, the process of continuous tuning allows substantial reduction of reference spurs so that excellent jitter can be achieved. As for the issue of amplitude disturbances due to the injection of current pulses, we will show that injection locking can also be practically achieved with much less disturbance by using a simple switch to periodically short the tank. A prototype of the clock multiplier reveals measured results of 130 fs of random jitter (rms) and a -63.9 dBc reference spur performance which corresponds to about 200 fs of deterministic jitter (peak-to-peak).

The paper is organized as follows. In Section II, we propose a differential *LC* oscillator that leverages a shorting switch to achieve subharmonic injection locking, and present an intuitive model of its operation. In Section III, we present a method of continuously tuning the natural frequency of the *LC* oscillator to track the desired harmonic by using a highly digital technique that was recently introduced for multiplying delay-locked loops [9]. Section IV provides an overall model of the injection locked oscillator while it is being continuously tuned which allows phase noise calculations of the system. Section V then presents measured results from a prototype system whose core element is a 0.13 μm CMOS custom integrated circuit. Finally, Section VI concludes.

II. Proposed Pulse Injection-Locked Oscillator

Fig. 2 illustrates the proposed technique of using a shorting switch to achieve subharmonic injection locking of a differential *LC* tank oscillator. We refer to this structure in which injection is achieved by pulses much narrower than the oscillator period as a pulse injection-locked oscillator (PILO), and note that it consists of a pulse generator, which is fed by the reference frequency, that drives a simple NMOS switch that is placed across the differential outputs of the *LC* tank circuit. An NMOS is used for switching due to its faster speed and lower resistance compared to PMOS, especially since the common mode voltage of the tank is less than mid-rail (specifically, $V_{\rm DS}$ of the current mirror). The natural frequency of the oscillator is tuned by a combination of appropriately switching in capacitors within a 4-bit MIM capacitor bank to achieve coarse tuning, and varying the tuning voltage, $V_{\rm tune}$, on an analog varactor (composed of an n-poly/n-well MOSCAP) to achieve fine tuning. A full swing output buffer is used to pass the VCO output to other blocks, such as the tuning circuits to be discussed.

The characteristics of the shorting switch and its input pulses form a key design consideration. The PILO injection strength, and thus the injection bandwidth, is affected by the amount of charge transferred due to the shorting operation. The smaller the resistance of the shorting switch, the higher the shorting current, and hence the higher the transferred charge. Increasing the width of the shorting pulses also increases the transferred charge, and hence increases the injection strength. Since the VCO phase noise will be further suppressed at lower frequencies with increased injection bandwidth, it is desirable to strive for this condition (assuming that the reference clock has low jitter). However, the increase in injection strength is at the expense of lowering the average Q of the tank, which effectively increases the VCO phase noise. As the width of shorting pulse is increased, its

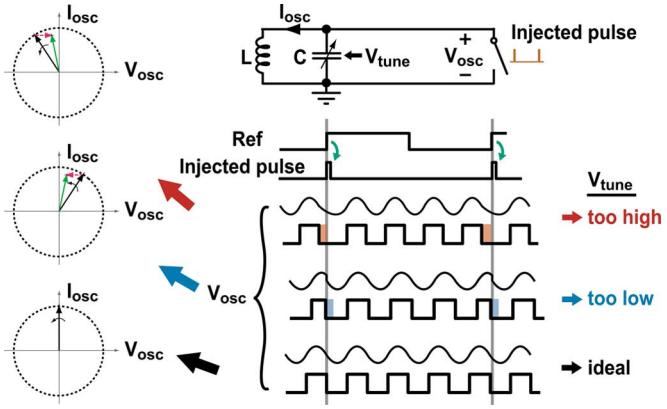

Fig. 3. Impact of frequency tuning on PILO output.

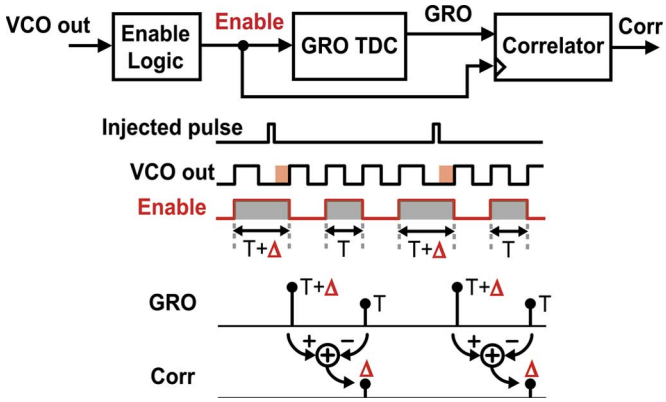

Fig. 4. Proposed technique of measuring deterministic jitter of the PILO output.

impact on the tank will be increased such that larger residual deterministic jitter and reference spurs occur. The prototype PILO allows a variable setting on the supply line voltage of the first two inverters in the pulse generator, $V_{\rm pw}$, in order to adjust their delay, and thereby change the pulse width of the shorting switch (as indicated in Fig. 2).

To provide intuition of the injection locking process in the proposed PILO circuit, Fig. 3 shows phasor diagrams that are normalized to the peak voltage and current of the tank, such that the phase vector periodically rotates around the unit circle as the energy of the tank alternates between the inductor and the capacitor. If the shorting pulse occurs when $V_{\rm osc}$ equals zero, it will have no effect (assuming the pulse is very narrow). Therefore, injection by shorting offers an advantage over current injection by minimizing the disturbance to oscillator amplitude in the case where the shorting pulse width is sufficiently small. On the other hand, if the shorting occurs before or after the zero crossing, the oscillator phase will be pushed towards the zero crossing point such that its phase is either advanced or delayed. When the oscillator is injection locked, this periodic phase shifting will cause the average frequency to match the desired frequency even if the natural frequency of the oscillator is slightly different than the desired harmonic of the injection source frequency. In other words, the injection-locked oscillator will have a zero average frequency error. However, since the injection is occurring at a sub-multiple of the oscillator frequency, the presence of such periodic phase shifting due to frequency offset will lead to a different cycle time for the oscillator during the injection cycle as compared to the free-running cycle time, and thereby induce deterministic jitter and reference spurs at the output of the PILO (as shown in Fig. 1).

The following derivation estimates the effect of the periodic phase shifting of the injection-locked oscillator due to difference between its output average frequency, $f_{\rm out} = N \cdot f_{\rm ref}$, and the oscillator's free running frequency, f_o. Assuming $|f_{\rm out} - f_o| = \alpha \cdot f_{\rm out}$, the offset in the *instantaneous* output period is approximately $\alpha \cdot T_{\rm out}$, where $T_{\rm out} = 1/f_{\rm out}$. Since the offset period accumulates for $N-1$ periods between consecutive injection pulses, the phase shift due to the injection must correct for the accumulated period offset in order for the oscillator to stay locked to the reference source, i.e., to maintain a zero error in the average period. Thus, the period of the injection cycle will differ by $\Delta \approx (N-1)\alpha \cdot T_{\rm out} \approx \alpha \cdot T_{\rm ref}$, causing deterministic jitter of the same amount. Using Fourier analysis, the reference spur (in dBc) $\approx 20\log_{10}(\Delta/T_{\rm out}) \approx 20\log_{10}(N \cdot \alpha)$.

III. Proposed Architecture With Continuous Tuning Technique

Continuous tuning of the oscillator to match its natural frequency to the desired reference harmonic under subharmonic injection locking is much more challenging than encountered with traditional phase-locked loop circuits. In a phase-locked loop, any difference in frequency between the oscillator and desired reference harmonic is observed as a progressively increasing phase difference between those signals. Therefore, even a small frequency difference yields a large phase error signal over time, which is easily corrected by the PLL circuit. Unfortunately, as shown in Fig. 3, an injection-locked oscillator yields only a small phase error due to such a frequency difference since the phase is continuously being reset at the reference rate. As such, the primary challenge for continuous tuning of the PILO is to achieve an accurate measurement of its periodically varying phase error.

As shown in Fig. 4, our proposed approach to measure the PILO phase error, Δ, is to leverage the technique from [9] and compare the oscillator's free running period, T, to its injection-altered period, $T+\Delta$. To perform this time measurement accurately, we take advantage of the gated ring oscillator time-to-digital converter (GRO TDC) described in [9], which measures the time span of *Enable* pulses that are input into it. Subtraction of pair-wise samples of the GRO output by use of a digital correlator block yields Δ. Note that since the same circuits are used to measure both T and $T+\Delta$, traditional issues such as offset and mismatch are greatly alleviated.

Given the digital measurement of Δ as discussed above, we now focus on the issue of closing the continuous tuning loop of the oscillator. As shown in Fig. 5, we accomplish this task by utilizing a feedback loop in which the varactor of the oscillator is controlled by a DAC which is, in turn, fed by an accumulated version of Δ. The feedback loop forces a steady state value of $\Delta = 0$ due to the fact that the accumulator will otherwise ramp up or down with a nonzero value of Δ. To reduce the required number of quantization levels of the DAC, a first order

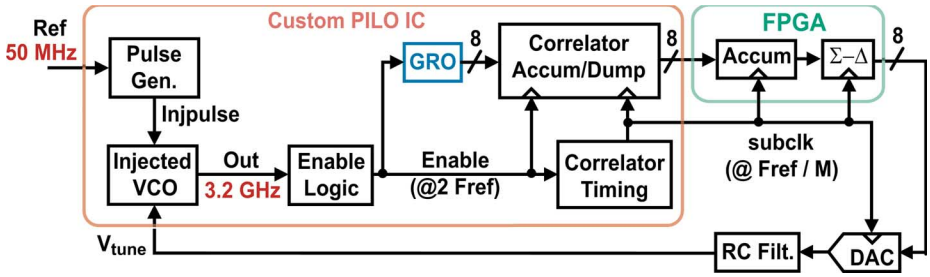

Fig. 5. PILO prototype and its frequency tuning feedback circuit.

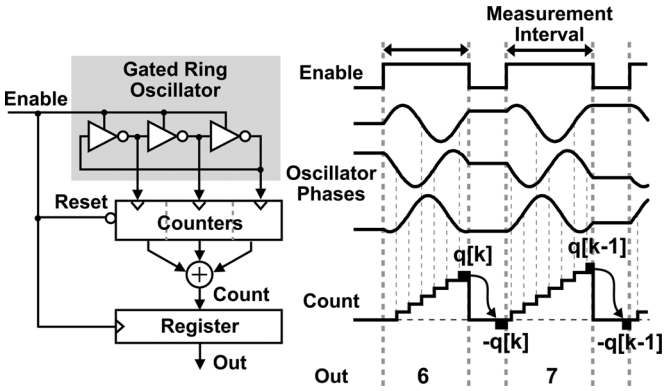

Fig. 6. Gated ring oscillator time-to-digital converter.

Sigma-Delta structure is used to dither between DAC levels, and a simple *RC* low-pass filter is used to smooth out the dithering waveform at the DAC output.

As shown in the figure, the prototype system consists of a custom 0.13 μm CMOS IC, an FPGA board, and an off-chip 16-bit DAC (only the 8 most significant bits of the DAC are used) with a passive *RC* filter (with 500 kHz bandwidth) at its output. The prototype uses a 50 MHz reference input to generate an output at 3.2 GHz (and up to 4 GHz). Note that the system is entirely digital except for the DAC, *RC* low-pass filter, and *LC* oscillator.

We now discuss the various circuits utilized in the prototype in further detail. We begin by briefly reviewing the key characteristics of the GRO TDC which are advantageous for this injection-locking application. We then discuss the means of creating measurement pulses for the GRO in order to compare the free running versus injected period of the oscillator. Finally, we present the digital correlator and accumulator circuit.

A. GRO Time-to-Digital Converter

Fig. 6 displays a conceptual diagram of the GRO TDC used to measure the time duration of the oscillator cycles. The key operating principle is to turn on a ring oscillator during the time measurement period (i.e., assert the *Enable* signal as shown in the figure) and count how many edges occur among the various oscillator stages. As such, the time resolution of the measurement corresponds to the delay per stage of the oscillator, and quantization error occurs at both the beginning and end of the measurement as indicated by the figure. By holding the state of the oscillator between measurements, the quantization error at the end of a measurement interval is transferred to the beginning of the next interval such that first order shaping of the quantization noise is achieved [9].

For the application considered here, the pair-wise subtraction that is performed on the TDC output in order to determine Δ leads to noise folding of its quantization noise such that noise shaping is effectively eliminated [10]. However, despite the loss of noise shaping, the GRO offers scrambling of its quantization noise so that filtering of its output yields high resolution. For the PILO application considered here, such filtering can be considerable since the injected oscillator's natural frequency only needs to be tuned with sufficient bandwidth to accommodate thermal variations.

In the PILO prototype presented in this paper, an advanced version of the GRO TDC is used as described in [11]. The chief difference from what is shown in Fig. 6 is that a multi-path oscillator topology is used to dramatically reduce the effective delay per stage to 6 ps, though the mismatch between its delay elements raises its quantization noise to having the equivalent resolution of about 18 ps. The delay per stage of 6 ps is used for calculation of the effective gain of the GRO TDC, while the equivalent mismatch resolution of 18 ps is used for modeling its noise contribution.

B. Generation of the GRO Enable Signal

For the PILO application, the GRO *Enable* signal must alternate between the naturally running period and injection-impacted period of the oscillator; thus its frequency is double that of the reference. Since the oscillator frequency is 3.2 GHz in this application, the key challenge in generating the *Enable* signal is in achieving a low power implementation.

Here we propose using an asynchronous multi-modulus divider [12] for the GRO *Enable* pulse generation as shown in Fig. 7. This divider structure produces pulses with pulse widths that vary in width according to which divider stage is tapped. Since the GRO requires a minimum time duration pulse to operate properly, the appropriate divider stage must be tapped to ensure this width requirement is met. In the prototype, the mod_1 signal yielded the best performance, which corresponds to two periods of the 3.2 GHz oscillator.

The multi-modulus divider provides the ability to efficiently generate *Enable* pulses for the GRO TDC, but these pulses must also be aligned such that they alternate between the free running and injection impacted oscillator period. To achieve such alignment, the divider phase can be stepped by temporarily changing its divide value away from its nominal value of $N/2$ (note that $N = 3.2$ GHz/50 MHz $= 64$ in the prototype).

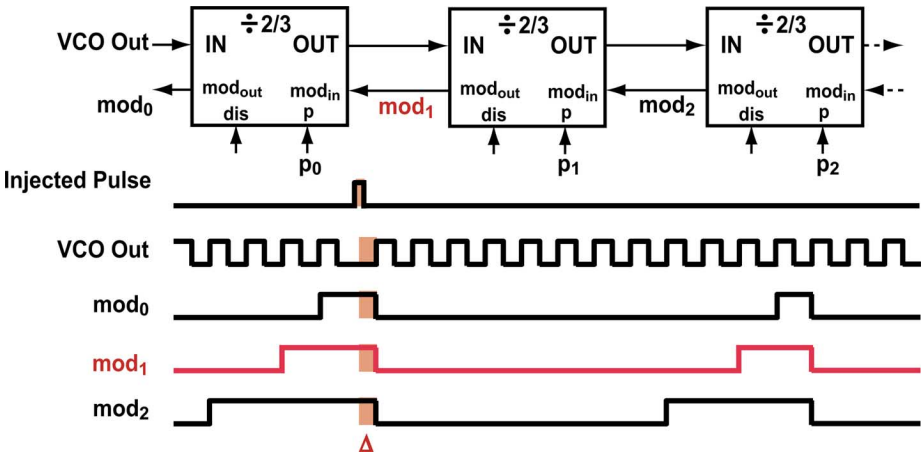

Fig. 7. Multi-modulus frequency divider used as an *Enable* generator.

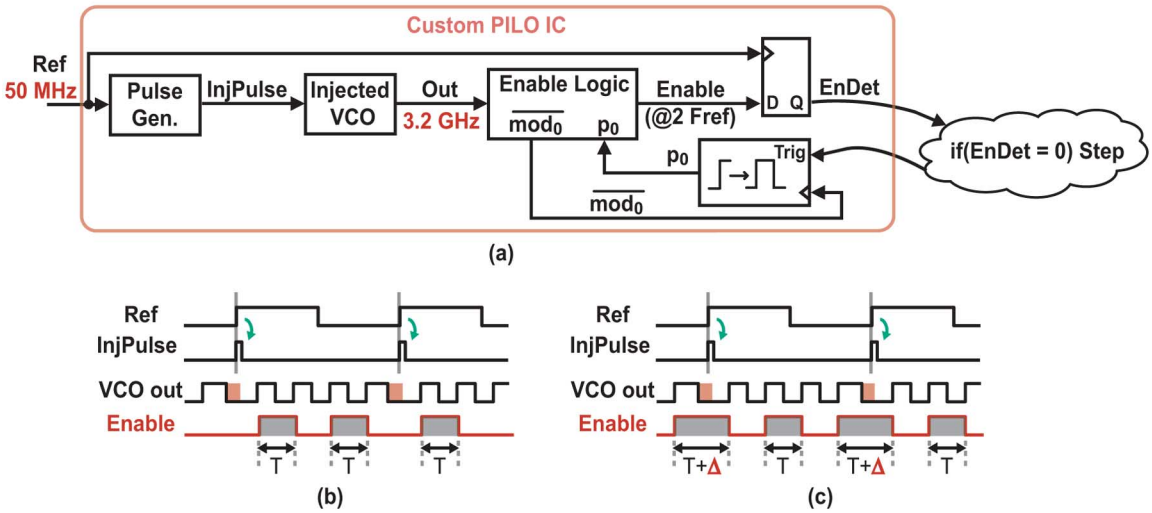

Fig. 8. (a) Divider stepping circuits. (b) Tuning error *not* captured by *Enable*. (c) Tuning error captured by *Enable*.

As shown in Fig. 8, this is accomplished by using a one-shot monostable circuit that receives the stepping command and then pulses p_0 (shown in Fig. 7) high for one divider cycle. In the prototype, the *Enable* alignment was done by hand through external control and monitoring of the PILO Enable generation circuit and stepping the divider until the *Enable* pulse is detected (i.e., when *EnDet* in Fig. 8 is asserted).

Fig. 9 shows the circuit implementation of each multi-modulus divider stage. The implementation is similar to [12], except that disabling functionality is added by including a NOR gate in the path of the p signal (sometimes called *CON*) to the input flip-flop so that it can be disabled by pulling the pin *dis* high. Disabling the stage, instead of bypassing it as described in [12], also allows the generation of any division ratio starting from 2, but without the subsequent stages generating potentially harmful subharmonics that can couple to the oscillator.

C. Correlator With Accumulate and Dump

Fig. 10 shows the implementation of the correlator circuit combined with an accumulate and dump structure. The correlator simply changes the sign of the GRO measurements in alternating fashion, which acts to subtract the free running versus

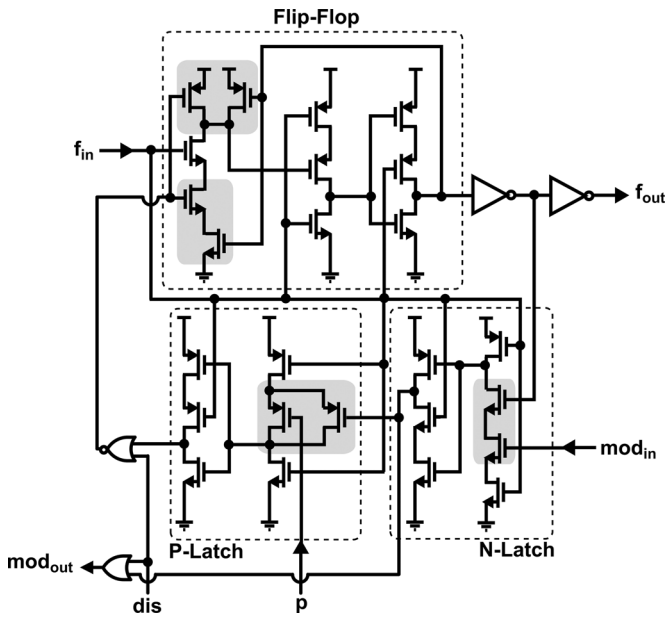

Fig. 9. Modular divider stage with disable functionality.

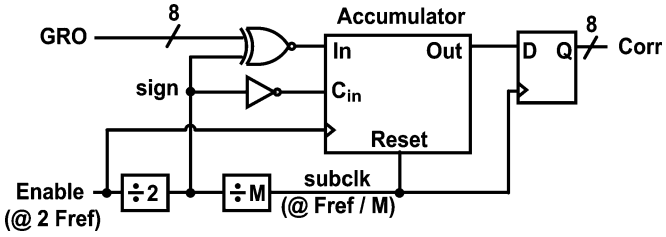

Fig. 10. Correlator with accumulate-and-dump.

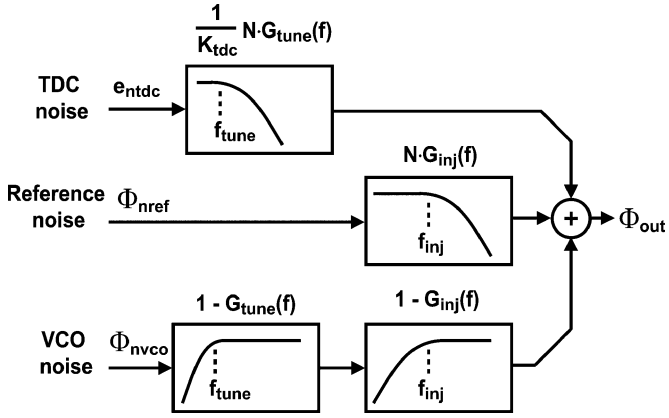

Fig. 11. Simplified phase noise model.

injection impacted periods of the oscillator. The accumulate-and-dump functionality is used to reduce the clocking rate of the subsequent digital stages, which for this prototype are located off-chip in the FPGA. This serves to reduce power consumption and relax timing margins in the interface to the FPGA.

IV. Architecture Modeling

The continuously-tuned PILO resembles a PLL in that the frequency error between the reference and oscillator output is tuned to zero by the action of feedback, but adds the additional element of injection locking when considering the overall system dynamics and noise performance. Fortunately, a phase noise model has been recently introduced for multiplying-delay locked loops (MDLL) that is suitable for a system in which a VCO is locked by both injection and a tuning loop [13]. We will leverage this work to construct a noise model for the proposed continuously-tuned PILO, beginning with a simplified top level view of the model and then proceeding to fill in details of that model.

Fig. 11 shows a high level phase noise model of the continuously-tuned PILO. As shown in the figure, there are three key noise sources in the system: TDC noise ($\mathrm{e_{ntdc}}$), reference phase noise (Φ_{nref}), and VCO phase noise (Φ_{nvco}). TDC noise influences the output phase noise through a low-pass filter, $(N/K_{\mathrm{tdc}})G_{\mathrm{tune}}(f)$, of bandwidth f_{tune}, which is formed by the dynamics of the continuous tuning. Since the continuous tuning needs only to track thermal variations, f_{tune} can be set to a very low value (i.e., $<$10 kHz). Reference noise also influences the output phase noise through a low-pass filter, $\mathrm{NG_{inj}}(f)$, but the bandwidth of this filter, f_{inj}, will generally be quite large relative to f_{tune} (up to about one fourth of f_{ref}). Finally, VCO phase noise will influence the output phase noise through a cascade of two highpass filters, $1 - G_{\mathrm{tune}}\,(f)$ and $1 - G_{\mathrm{inj}}(f)$. Similar to a PLL, the VCO phase noise is suppressed at low frequencies since it is forced to track the reference. Unlike a PLL, the VCO has two paths by which it tracks the reference—the injection-locking path and the continuous tuning path. By achieving a high bandwidth injection-locking path and low bandwidth continuous-tuning path, *both* VCO noise and TDC noise can be significantly suppressed. This is in contrast to PLL circuits which must directly trade off the influence of VCO noise and detector noise by choice of the PLL bandwidth [14].

Fig. 12 shows a more detailed block diagram of the continuously-tuned PILO, which is a direct analogy of the model presented in [13]. We see again that the VCO output phase is influenced by the injection path, $\mathrm{NG_{inj}}(f)$, and by the continuous tuning path, which is modeled as a feedback loop whose key elements are the mostly digital tuning path and feedback division factor $1/N$, where N is the ratio of the output frequency to reference frequency. In contrast to a traditional PLL, the influence of injection-locking leads to the inclusion of a highpass filter, $1 - G_{\mathrm{inj}}(f)$, within the continuous-tuning feedback path. In effect, the presence of the $1 - G_{\mathrm{inj}}(f)$ highpass filter accounts for the previously mentioned fact that the injection locking continually resets the phase error between VCO and the reference harmonic that it is injection-locked to.

Further detail is now given for the various blocks shown in Fig. 12. K_{tdc} is the gain of the GRO TDC and is equal to $T_{\mathrm{ref}}/(2\pi T_{\mathrm{tdc}})$, where T_{tdc} is the raw resolution of the GRO TDC (i.e., 6 ps in this case). $H_{\mathrm{acc}}\ (f)$ is the transfer function of the digital accumulator, which approximately equals $F_{\mathrm{acc}}/(j2\pi f)$ at low frequencies, where F_{acc} is the clocking rate of the accumulator (nominally the same as F_{ref}). K_{ext} is the additional gain in the loop that is used to control the tuning loop bandwidth and is equal to 2^M if implemented by bit shifting, where M is the number of bits that the digital word is shifted by. K_{dac} is the gain of the DAC block (including the first order Sigma-Delta (SD) which dithers it) and is equal to $\mathrm{FS}/2^B$, where *FS* is the DAC full scale, and B is the number of input bits to the SD/DAC block. Finally $H_{\mathrm{rc}}\ (f)$ is the transfer function of the *RC* low-pass filter.

We can relate Fig. 12 to Fig. 11 by computing the value of $G_{\mathrm{tune}}\ (f)$ based on the feedback loop shown in Fig. 12 (note that we will examine $G_{\mathrm{inj}}\ (f)$ in more detail below). As such, we compute

$$G_{\mathrm{tune}}(f) = \frac{A_{\mathrm{tune}}(f)}{1 + A_{\mathrm{tune}}(f)}$$

where $A_{\mathrm{tune}}(f)$ is the open transfer function of the continuous-tune feedback loop, calculated as

$$A_{\mathrm{tune}}(f) = K_{\mathrm{tdc}}H_{\mathrm{acc}}(f)K_{\mathrm{ext}}K_{\mathrm{dac}}H_{rc}(f) \times \frac{K_v}{jf}(1 - G_{\mathrm{inj}}(f))/N.$$

Note that since $A_{\mathrm{tune}}(f)$ goes to infinity at low frequencies, $G_{\mathrm{tune}}(f)$ goes to 1 at low frequencies. The value of f_{tune} is estimated by the following expression [10]:

$$f_{\mathrm{tune}} = \frac{1}{2\pi}\frac{1}{T_{\mathrm{tdc}}}F_{\mathrm{acc}}K_{\mathrm{ext}}\frac{FS}{2^B}\frac{K_v}{F_{\mathrm{out}}F_{\mathrm{ref}}}.$$

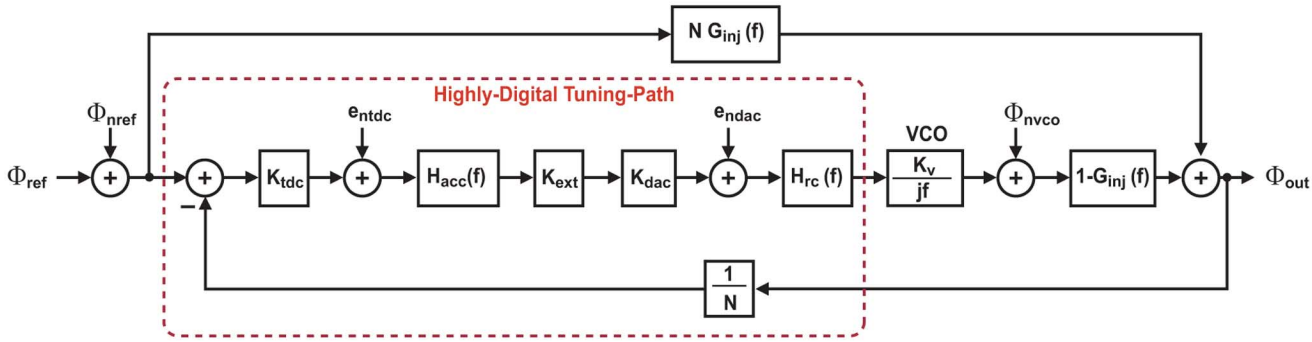

Fig. 12. Phase noise model of the proposed architecture.

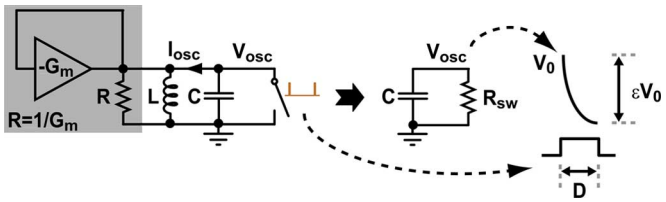

Fig. 13. Approximation of the oscillator as a discharging capacitor.

Calculation of the various transfer functions in Fig. 11 follows as

$$TF_{\rm tdc} = \frac{\Phi_{\rm out}}{e_{\rm ntdc}} = \frac{N}{K_{\rm tdc}} G_{\rm tune}(f)$$

$$TF_{\rm ref} = \frac{\Phi_{\rm out}}{\Phi_{\rm nref}} = (NA_{\rm tune}(f) + NG_{\rm inj}(f))/(1 + A_{\rm tune}(f)) \approx NG_{\rm inj}(f)$$

$$TF_{\rm vco} = \frac{\Phi_{\rm out}}{\Phi_{\rm nvco}} = (1 - G_{\rm tune}(f))(1 - G_{\rm inj}(f)).$$

We now consider $G_{\rm inj}(f)$ in further detail, which is the key transfer function describing the injection-locking behavior of the PILO circuit described above. It was shown in [13] that $G_{\rm inj}(f)$ depends only on the reference frequency and the injection effectiveness, characterized by a factor β, resulting in the expression

$$G_{\rm inj}(f) = \frac{\beta}{1 + (\beta - 1)e^{-j2\pi \cdot f \cdot T_{\rm ref}}} e^{-j2\pi \cdot f \cdot T_{\rm ref}/2} \frac{\sin(2\pi \cdot f \cdot T_{\rm ref}/2)}{2\pi \cdot f \cdot T_{\rm ref}/2}. \quad (1)$$

Since the value of β corresponds to the injection effectiveness, it is a direct function of the switching properties in the case of the PILO. As shown in Fig. 13, the PILO switch is driven by short pulses of width D generated by the reference frequency source and has an "ON" resistance of $R_{\rm sw}$. Since the pulse is short, we can consider the inductor to be an open circuit during its operation. Also, we can ignore the equivalent parallel loss in the tank, R, under the assumption that $R_{\rm sw} \ll R$. As such, the right side of Fig. 13 indicates that we can approximate the influence of the switch on the oscillator tank as a simple *RC* circuit.

In the case where the oscillator is perfectly locked to the injection pulses, and D is extremely small, the switch would have no influence on the PILO tank since the voltage across the capacitor would be zero during the switch time under steady-state operating conditions. However, for the practical case where there is a slight frequency offset (e.g., due to noise) between the oscillator and the corresponding harmonic of the injection source, the effect of the switch is to discharge the tank capacitor voltage at the time of the switch activation, V_o, according to the *RC* model shown in Fig. 13. Assuming a rectangular pulse as shown in the figure, the relative change in tank capacitor voltage, ε, is given by

$$\varepsilon V_0 = V_0 \left(1 - e^{\frac{-D}{R_{\rm sw}C}}\right) \rightarrow \varepsilon = 1 - e^{\frac{-D}{R_{\rm sw}C}}. \quad (2)$$

It can be shown using simple trigonometry [10] that when the oscillator is close to its zero crossing, the relative change in its phase due to injection, i.e., β in (1), is approximately the same as the relative change in its voltage such that $\beta \approx \varepsilon$. The injection-locking bandwidth can approximately be found from (1) by fitting it to a first-order transfer function. It is worth noting that a more rigorous analysis similar to other works (e.g., [4], [15]) can be applied to a PILO to investigate its open-loop injection-locking properties.

Equation (2) reveals that the relative change in tank voltage, and thus the injection strength, increases by increasing the pulse width, or decreasing the switch resistance. Due to the exponential effect, the ability to increase ε by making the pulse width, D, larger starts to diminish as D approaches the value $R_{\rm sw}C$. Any benefit of further increase in D, which essentially leads to a higher injection-locking bandwidth, $f_{\rm inj}$, will be offset by an increase in random jitter due to the reduction of tank's Q and increase of deterministic jitter due to reference spurs. We can also increase ε by reducing $R_{\rm sw}$, which entails increasing the switch size, but this will lead to increased capacitance on the switch which results in an increased rise time of the pulse and corresponding reduction in the effective pulse width. Overall, the goal should be to aim for the smallest pulse width that can be reliably achieved, and set the size of the switch as large as possible (to reduce the value of $R_{\rm sw}$) without adversely impacting the pulse.

The interested reader should refer to [13] and [10] for a more detailed derivation of the noise model and the related expressions. In addition, MATLAB phase noise and CppSim behavioral models of the proposed architecture are available at http://www.cppsim.com.

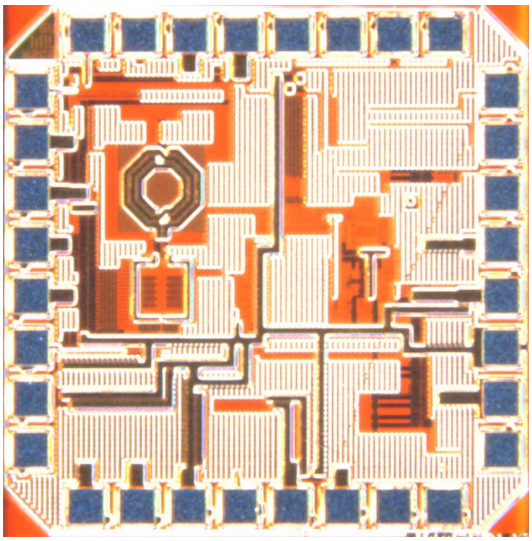

Fig. 14. Die photo.

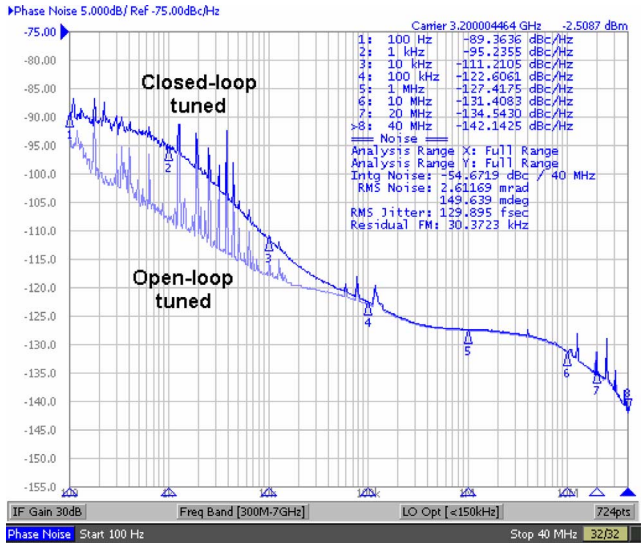

Fig. 15. Measured phase noise for the open-loop and closed-loop tuned PILO (at 3.2 GHz).

V. Measured Results

As shown in Fig. 5, the prototype of the continuously tuned PILO consists of a custom IC, FPGA, external DAC, and a simple *RC* filter. Fig. 14 shows the die photo of the custom 0.13 μm CMOS IC, which contains active circuit area of 0.4 mm^2. The power dissipation of the chip, not counting the output buffers, is 28.6 mW.

In order to isolate the noise added by the continuously-tuned PILO from the reference frequency signal that feeds it, a very clean reference frequency was generated by dividing down a 3.2 GHz signal produced by an Agilent 8257D signal source to a 50 MHz square wave signal. The resulting sharp edges of the square wave increased the immunity of the reference signal to corruption while being transported to the PILO circuit on the custom IC. The measured jitter of the 50 MHz reference signal was about 80 fs rms (integrated from 1 kHz to 20 MHz).

Fig. 15 displays measured phase noise of the PILO under open loop tuning (where its natural frequency was manually tuned to match the injection frequency), and closed-loop tuning of the PILO using the feedback technique described above. The integrated phase noise (from 100 Hz to 40 MHz) is 111 fs (rms) for the open-loop tuned case, and 130 fs (rms) for the closed-loop tuned case. Note that the impact of the reference spur is not included on those values. As observed in Fig. 15, the open-loop tuned PILO achieves low phase noise at low frequencies due to the fact that injection-locking leads to suppression of the low frequency VCO phase noise [6], [13], [15].

For either the open or closed loop case, it is important to note that the oscillator frequency is locked to the reference (i.e., there is zero average frequency difference between the oscillator and the associated reference harmonic), which is analogous to an integer-N PLL. The primary difference is that the open loop case will typically have a much larger reference spur and be vulnerable to previously mentioned problems as temperature varies. In contrast, the closed loop case leads to a much smaller reference spur and improved reliability at the cost of low frequency noise caused by the TDC measurement circuitry. To test the locking range, the reference frequency was swept after initial lock. For

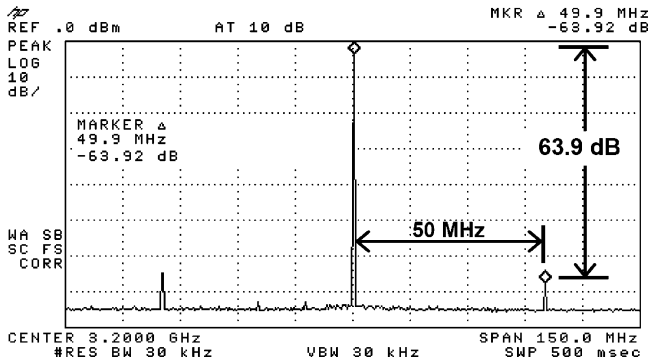

Fig. 16. Measured spurious performance of the close-loop tuned PILO (at 3.2 GHz).

the closed-loop case the oscillator stays locked throughout the entire tuning range of the oscillator's varactor at the selected capacitor bank (which is about 80 MHz in the prototype), whereas the open loop case offers a much narrower lock range (which is about a few megahertz in the prototype).

Compared to the open-loop tuned PILO, the closed-loop tuned PILO in Fig. 15 has higher noise at lower frequencies due to the detection noise added by the GRO TDC. However, the advantage of closed-loop tuned PILO is that it dramatically reduces deterministic jitter caused by periodic perturbation of the oscillator phase from the injection pulses. Reduction of the bandwidth of the closed-loop tuning is advantageous for lowering the impact of TDC noise, and is digitally set in the prototype without increased area or leakage as encountered in analog loops. The loop bandwidth needs to be set high enough to track thermal variations, and is set to about 1 kHz in this case, resulting in an increase in jitter due to the tuning loop of less than 20 fs (rms).

Comparison of the measured phase noise to the phase noise model discussed earlier leads to an estimate of the injection effectiveness, β, as somewhere between 0.65 and 0.75. Based on (1), this results in a value of $f_{\rm inj}$ of about 8 MHz. The GRO TDC raw and mismatch resolution are estimated at about 6 and 18 ps, respectively. Fig. 16 shows the -63.9 dBc reference spur

TABLE I
INTEGRATED PHASE NOISE OF VARIOUS CALCULATED NOISE CONTRIBUTORS

Phase noise Source	Reference	SD-DAC	GRO-TDC	VCO	Total closed-loop (calculated)	Total open-loop (measured)	Total closed-loop (measured)
Integrated phase noise (fs rms) (from 1 kHz to 20 MHz)	60	36	47	22	87	100	110

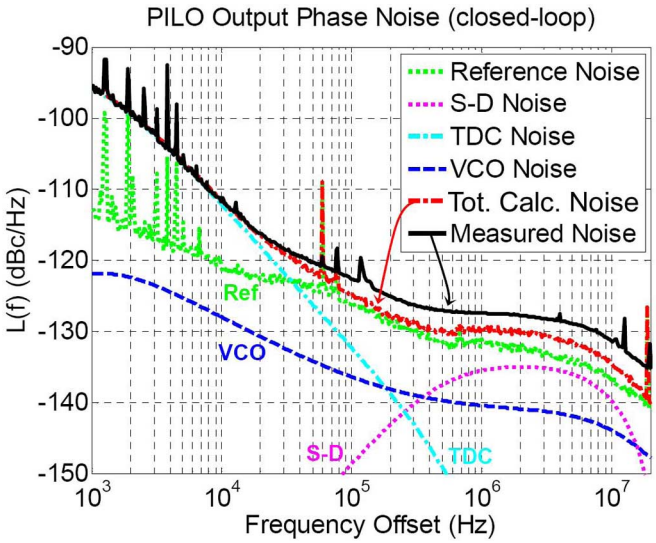

Fig. 17. Calculated output phase noise and associated noise contributions based on measured reference phase noise, calculated SD noise, estimated TDC noise, and estimated VCO noise, with measured overall noise superimposed, for the closed-loop tuned PILO (with BW $\approx$ 1 kHz).

occurring for the closed-loop tuned PILO that was measured by an HP 8595E spectrum analyzer, which corresponds to deterministic jitter estimated at approximately 200 fs (peak-to-peak).

Finally, to gain an insight on the contributions of various noise sources and verify the noise model, the measured reference phase noise, in addition to measured and estimated parameters of the architecture, were used to calculate the closed-loop phase noise of the PILO and compare it to the measured result, as shown in Fig. 17. In addition, Table I lists the integrated phase noise of the various noise sources (integrated to 20 MHz only, due to the limited frequency span of the measuring instrument at the 50 MHz reference frequency).

The VCO phase noise (free running) was measured to be about -148 dBc@20 MHz with a 200 kHz $1/f^3$ corner, which results in a calculated VCO noise contribution well below the measured phase noise, and a noise contribution of only 22 fs (rms). Given the low VCO contribution, the gap between the calculated and measured phase noise at high-frequency points to a missing noise contributor that is not accounted for in the figure. That missing source is the additional reference noise added by the reference buffer, pulse generator and possibly noise coupling. A good fit was reached by adding a flat phase noise of -167 dBc/Hz to the reference (i.e., at 50 MHz), which is a reasonable level, and within the range of expected jitter from simulation. The buffer added 67 fs (rms) to the reference noise, making its total at 90 fs (rms). This reveals the importance of using a low jitter reference and the care needed for buffering it to achieve low phase noise for the injected-locked oscillator.

VI. CONCLUSION

This paper presented a low jitter, highly digital, continuously tuned PILO architecture that leverages subharmonic injection-locking of an *LC* oscillator to achieve low jitter clock multiplication. The unique aspects of this work include the use of a shorting switch rather than current pulse injection to achieve injection locking of an *LC* oscillator, and a method to achieve continuous tracking of the natural frequency of the oscillator to the desired harmonic of the reference that it is locked to. Measured results from a custom prototype yield 130 fs (rms) of random jitter (corresponding to integrated phase noise from 100 Hz to 40 MHz) and 200 fs (peak-to-peak) deterministic jitter (corresponding to a -63.9 dBc reference spur) from a 3.2 GHz output and 50 MHz reference frequency. Therefore, the proposed structure offers a very promising approach for low jitter clock multiplication in cases where a clean reference signal is available. Note that a possible future research direction is to leverage a mode-locked laser source as the reference pulse source due to its ability to generate very short (optical) pulses with extremely low jitter [16].

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