An efficient high-resolution 11-bit noise-shaping multipath gated ring oscillator TDC

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Abstract

An 11-bit, 50-Msps time-to-digital converter (TDC) using a multipath gated ring oscillator (GRO) with 6ps of delay per stage achieves low power (2.2 to 21mW) and small area of 160x260µm in 0.13µm CMOS. The structure also achieves first order noise shaping of the GRO quantization and mismatch noise; the resulting TDC error integrates to < 100 fs (rms) in a 1 MHz bandwidth to achieve dynamic range of over 90dB with no calibration required.

Introduction

Digital phase-locked loops (PLL) provide many implementation advantages compared to their analog counterparts by avoiding large capacitors for loop filters and the complications of designing analog-intensive components such as charge pumps. Achieving high performance in such systems rests on their time-to-digital converter (TDC), which is used to measure the instantaneous time difference between the edges the PLL output and an input reference frequency.

Similar to ADC structures, the desired properties of TDC implementations are to achieve high resolution in time measurement with large dynamic range while simultaneously achieving a low power and area implementation. In this paper we present techniques to achieve low power and area for a recently introduced multi-phase gated ring oscillator (GRO) TDC [1].

Multipath Gated Ring Oscillator Core

Fig. 1 illustrates the basic concept of a GRO-TDC as first presented in [2]. The key idea is to measure time by enabling a ring oscillator during the measurement interval and counting the number of transitions. By preserving the oscillator state in between measurements, the *overall* quantization error can be described as *Error[k]=q[k]–q[k-1],* where *q[k]* and *q[k-1]* correspond to the *current* and *previous* quantization error, respectively. The difference operation on *q[k]* reveals first order noise shaping of the quantization noise, and it turns out that mismatch between delay stages is also first order noise shaped due to barrel shifting through the delay stages.

Improved performance for the GRO can be achieved by using a multipath structure (Fig. 2) as proposed in [1]. This approach allows reduction of the delay per stage to 6ps in 0.13u CMOS by connecting the inputs for each stage to a *combination* of previous delay stages. In [1], the proposed GRO has 47 identical stages, each consisting of a core of two PMOS and three NMOS transistors that can be disconnected from the supply to enable the gating functionality.

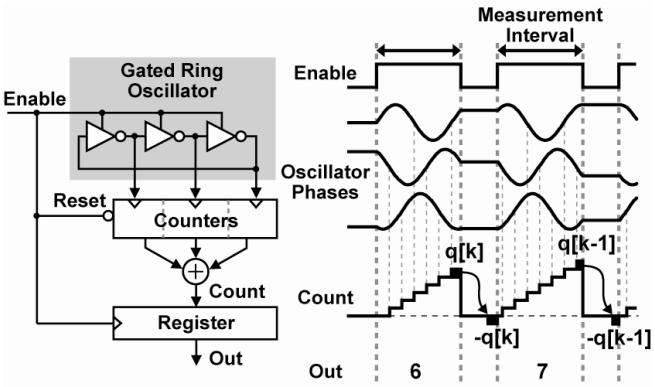

Fig. 1. Concept of gated ring oscillator TDC with first-order noise shaping

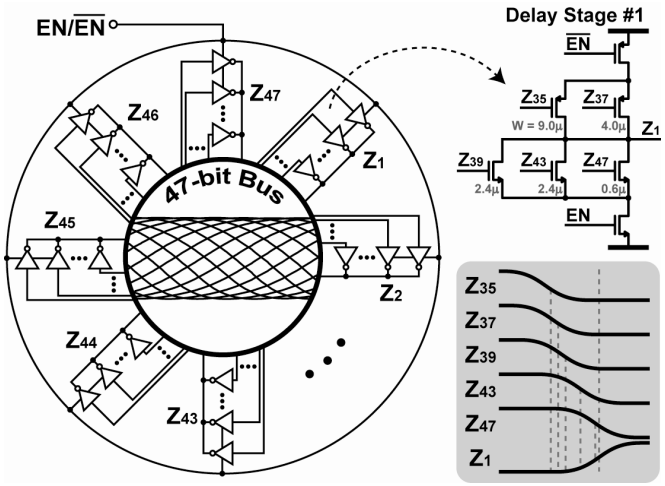

Fig. 2. Proposed multipath GRO with 6ps of delay per stage

Efficient Phase Measurement Circuitry

A key implementation challenge of the proposed GRO in [1] is to efficiently count the number of transitions that occur in a given measurement cycle. While the simple counter approach shown in Fig. 1 could be used, a total of 94 counters would be required for the multipath GRO, which would be costly in power. To reduce this power, in theory, we could use a single counter to keep track of phase wrapping, and then sample the oscillator state in order to calculate the phase residue. Unfortunately, as depicted on the left side of Fig. 3, the sampled state of the full GRO is unreliable since *multiple* outputs are transitioning at any instant. To solve this issue, we propose partitioning the GRO outputs into cells (with one counter each) so that within each cell only *one* input transitions at a time. Shown on the right side of Fig. 3, the

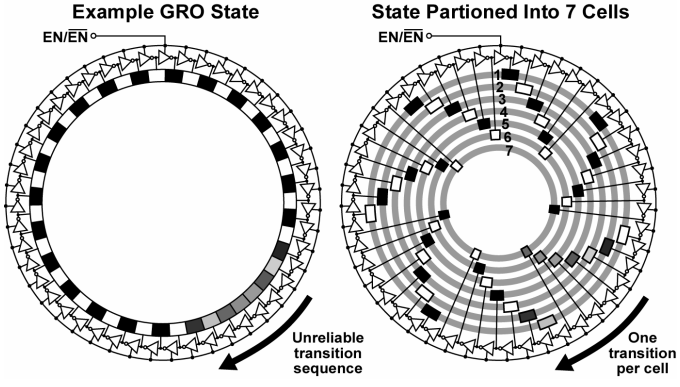

Fig. 3. Partioning the GRO outputs into cells to allow for a reliable state-to-phase mapping

prototype design has 6 identical cells (Nos. 1-6) each with 7 inputs, and with one cell (No. 7) with 5 inputs. Therefore, only 7 counters are required in this design, each of which operates at the nominal GRO frequency of 1.8GHz. The overall GRO-TDC block diagram is shown in Fig. 4.

Another critical aspect of the GRO-TDC is that noise shaping will be corrupted if errors are made by the cell in counting the phase wraps. The key challenge in this regard is to remove glitches at the counter inputs that can occur when a GRO output voltage is held near a logical threshold in the disabled state. To explain, after disabling the GRO, charge re-distribution in the inverter core alters the corresponding output voltages such that a threshold can be crossed more than once. This issue is addressed with the circuit shown in Fig. 5. To explain its operation, first consider that a clock signal non-overlapping with the enable pulse (Fig. 4) is used to confine the possible transition activity at the counter input to a window approximately equal to the enable state. Second, a de-glitch circuit utilizes the known sequence of GRO states to make certain the counter input sees exactly one positive transition per GRO cycle. Lastly, the counter output is read with a delayed clock to satisfy a worst-case timing. After the GRO states are sampled with a master-slave DFF (comprised of the two D-Latches shown), the overall transition count is computed by summing the scaled counter output with the phase residue, and then taking the first order difference to compute the overall output for a given measurement interval.

Measurements

The prototype TDC was designed and fabricated in 0.13µm CMOS. The 1x1mm chip has an active area of only 160x260µm (0.04mm^2). A 1.5V supply is used for measurements, although operation was verified from 1.0-1.6V. The TDC current is a linear function of the average measurement time, and ranges from 1.5-14mA (2.2-21mW).

Fig. 6 shows both the frequency and time domain GRO-TDC 50-Msps output with a 26kHz input of 1.2ps$_{pp}$ in addition to a time offset of about 1.6ns. The 65,536pt FFT is performed with a Hanning window on 20 sequential collects before being averaged to result in the double-sided power spectral density as shown. Noise shaping of more than 20dB is clearly evident, with 1/f noise dominating at low frequency. The shaded horizontal line in Fig. 6 corresponds to a 50-Msps classical quantizer (i.e. no noise shaping) with 1ps steps. However, by looking at the time domain output after digitally

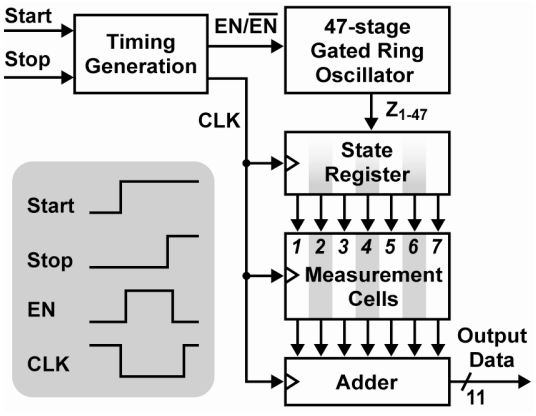

Fig. 4. Overall block diagram of proposed GRO-TDC

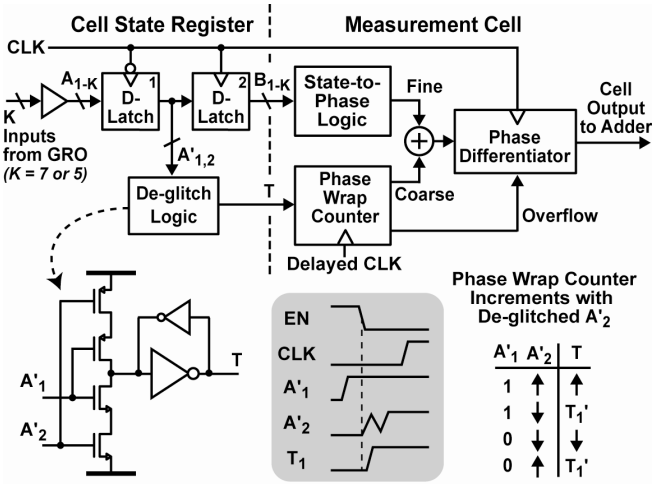

Fig. 5: Circuit schematic for phase measurement including glitch-free phase wrap counting

filtering with a 1MHz bandwidth (Fig. 6), the GRO-TDC is clearly able to resolve a 1.2ps$_{pp}$ signal whereas a classical quantizer with 1ps resolution would struggle due to the lack of quantization noise scrambling. In fact, the integrated noise of the GRO-TDC from 2kHz to 1MHz is below 100fs$_{rms}$. With a full-scale of 11-bits, the dynamic range in a 1MHz bandwidth is calculated to be over 90dB.

References

[1] C-M. Hsu, M. Straayer, M. Perrott, "A Low-Noise, Wide-BW 3.6GHz Digital ΣΔ Fractional-N Frequency Synthesizer with a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation," *ISSCC Dig. Tech. Papers*, Feb. 2008

[2] B. Helal, M. Straayer, M. Perrott, "A Low Jitter 1.6 GHz Multiplying DLL Utilizing a Scrambling Time-to-Digital Converter and Digital Correlation" *VLSI Symp. Dig. Tech. Papers*, pp. 166-167, June 2007

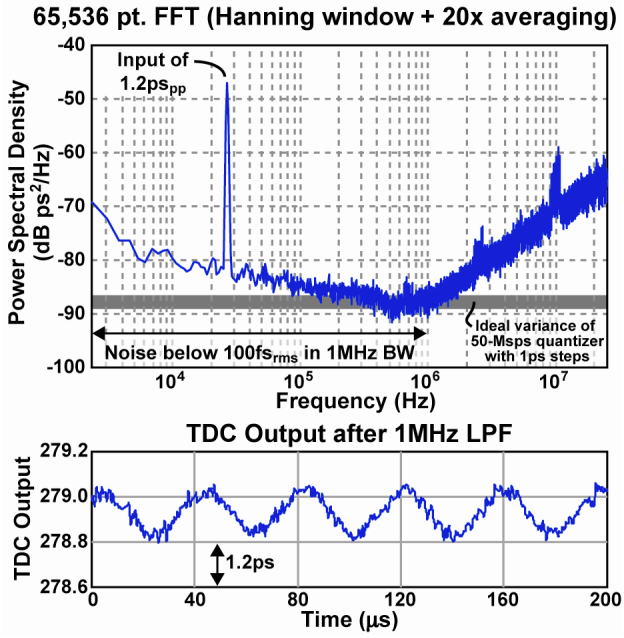

Fig. 6. Measured TDC output with a 1.2ps$_{pp}$ input at 26kHz