A 10-bit 20MHz 38mW 950MHz CT ΣΔ ADC with a 5-bit noise-shaping VCO-based Quantizer and DEM circuit in 0.13u CMOS

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Abstract

A combined 5-bit, 1st order noise-shaped quantizer and DEM circuit running at 950MHz based on a multi-phase VCO is presented. This quantizer structure is the key element in a 3rd order noise shaped ADC with 2nd order loop dynamics and a single opamp. Measured performance is 60dB SNR at 20MHz bandwidth in 0.13u CMOS while consuming 32mA from a 1.2V supply.

Introduction

High-speed CT ΣΔ ADC implementations face many challenges, including higher order noise shaping in the presence of excess loop delay and inclusion of low power dynamic element matching (DEM) circuits. To address such issues, we propose a combined 5-bit, 1st order noise-shaped quantizer and DEM circuit running at 950MHz based on a multi-phase VCO. As illustrated in Fig. 1, we combine this structure with a feedback structure consisting of two 5-bit current DACs and a single opamp to achieve a 3rd order noise-shaped ADC with 60dB SNR at 20MHz bandwidth in 0.13u CMOS which draws 32mA from a 1.2V supply. The proposed ADC architecture differs from prior work using a VCO to perform quantization [1-4] in that we achieve *both* 1st order noise shaping of the quantization noise and 1st order DEM control of multi-bit, thermometer-coded DAC circuits within a *single structure* that allows high frequency operation with compact area and low power.

VCO-based Quantizer and DEM Circuit

Fig. 2 illustrates the concept of achieving 1st order noise shaping with a VCO-based quantizer [1,2]. As shown, the relative phase of the output edges of a VCO compared to a reference clock is altered according to the *integral* of the input voltage signal. Unlike conventional integrators, the VCO phase never saturates (though one must keep track of phase wrapping), and quantization of this signal is achieved by progressively counting the number of VCO edges that occur up to the time of a given reference edge. Ideally, the resulting quantization noise of the phase signal is white. Differentiation of the quantized phase signal, Φ_q, yields a quantized frequency signal, ω_q, whose quantization noise is 1st order noise shaped. The use of a multi-stage VCO allows for reduction of the quantization noise by allowing increased resolution in the counting process.

While the quantizer shown in Fig. 2 is very efficient at achieving noise shaping and multi-bit operation, it suffers from the nonlinear relationship between the input voltage and output frequency of a practical VCO [2]. To improve the linearity, we surround the structure with feedback corresponding to a 2nd order ΣΔ ADC as shown in Fig. 1. The 1st order noise shaping property of the quantizer allows us to achieve 3rd order noise shaping with only a 2nd order ΣΔ

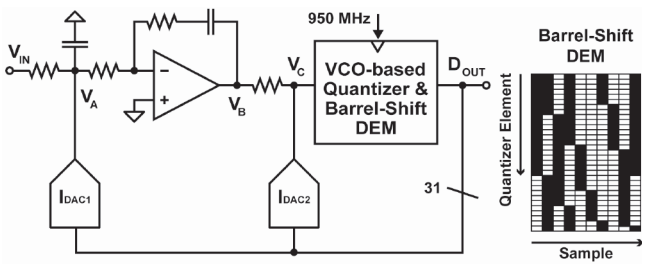

Fig. 1. Simplified block diagram of the proposed ADC

structure, which allows improved robustness in the presence of excess loop delay compared to classical 3rd order ΣΔ structures. As indicated in Fig. 3, we simply hard-wire each quantizer output to a corresponding DAC element to achieve the barrel-shifting operation required for 1st order DEM control of both 5-bit current DACs used in the feedback.

When accounting for process variations, the VCO-based quantizer requires coarse tuning of its offset to achieve its full dynamic range. To understand this issue, consider that application of a zero input into the overall ADC, as shown in Fig. 1, causes the differential control voltage, V_C, to adjust the VCO frequency to $F_S/4$ (where F_s is the sample rate of the ADC) such that an equal number and 1's and 0's are present over time. Ideally, the $F_S/4$ frequency is achieved with V_C equal to zero in order to center the range of the quantizer input and minimize second order distortion. Fortunately, due to the high sensitivity of the VCO frequency to V_C, we can tolerate a small offset on V_C without severe consequence since the differential full scale range of the quantizer is achieved with only +/- 300 mV_{pp} range on V_C, which is smaller than the output range of the opamp and I_{DAC2} that feed the quantizer input. As such, 2-bits of coarse tuning on the VCO delay stages are sufficient to achieve reasonable centering of V_C across process variations.

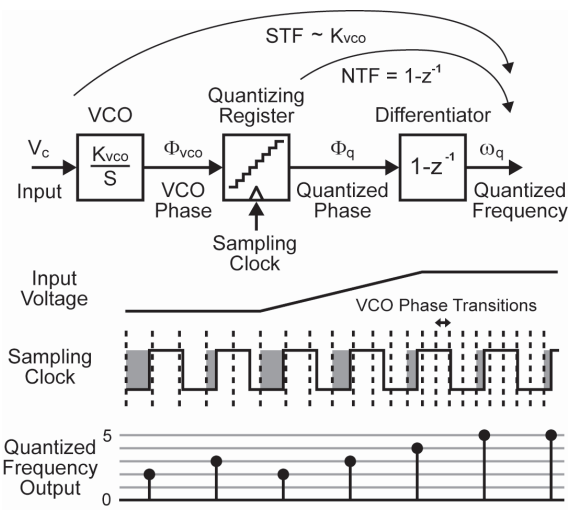

Fig. 2. VCO quantizer noise shaping concept

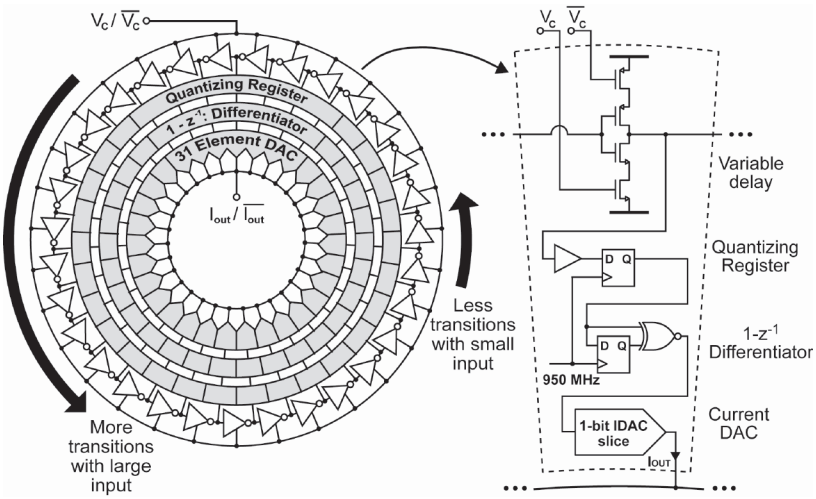

Fig. 3. Implementation of the VCO quantizer / DEM structure

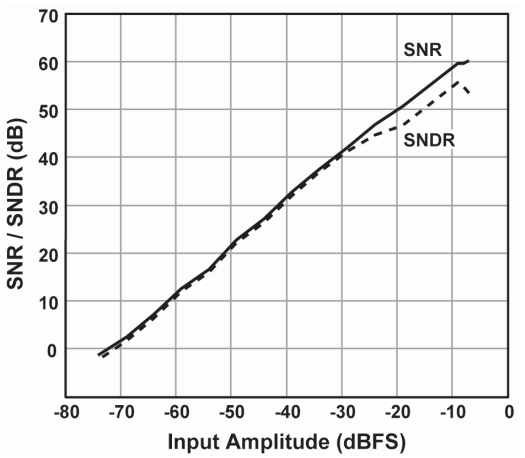

Fig. 4. Measured SNR and SNDR vs. amplitude

ADC Design

The 31 bit-wise connected elements of I_{DAC1} are used to feedback the output of the quantizer to the input of the ADC. Degenerated current sources are used to reduce 1/f noise, and RZ pulses are formed by using full-logic switch control signals derived from the sampling clock.

To prevent the large current deviations of I_{DAC1} from hurting the distortion performance of the ADC, a passive filter with a few MHz of bandwidth is included at the front end of the ADC as shown in Fig. 1. There is a negligible noise penalty from including the additional resistance at the ADC input.

Although the loop is only 2nd order, appropriate compensation is desired to mitigate the effects of excess loop delay and parasitic poles which degrade the loop phase margin. To estimate the delay of the quantizer/DEM operation, note that V_C is integrated over the previous sampling period and that the I_{DAC1} pulse begins on the negative edge following the quantizer transition. The combination of these effects leads to a total excess loop delay of approximately $z^{-1.25}$. To compensate for this delay, a minor feedback loop is formed by adding the current output of I_{DAC2} (NRZ) to the voltage output of the opamp prior to the quantizer through the resistor show in Fig. 1. The parasitic pole created by the resistor and VCO input capacitance is high in frequency and well compensated by the minor loop.

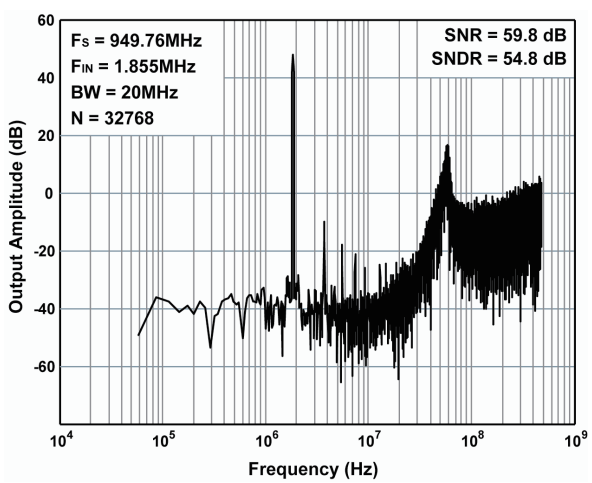

Fig. 5. Measured output FFT spectrum (Hanning window)

Measurements

The ADC demonstrates 60dB SNR and 55dB SNDR with 20 MHz of input bandwidth as shown in Fig. 4 for a 1.855MHz input signal and 950MHz sample rate. Input frequencies from 500KHz to 7.5MHz were also tested and demonstrated similar performance. With a power consumption of 38mW (excluding decimation, which was not implemented on-chip), the conversion efficiency is 1.1pJ/bit. The output spectrum of the ADC is shown in Fig. 5 using a Hanning windowed 32,768 point FFT.

A microphotograph of the 1x1mm chip with 20 pads is shown in Fig. 6. The active area of the converter not including decoupling capacitors is 500x370µm.

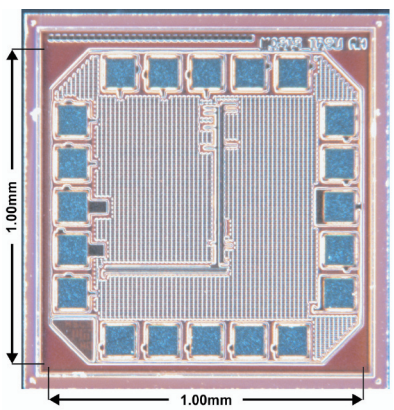

Fig. 6. Measured SNR and SNDR vs. amplitude

References

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