SP 22.2: A 27mW CMOS Fractional-N Synthesizer/Modulator IC

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A 1.8GHz transmitter supports a data rate of 2.5Mb/s using GFSK with BT=0.5, the same modulation method used in DECT. The architecture increases, by over an order of magnitude, the achievable data rate for a transmitter method described in Reference 1, in which phase/frequency modulation is by dithering the divide value within a phase locked loop (PLL). This design avoids mixers and D/A converters to generate I and Q waveforms, so that simplicity and power savings are achieved. The system depicted in Figure 1 was built using a custom, CMOS fractional-N synthesizer that contains several key circuits. Included are an on-chip, continuous-time filter that requires no tuning or external components, a digital MASH $\Sigma\Delta$ converter that achieves low-power operation through pipelining, and a 64-modulus divider that supports any divide value between 32 and 63.5 in half cycle increments. Also included is a phase/frequency detector (PFD) from Reference 2 that avoids dead-zone problems.

The theory of the proposed method is illustrated in Figure 2, that shows a linearized model of the transmitter. To obtain a simple PLL implementation, its transfer function is chosen to have a second-order rolloff with a natural frequency of f_0. To adequately attenuate quantization noise produced by the $\Sigma\Delta$ converter, a low value of f_0 relative to the PLL reference frequency of 20MHz is required. In this case, f_0 is 84kHz. Unfortunately, the resulting PLL bandwidth is over an order of magnitude too low to pass the modulation data at 2.5Mb/s. To overcome this obstacle, a digital compensation filter is used to 'flatten' the PLL transfer function seen by the modulation signal. Implementation of this filter is by modifying the Gaussian transmit filter used to produce GFSK modulation. The compensation increases the dynamic range of data coming into the $\Sigma\Delta$ converter, which is dealt with by using a converter with 6 output bits and a 64 Modulus divider.

The requirement for a multiple output bit $\Sigma\Delta$ converter allows the use of the MASH architecture, which can be pipelined using the method illustrated in Figure 3. Substantial power savings are obtained by this approach since it allows the required throughput rate to be achieved with lower circuit speed, thus permiting reduction of the converter power supply voltage. To explain, the top of Figure 3 shows a 3b integrator whose adder has been pipelined so carry bits propagate through only one bit stage during each clock cycle. To accomodate the delay of carry information into more significant bits, appropriate delays are added to the integrator input bits. The resulting output bits are realigned in time by placing delays in their path as well. This technique increases latency in the converter, permissible for any order MASH architecture since there is no global feedback. The bottom of Figure 3 shows this approach applied to the second-order case. The circuit is similar to the figure but is pipelined every two bits. The $\Sigma\Delta$ converter and preceding adder, shown in Figure 1, operate at 20MHz at 0.33mW with a supply voltage of 1.25V.

A 64 modulus divider is created by cascading a chain of divide by 2/3 state machines with a high-speed divide by 2/2.5/3/3.5 state machine as shown in Figure 4. The half-cycle divide values are by multiplexing the four phase output of a divide by 2 circuit. Similar in principle to that found in Reference 3, this design allows single cycle increments of division of the VCO frequency when a preceding divide by 2 prescaler is used. The inclusion of the prescaler reduces the operating frequency of the divider, and changes the range of divide values to all integers between 64 and 127. The divider, along with its input amplifiers, operates at 930MHz at 22mW with a 3V supply.

To obtain good matching between the digital compensation filter and PLL dynamics, tight control over the PLL transfer function is achieved through the use of an accurate, on-chip, continuous-time loop filter with adjustable gain to compensate for variations in VCO gain. Shown in Figure 5, the design feeds output currents from a charge pump into the inputs of an opamp that integrates one current and adds to it a first-order filtered version of the other current. The first-order pole, w_p, is created using a switched capacitor technique that reduces its sensitivity to thermal and process variations and removes need for tuning. The output of the first-order filter, the voltage across $24 \cdot C$, is a continuous-time signal even though the filter time constant is formed through a sampling operation. The rate of sampling $24 \cdot C$ can be high, since it is independent of the settling dynamics of the opamp, and is set equal to the frequency of the PFD output, ϕ, to avoid aliasing problems. As for the charge pump, the best dynamic range for modulation is achieved when a 50% duty cycle in ϕ produces zero average output current. To obtain a low offset in this regard, feedback is used to control the tail current in the charge pump, and its differential outputs are held at the same voltage by the action of the loop filter opamp. This also leads to an accurate setting of the zero, w_z, since the charge-pump currents are closely matched. The charge pump and loop filter, supporting bias circuitry, and 5b D/A converter operatewith a 3.3V supply, and consume a total of 2.4mW.

The fully-functional synthesizer chip, with external components shown in Figure 1, generate the eye diagram and output spectrum in Figure 6 as measured by an HP 89441A.

Acknowledgments:

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[2] Thamsirianunt, M., T. A. Kwasniewski, "A 1.2μm CMOS Implementation of a Low-Power 900-MHz Mobile Radio Frequency Synthesizer," IEEE Custom IC Conf., 1994.

[3] Craninckx, J., M. S. J. Steyaert, "A 1.75-GHz/3-V Dual-Modulus Divide-by-128/129 Prescaler in 0.7μm CMOS," J. Solid-State Circuits, July, 1996.

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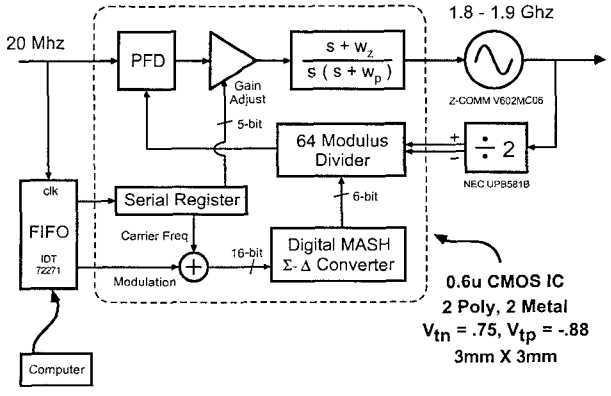

Figure 1: Transmitter test system.

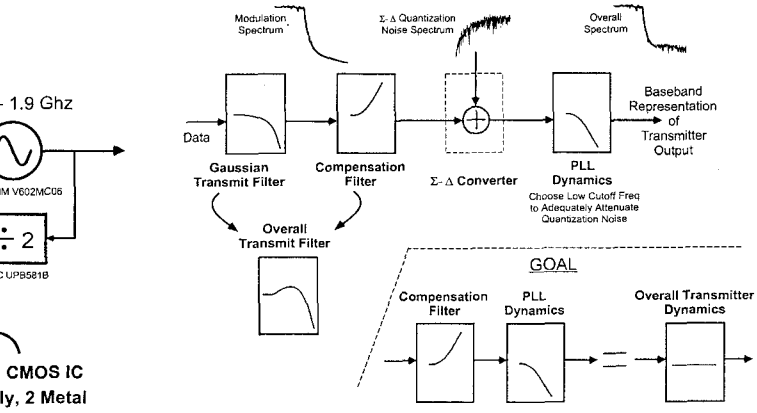

Figure 2: Linearized model of transmitter.

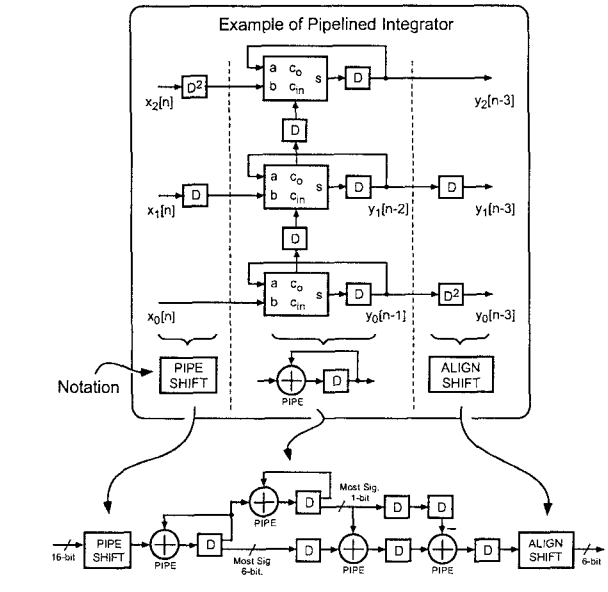

Figure 3: Pipelined MASH S-D converter.

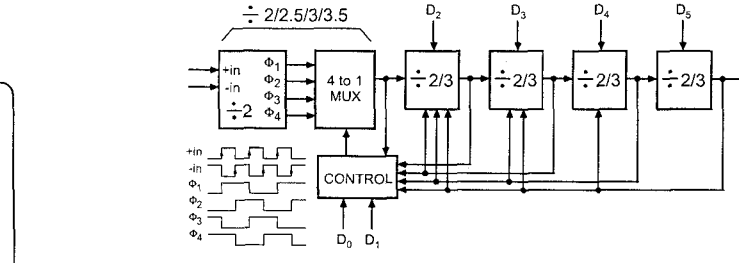

Figure 4: Block diagram of 64 modulus divider.

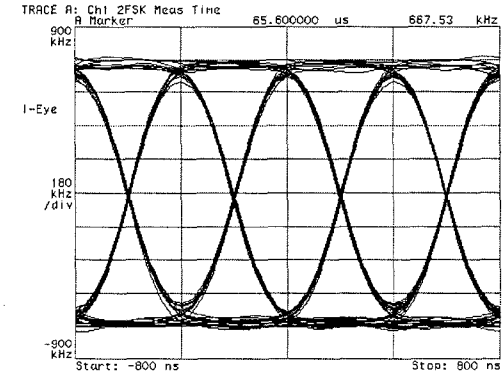

Figure 6: Measured results.

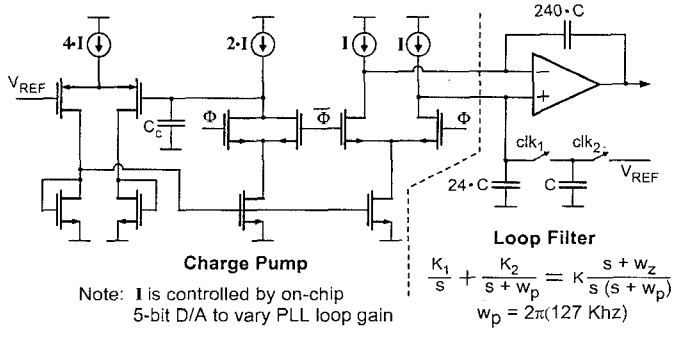

Figure 5: Implementation of loop filter.

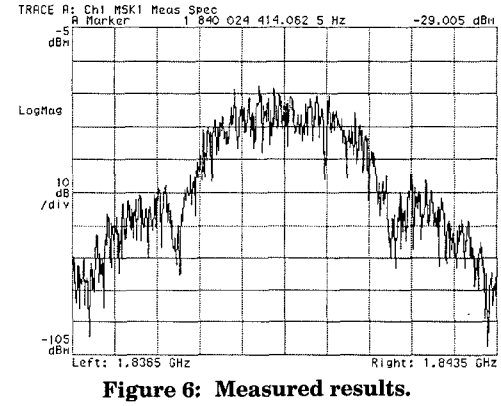

Figure 7: See page 487.

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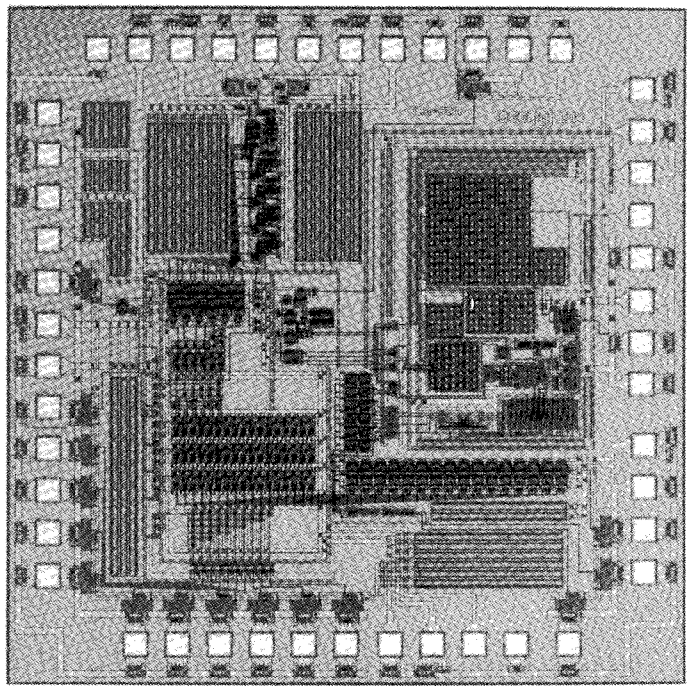

Figure 7: Chip micrograph.

SP 22.3: A 12mW Wide Dynamic Range CMOS Front-End for a Portable GPS Receiver

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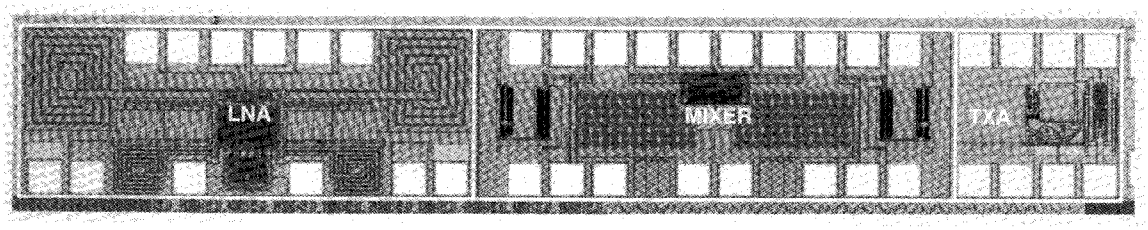

Figure 6: Die micrograph.