13.1 A Low-Area Switched-Resistor Loop-Filter Technique for Fractional-N Synthesizers Applied to a MEMS-Based Programmable Oscillator

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MEMS resonators have recently emerged as an alternative structure to crystal resonators in providing frequency references which achieve better than 50 ppm accuracy over the industrial temperature range. As illustrated in Fig. 13.1.1, a programmable oscillator utilizing a MEMS resonator is achieved by wire bonding a MEMS resonator die to a CMOS die that contains an oscillator sustaining circuit, temperature sensor, fractional-N synthesizer, and various digital blocks. The output of the sustaining circuit provides a 5 MHz reference frequency to the fractional-N synthesizer, which outputs a higher frequency that can be digitally adjusted with sub-ppm resolution over a >10% tuning range. By then sending the fractional-N synthesizer output into a programmable frequency divider (i.e., divide-by-N circuit), any frequency in the range of 1 to 115 MHz can be achieved by proper combination of the fractional-N synthesizer and programmable divider settings.

As shown in Fig. 13.1.1, the sub-ppm tuning capability of the fractional-N synthesizer enables straightforward compensation of frequency deviation in the MEMS resonator due to temperature variation. In particular, a temperature sensor on the CMOS die is utilized in combination with digital logic that performs polynomial multiplication of the digitized temperature value in order to compensate for curvature in the MEMS frequency variation across temperature. The MEMS resonator utilized in this work has sufficient part-to-part consistency in its temperature to frequency characteristic such that better than 50 ppm accuracy can be achieved from -40 to 85 degrees C.

Figure 13.1.2 displays a block diagram of the fractional-N synthesizer, which includes a phase detector (PD), loop filter, VCO, frequency divider, and Σ–Δ modulator. In practice, loop filter noise (which includes charge pump noise for conventional PLLs) can dominate the phase noise profile of a PLL at low frequency offsets unless large capacitance is utilized within the loop filter. To lower the impact of such noise without requiring a large capacitance, we propose increasing the gain of the PD. While previous techniques have achieved higher PD gain for integer-N synthesizers using sampling detectors [1], we propose a technique that is suitable for fractional-N synthesizers and works by decreasing the effective range of the PD by utilizing a higher frequency divider output [2]. As shown in Fig. 13.1.2, the decreased PD range leads to a higher slope in the PD characteristic, so that higher PD gain is achieved.

While the higher gain PD could be utilized within a conventional charge pump PLL structure, we propose the switch resistor loop filter shown in Fig. 13.1.3. This loop filter structure requires only CMOS switches, resistors, and capacitors, and can approximate a lead-lag filter response with the constraint that the DC gain is no greater than one. The constraint in DC gain is compensated by having a higher PD gain and a relatively high VCO K_v value, though the average PD error will change according to the VCO frequency as with a Type I PLL. By utilizing several stages of switches, charge is gated to the VCO control input (i.e., C_3) in a manner that lowers reference spurs [3]. Also, frequency acquisition time is improved by directly gating charge to C_3 using the simple switched capacitor network shown in Fig. 13.1.3. Since the switched capacitor network is not active once the PLL is in lock, this technique poses neither a power nor noise penalty to the PLL in steady state conditions. Overall, compared to the classical charge pump PLL, the proposed switched resistor topology offers a relatively simple design that requires no bias currents and reduced analog design effort.

Figure 13.1.4 illustrates the implementation of the switches, which consist of NMOS and PMOS transistors that are sized such that the worst case switch resistance is less than 10% of the poly resistance that they switch. As indicated by the figure, pulsing the resistor acts to boost its *effective* resistance since the average current through the resistor will be reduced according to the ratio of the pulse on-time, T_{on}, to its period, T_{period}. The benefit of this resistance boost is a reduction in area required to achieve a given RC time constant in the loop filter. In practice, charge that has been stored on parasitic capacitance of the switch and poly resistor will drain through the resistor even when the switch is off, which increases the average current through the resistor and therefore lowers its effective resistance. However, detailed SPICE simulations reveal that the effective resistance can easily be increased by over an order of magnitude above the poly resistance value through proper choice of T_{on}/T_{period}.

A simplified view of the phase/frequency detector (PFD) is shown Fig. 13.1.5. Here the divider output, whose frequency is four times that of the reference, is used to clock through the reference edges in order to create non-overlapping pulses for the PD. As indicated in Fig. 13.1.2, the Up and Down pulses change in width in opposite directions according to the phase difference between the Reference and associated Divider output edges. The Last pulse is designed to have a low T_{on}/T_{period} ratio as to achieve a high effective resistance of 16 Megaohms for R_3 (where R_3 is a 500 kOhm poly resistor that is indicated in Fig. 13.1.3), which provides an adequately low zero for the PLL to be stable without requiring large capacitance. Finally, the frequency detector (FD) essentially checks if four divider rising edges occur per reference period, and pulses the FD outputs appropriately if this condition is not met. Once the PLL is in lock, the FD output signals automatically become inactive so that capacitor C_c remains disconnected from C_3 (see Fig. 13.1.3) under steady-state conditions.

Figure 13.1.6 shows measured phase noise at 100 MHz output frequency at room temperature, and also shows the stability in output frequency as temperature is varied from -45 to 90 degrees for 100 parts after single-temperature calibration. The phase noise plot reveals that the PLL bandwidth is ~30 kHz, the reference spur is -65 dBc, and integrated phase noise (1 kHz to 40 MHz) is 16.7 ps rms. Frequency stability is better than 50 ppm across the industrial temperature range.

Figure 13.1.7 shows the 0.18µm CMOS die, which measures 1.5 by 1.65 mm, with the MEMS die wire-bonded on top. By utilizing conventional wafer grinding techniques to thin the CMOS and MEMS dies [4], the stacked CMOS/MEMS die structure is placed in standard 0.75 mm thick plastic QFN packaging. The entire fractional-N PLL, including the loop filter but excluding the LC VCO and buffer, has an area of 0.09 sq. mm., while the LC VCO and buffer has an area of 0.22 sq. mm. The current consumption of the entire chip is measured to be 3.2/3.7 mA (typical) at 1.8/3.3 V supply assuming 20 MHz output with no load. Of this total current consumption, the VCO and buffer is estimated to consume 1.3 mA and the rest of the PLL is estimated to consume 0.7 mA based on SPICE simulations.

Acknowledgements:
Thanks to Pavan Gupta for the die photo, and Mike Ludwig and Jimmy Nguyen for layout.

References:
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 978-1-4244-6034-2/10/$26.00

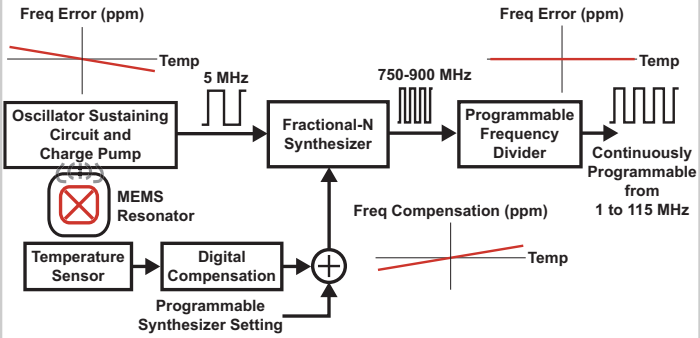

Figure 13.1.1: MEMS-based oscillator circuit consisting of a MEMS die wire-bonded to a CMOS die with sustaining circuit, frac.-N synthesizer, programmable frequency divider, and temperature compensation circuits.

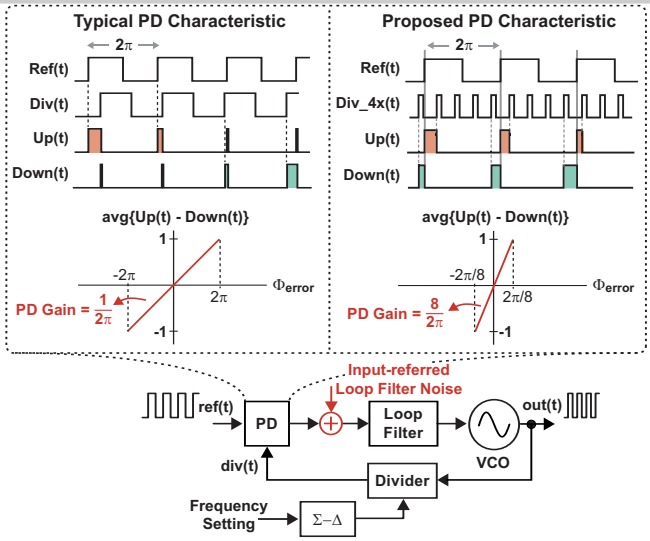

Figure 13.1.2: Block diagram of fractional-N synthesizer with focus on increasing the phase detector (PD) gain by reducing its effective range.

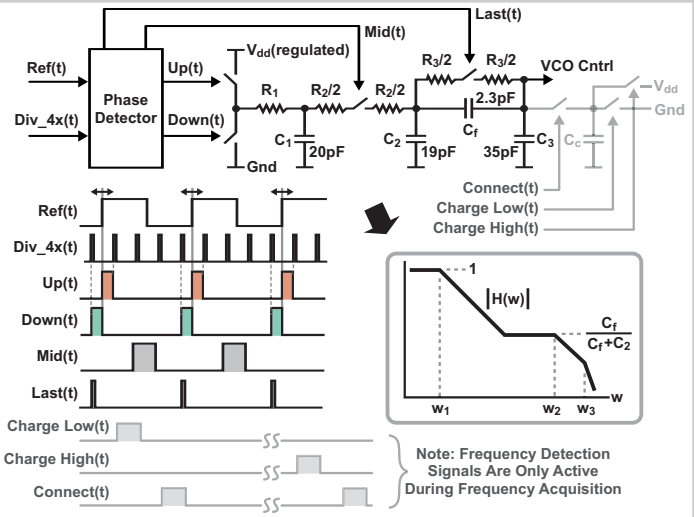

Figure 13.1.3: Proposed switched resistor loop filter, which approximates a lead-lag filter using all passive devices and CMOS switches. Freq. detection is performed with switched capacitor circuit shown in lighter shade.

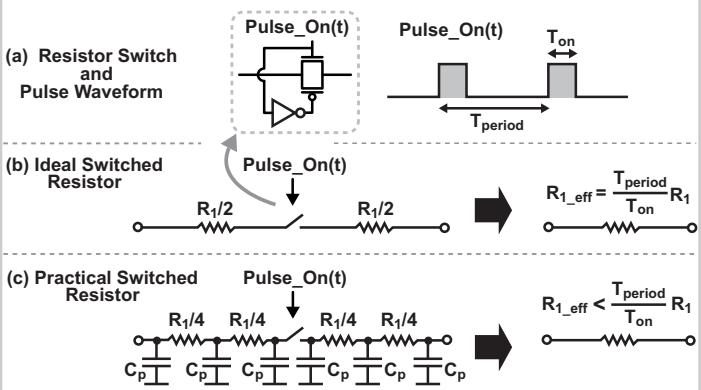

Figure 13.1.4: Implementation of switched resistor using CMOS devices and poly resistors, along with impact of pulsed switching and parasitic capacitance on the effective resistance.

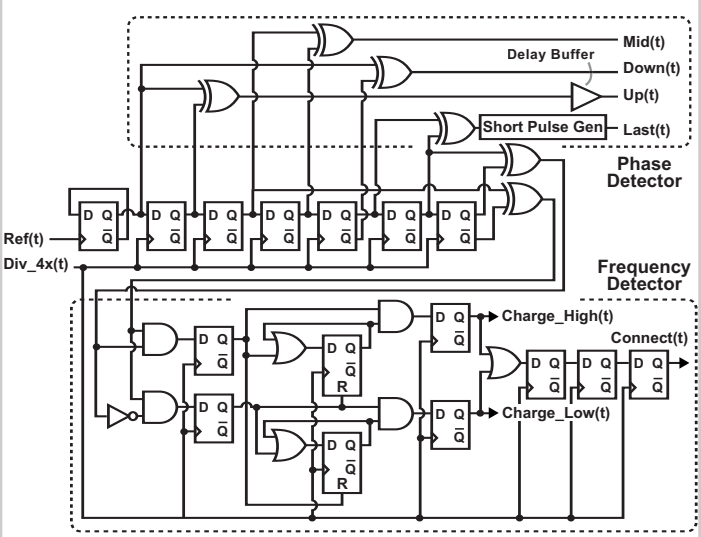

Figure 13.1.5: Simplified schematic of phase and frequency detectors.

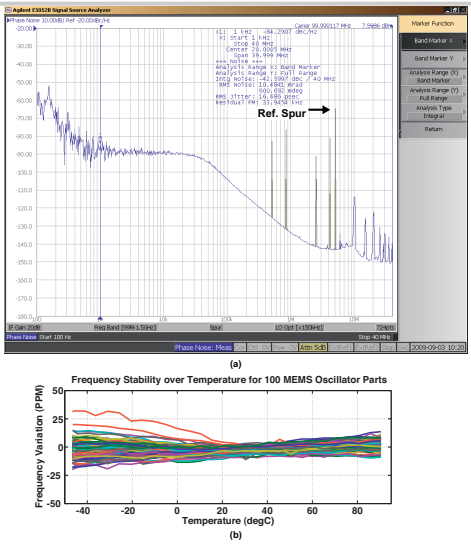

Figure 13.1.6: Measured results for (a) phase noise (measured at 100 MHz output frequency) and (b) frequency stability versus temperature.

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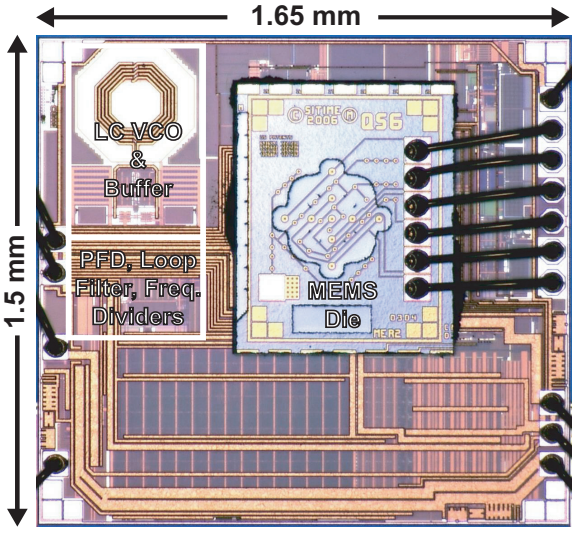

Figure 13.1.7: Micrograph of the 0.18µm CMOS die with MEMS die attached on top.

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