18.2 A 2.5Gb/s Multi-Rate 0.25μm CMOS CDR Utilizing a Hybrid Analog/Digital Loop Filter

Michael H. Perrott[2], Yunteng Huang[1], Rex T. Baird[3], Bruno W. Garlepp[4], Ligang Zhang[1], Jerrell P. Hein[1]

[1]Silicon Laboratories, Austin, TX
[2]Massachusetts Institute of Technology, Cambridge, MA
[3]Montana State University, Bozeman, MT
[4]Rambus, Los Altos, CA

A CDR architecture is presented in 0.25μm CMOS that leverages a fully integrated hybrid analog/digital loop-filter structure to achieve the desired jitter performance with low area and power consumption while also allowing multi-rate operation at 155, 622, 1250, and 2500Mb/s data rates. The overall CDR performance exceeds SONET requirements. The small package size of the CDR chip and the elimination of sensitive noise-entry points at package pins due to full integration of the loop filter simplifies the board design. In this paper, key techniques for the implementation of the hybrid loop filter, including a phase-to-digital converter and digital decimator, are described.

Figure 18.2.1 illustrates a classical CDR topology and associated analog loop-filter topologies. The loop filter must be properly designed to achieve the appropriate bandwidth and adequately low peaking in the overall closed-loop PLL transfer function. In practice, analog loop-filter approaches are often difficult to integrate due to the large area required by their capacitors, are hard to configure for different time constants, and are highly sensitive to temperature and process variations as well as leakage currents that cause the VCO frequency to drift in the absence of incoming data transitions. While modern technology potentially allows direct implementation of the entire loop filter with a digital equivalent, it is more efficient to use a hybrid analog/digital approach in order to lower the required bandwidth of the required A/D and D/A structures. In particular, in the proposed design, the higher-bandwidth feed-forward path is chosen to be in the analog domain, and only the lower-bandwidth integration path is implemented in the digital domain (see filter (2) in Fig. 18.2.1). This strategy enables full integration of the loop filter by replacing the large integrating capacitor with a compact and configurable digital accumulator while also allowing a low-power implementation of the overall loop filter.

Figure 18.2.2 illustrates the proposed CDR architecture incorporating the hybrid analog/digital loop filter. For simplicity, only 2.5Gb/s operation are considered. A phase-to-digital converter is used to encode the analog phase-error signal in digital format, which is then passed on to the hybrid filter whose topology is analogous to that of filter (2) in Fig. 18.2.1. The top filter section is an analog feed-forward path that is scaled by current I_f to achieve the desired closed-loop PLL bandwidth and then lowpass filtered to smooth out the digital-error waveform. The bottom section is a digital integration path that is realized by a digital decimator, accumulator, ΔΣ DAC, scaling current I_i, and lowpass filter that smooths out the ΔΣ quantization noise. The outputs of the top and bottom paths are summed and fed into the input port of an analog varactor within the VCO shown in Fig. 18.2.3.

The VCO is an LC oscillator designed for low-noise operation that uses an analog varactor and digital switched-capacitor array to simultaneously achieve the required noise performance and adequate frequency tuning range [1]. The analog varactor provides continuous frequency adjustment across 2% tuning range. The digital switched-capacitor array provides discrete frequency adjustment from 2.35 to 2.8GHz in order to allow operation at the required SONET FEC and non-FEC rates across all process and temperature variations. The array consists of a combination of binary and unitary codes that are segmented into coarse, medium, and fine sections. The digital capacitor settings are controlled by a referenceless frequency-acquisition block that will be described in a future publication.

Standard digital phase detectors for CDRs consist of bang-bang circuits that lead to nonlinear PLL dynamics. Unfortunately, such circuits complicate efforts to achieve the required jitter-transfer mask due to their nonlinear behavior. Figure 18.2.4 illustrates the proposed phase-to-digital converter that overcomes these problems by efficiently achieving high resolution conversion so that the PLL dynamics are linear. The structure consists of a standard Hogge detector circuit that feeds its error output into a first-order CT ΔΣ ADC [2]. Fast operation of the structure is achieved by avoiding the use of opamps, and performing a required subtraction operation in the current domain. Note that the ΔΣ is operated at half the CLK frequency in order to allow its register to more easily resolve small inputs.

To avoid building a GHz-speed accumulator, the output of the phase-to-digital converter is sent to a decimator that reduces the required operating speed of the accumulator to 77MHz at the expense of losing its 4 LSbs. To accomplish this task, the decimator acts as a simplified accumulator structure whose only output is its carry-out bit. Figure 18.2.5 illustrates a topology to achieve this decimation operation – this structure leverages the accumulator implementation offered by ripple counters. To explain, the output transitions of an N-stage ripple counter occur every time the input cycles through 2^N transitions, so that its output corresponds to the carry-out bit of an accumulator whose signals are encoded as transitions rather than assertion levels. To switch between assertion and transition domains, a 1-to-transition converter is included at the decimator input and a transition-to-1 converter is placed at the decimator output. A 4b ripple counter is placed between these converters, where each ripple counter stage includes a clock divide-by-2 circuit and a re-synchronizing register.

The prototype CDR circuit exceeds all SONET performance specifications at 2.5Gb/s, 622Mb/s , and 155Mb/s data rates as well as Gb Ethernet specs at 1.25Gb/s data rate. Figure 18.2.6 shows measured transfer curve and eye diagram plots at 2.5Gb/s – the transfer curves are well within the SONET specification, and the eye diagram is wide open. Measured jitter tolerance is >0.55UI and jitter generation is typically $1.2ps_{rms}$, which is <1/3 of the SONET specification at 2.5Gb/s. The current draw is 170mA with 3.3V or 2.5V supply, which includes clock and data drivers. Finally, the package occupies $25mm^2$. Figure 18.2.7 shows a die micrograph of the chip.

References:

[1] E. Hegazi, et al., "A Filtering Technique to Lower LC Oscillator Phase Noise," *IEEE J. of Solid-State Circuits*, pp. 1921-1930, Dec., 2001.
[2] M.H. Perrott, R.T. Baird, and Y. Huang, "Digitally-Synthesized Loop Filter Circuit Particularly Useful for a Phase Locked Loop," *US Patent 6,630,868,* Oct., 7, 2003.

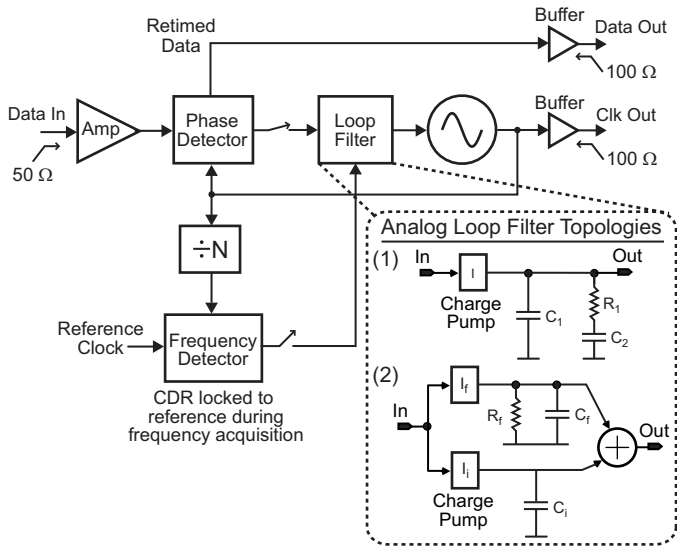


Figure 18.2.1: Block diagram of a classical CDR.

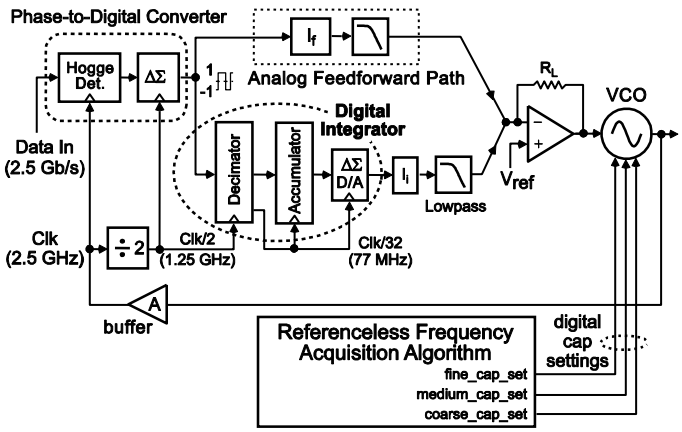


Figure 18.2.2: Proposed CDR with digital integrator.

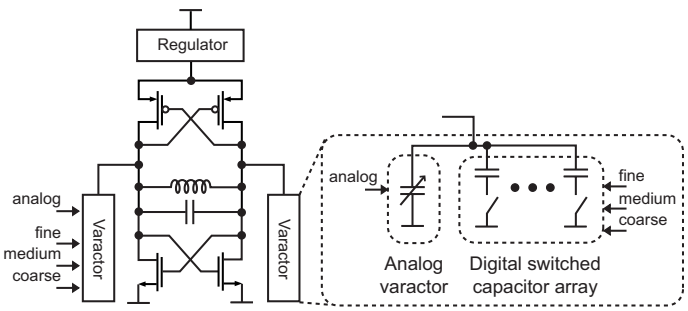


Figure 18.2.3: VCO architecture.

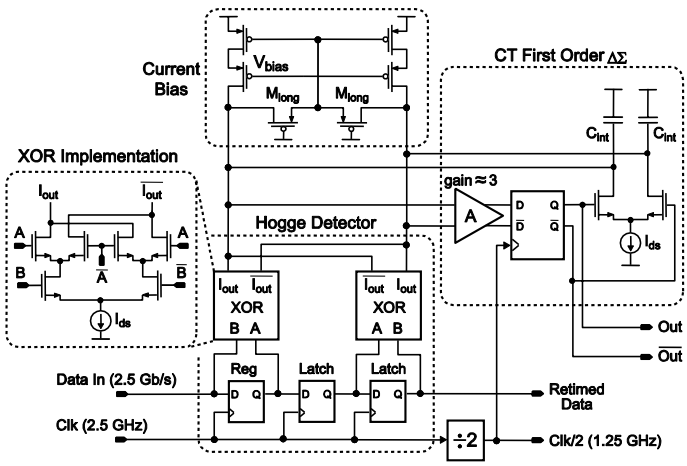


Figure 18.2.4: Proposed phase-to-digital converter.

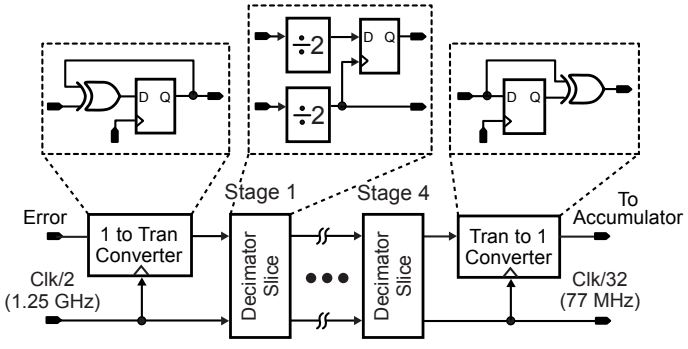


Figure 18.2.5: Proposed digital decimator implementation.

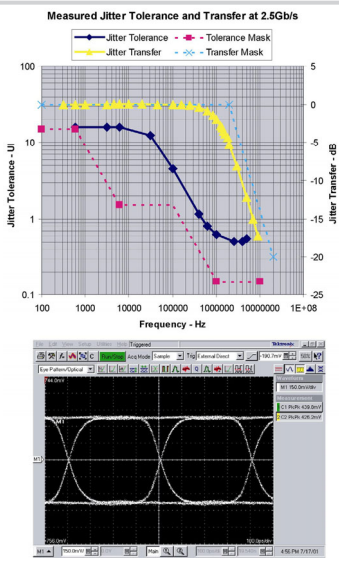


Figure 18.2.6: Measured results at 2.5Gb/s.

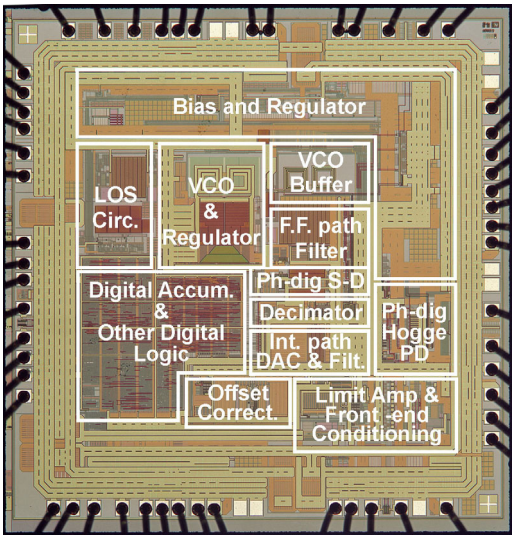


Figure 18.2.7: Die micrograph.

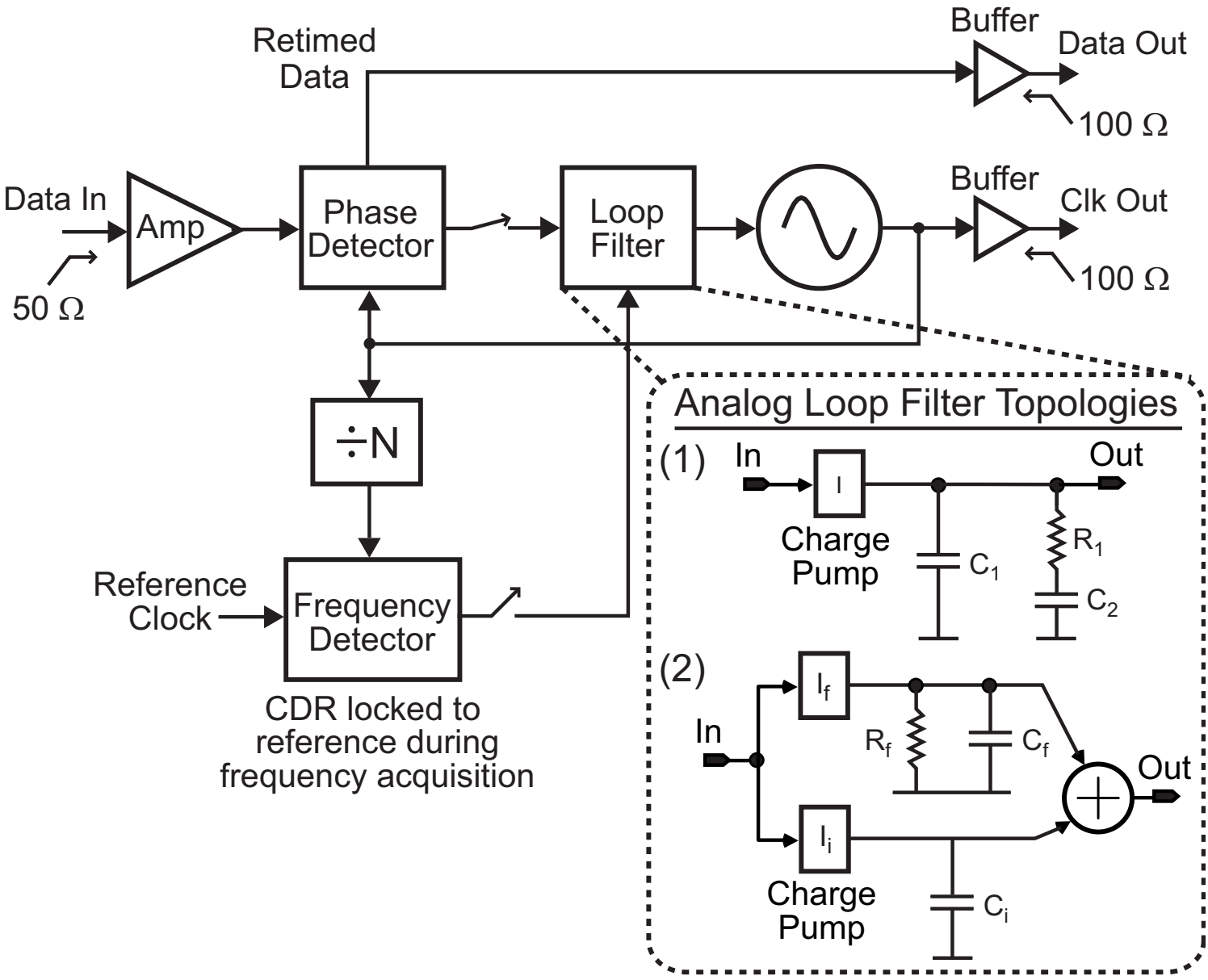


Figure 18.2.1: Block diagram of a classical CDR.

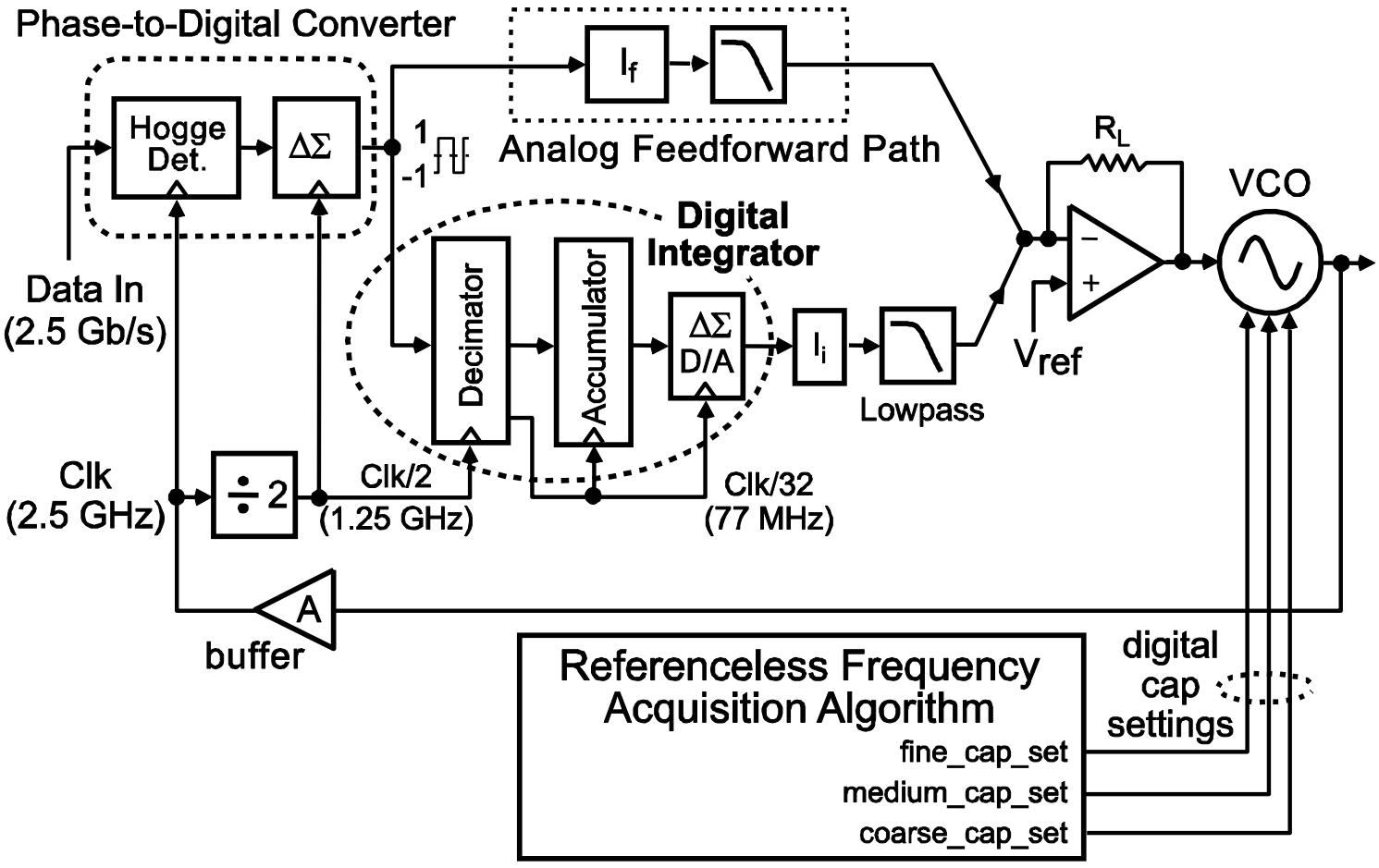


Figure 18.2.2: Proposed CDR with digital integrator.

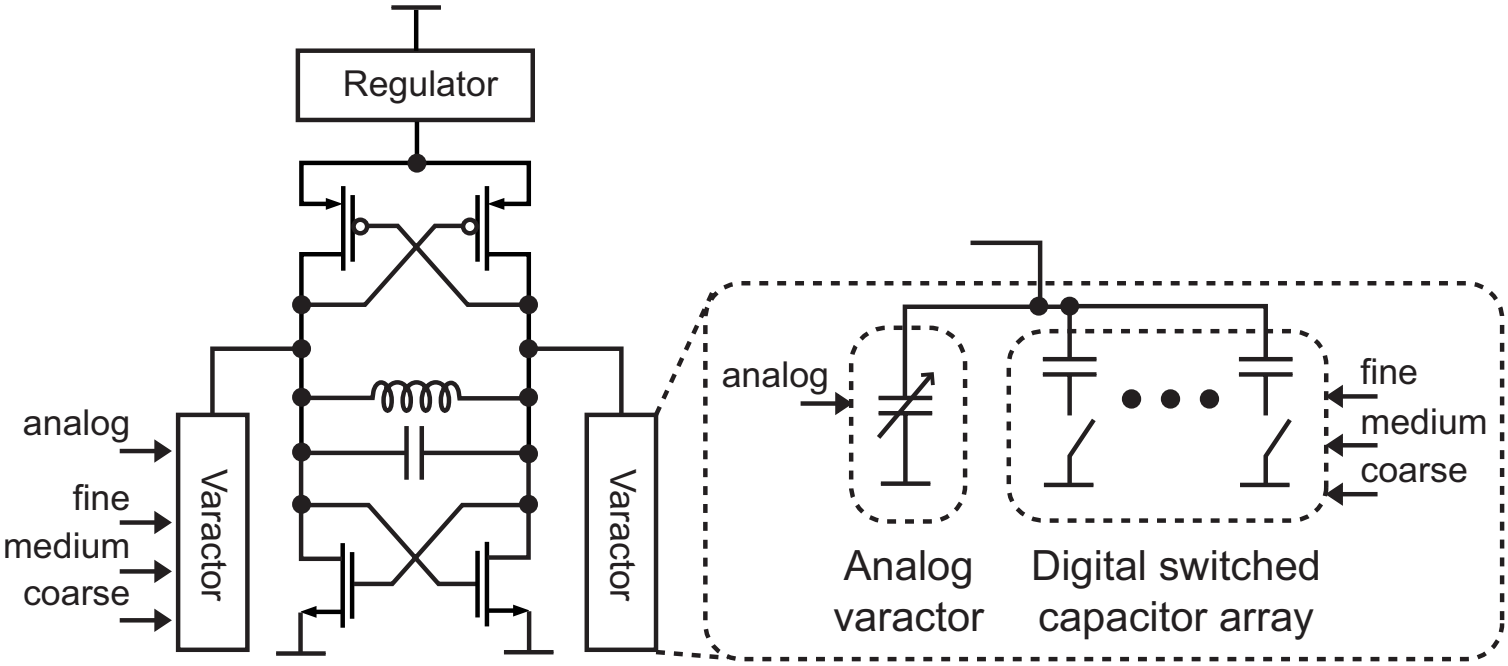


Figure 18.2.3: VCO architecture.

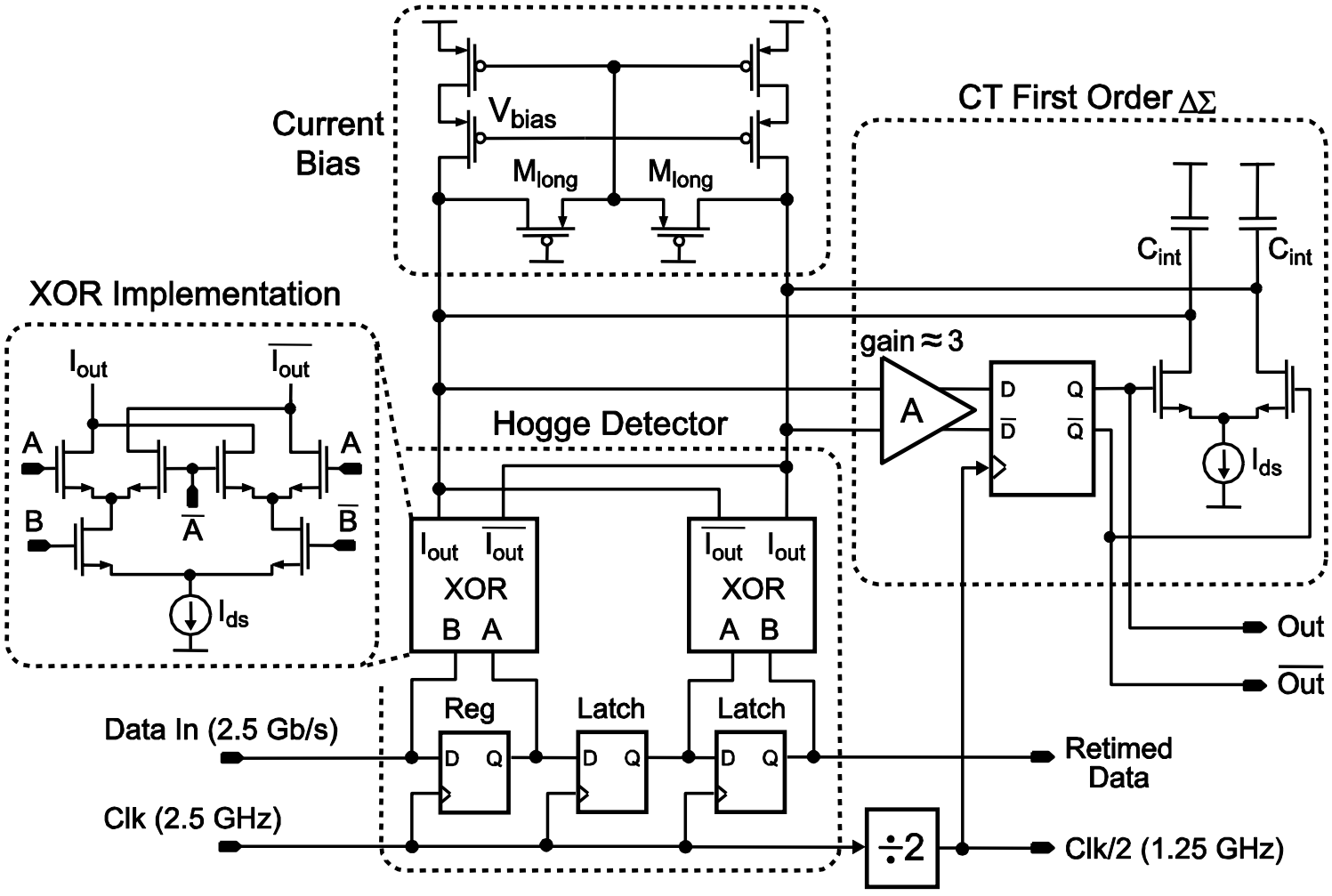


Figure 18.2.4: Proposed phase-to-digital converter.

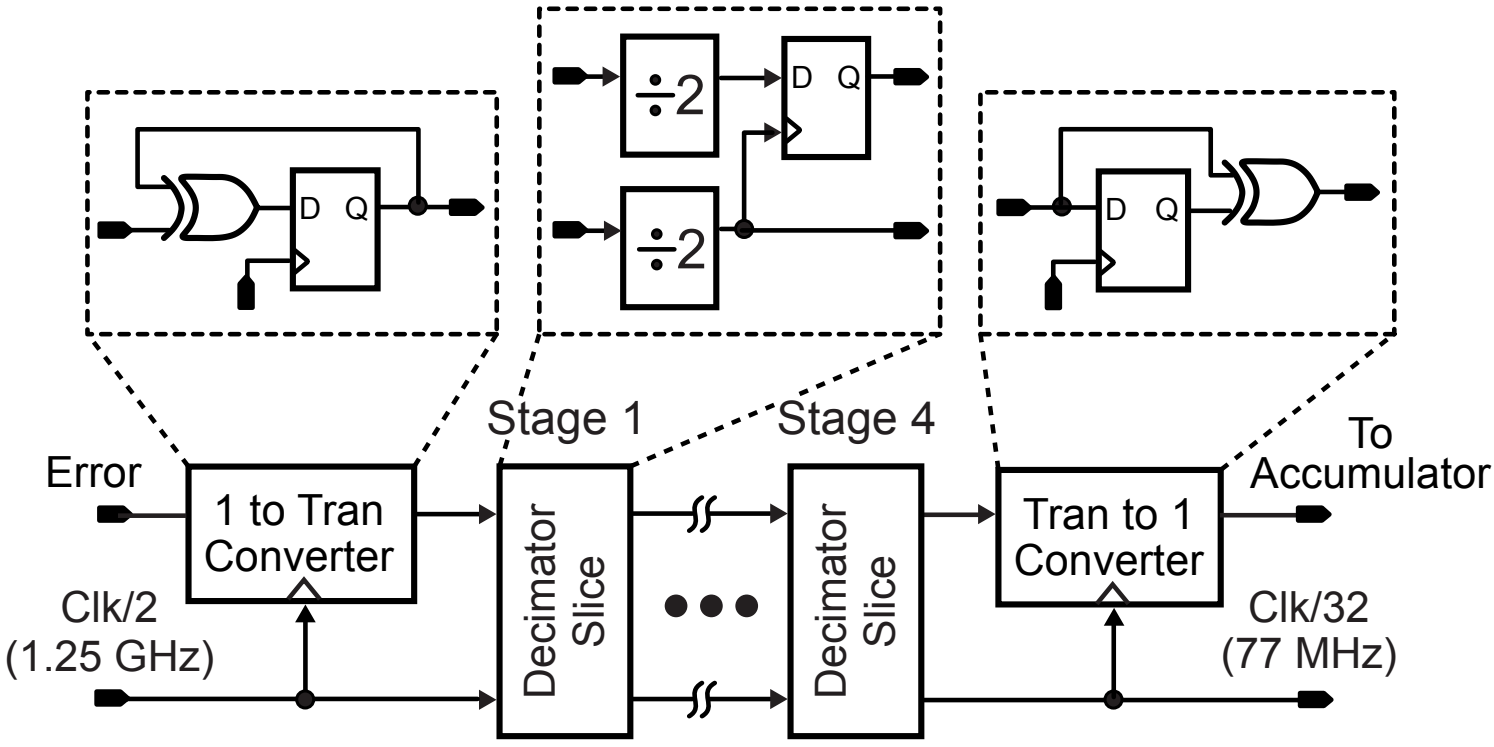
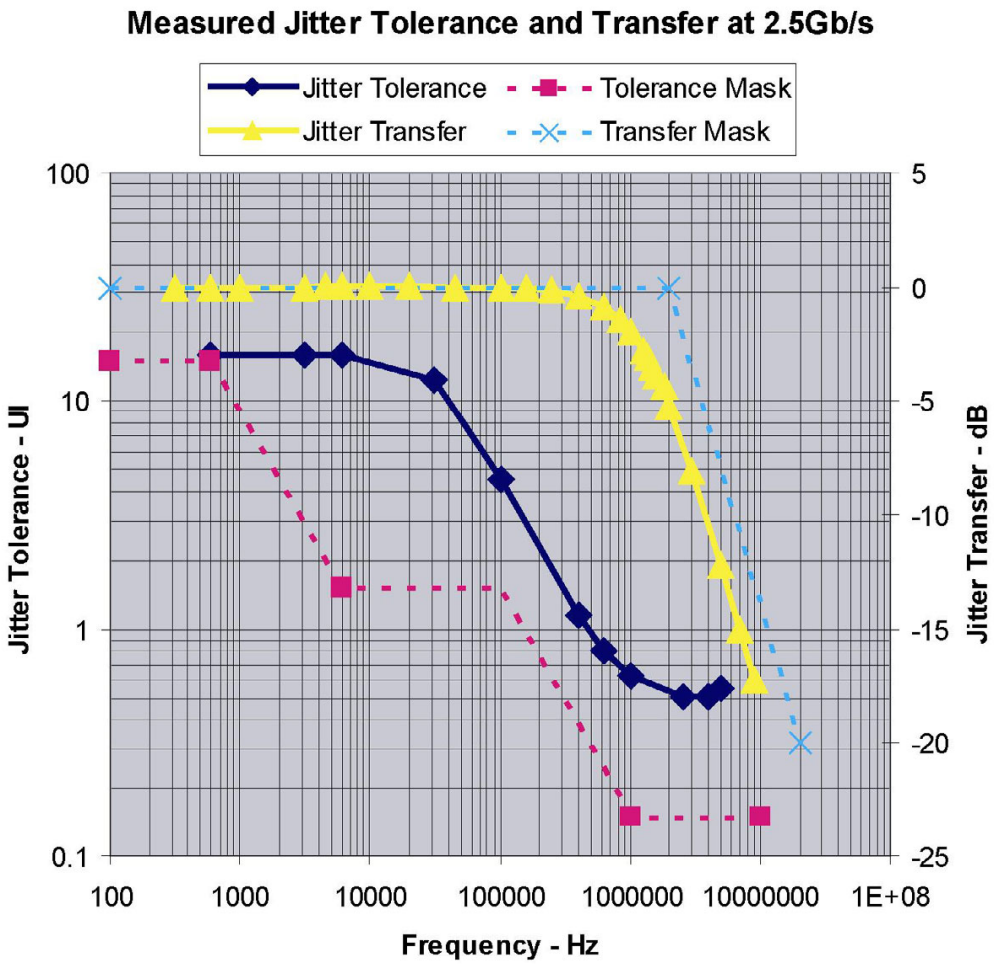


Figure 18.2.5: Proposed digital decimator implementation.



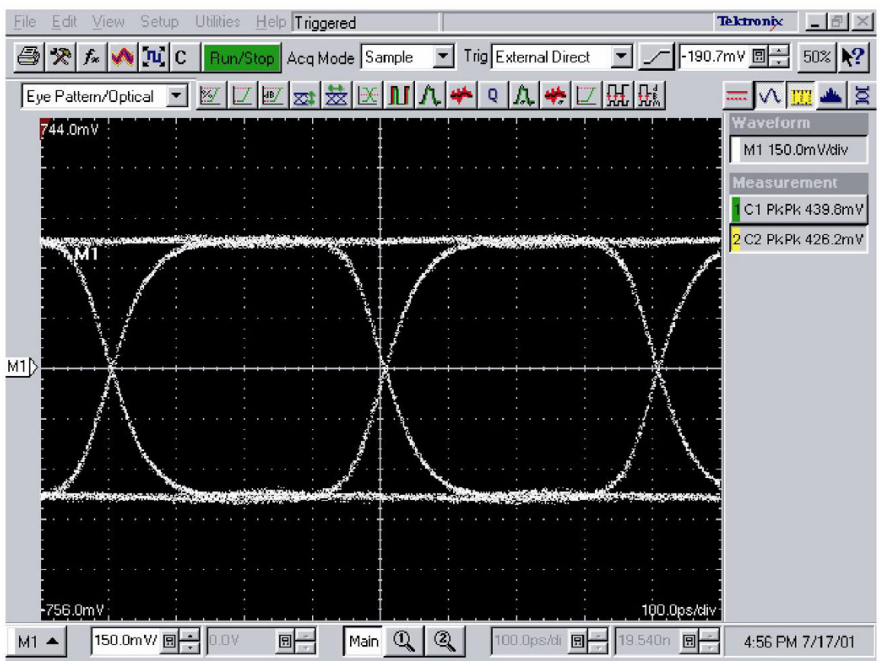


Figure 18.2.6: Measured results at 2.5Gb/s.

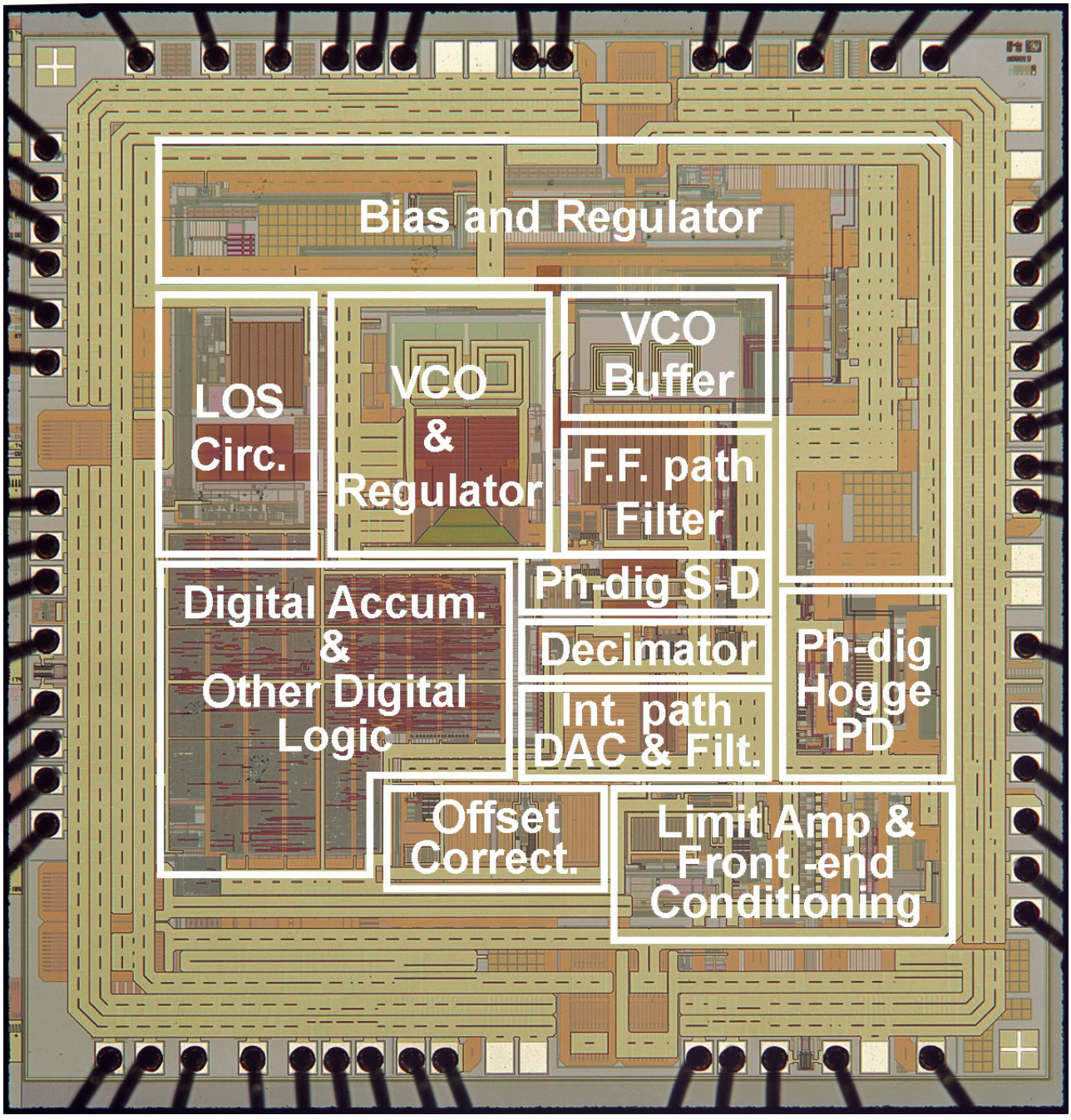


Figure 18.2.7: Die micrograph.