A VCO-based Analog-to-Digital Converter with Second-Order Sigma-Delta Noise Shaping

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Abstract—**A voltage-controlled oscillator (VCO) based analog-to-digital converter (ADC) utilizing Sigma-Delta (Σ–Δ) techniques for second order quantization noise shaping is presented. A custom IC prototype of this highly digital architecture achieves 60-dB signal-to-noise ratio (SNR) over a 1-MHz bandwidth with 800-MHz sampling rate. It was fabricated in a 0.18-μm 1-poly 5-metal CMOS technology.**

I. Introduction

There has recently been increasing interest in developing highly digital analog-to-digital converter (ADC) structures for on-chip testing and ease of integration in future CMOS processes. An intriguing circuit to utilize in such cases is a ring oscillator voltage-controlled oscillator (VCO), which outputs a clock waveform whose frequency is a function of an input tuning voltage. By comparing the clock frequency to that of a separate clock reference using digital counters, one can create an all-digital ADC that can be readily utilized for on-chip monitoring of supply voltage variations and other on-chip waveforms [1]. Such VCO circuits have also been employed to realize multi-bit quantizers with first order noise shaping, which allow simplified implementation of high order Sigma-Delta (Σ–Δ) ADCs [2] [3]. A shortcoming of approach [1] is that the effective conversion rate must be quite low to achieve high resolution. Utilizing a multi-phase ring VCO contributes to improvement of the resolution, but the conversion rate is still limited [4] [5]. The shortcoming of approaches [2] and [3] is that the overall A/D implementation ends up being primarily analog in nature.

In this paper, we propose a VCO-based ADC structure which allows second-order Σ–Δ noise shaping to be achieved with a highly digital structure. Rather than the purely digital solution of [1], [4], and [5] or the highly analog solution of [2] and [3], we suggest the use of a primarily digital structure that is augmented by a small amount of low performance analog circuitry to achieve the higher order noise shaping. The topology presented here leverages a previously suggested structure for Σ–Δ frequency discrimination described in [6]. Our contribution is in showing the utility of this structure for A/D conversion, applying fractional-N phase-locked loop (PLL) modeling approaches [7] to

quantify its behavior, and demonstrating a practical implementation by showing measured results from a custom IC prototype of the structure.

We begin by discussing the integrating characteristics of VCO structures and their application to Σ–Δ A/D conversion. We then show the application of the structure in [6] to achieve a second-order Σ–Δ ADC. An analytical model of this converter based on a fractional-N frequency synthesizer model is then presented. Unique issues to the proposed structure are then discussed. Finally, we show measured results of a custom IC prototype implementing the A/D structure.

II. Background

Fig. 1 illustrates the classical VCO model used for PLL modeling, which identifies its behavior as an ideal integrator with an input signal in voltage and an output signal in phase. Note that a phase detector can be used to convert the output phase to voltage or current in order to use the VCO as a voltage-to-voltage or voltage-to-current integrator.

Fig. 2 illustrates how a first-order continuous-time (CT) Σ–Δ modulator can be implemented with a VCO. Here we assume that the VCO frequency is essentially locked to the reference clock frequency such that all phase deviations of the VCO are confined to one reference cycle interval. The phase detector is unnecessary in this case because the one-bit quantizer operates as a one-bit time-to-digital converter – the quantizer output goes to low if the VCO output signal lags
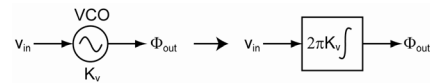

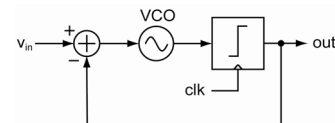
Fig. 1. VCO as a voltage-to-phase integrator.

Fig. 2. A first-order CT Σ–Δ ADC employing a VCO.

behind the sampling clock, and it goes to high if the VCO output signal leads the sampling clock. Thus, the output phase signal of the VCO, which is the integral of the VCO input voltage, is quantized and then fed back to the input of the VCO. Note that a practical VCO requires a band-limited input control voltage to perform accurate voltage-to-phase integration; hence, the architecture in Fig. 2 is useful to show for pedagogical purposes but not as a practical A/D structure.

Fig. 3. Proposed second-order CT $\Sigma-\Delta$ ADC employing a VCO.

III. PROPOSED A/D STRUCTURE

Fig. 3 shows the proposed second-order $\Sigma-\Delta$ ADC architecture using a VCO as a first-stage integrator. By using a dual-modulus divider, the quantizer output need not be fed back to the input of the VCO. Therefore, the VCO input is influenced only by a band-limited input signal, and accurate voltage-to-phase integration is achieved.

The structure shown in Fig. 3 has been previously suggested for use as a $\Sigma-\Delta$ frequency discriminator [6], which converts the instantaneous frequency of the VCO to a digital sequence. Here we focus on converting the input tuning voltage of the VCO to a digital sequence, so that we are performing voltage-to-digital conversion rather than frequency-to-digital conversion. The benefit of this structure for A/D conversion is that it performs second-order noise shaping with a highly digital implementation – the only analog elements are essentially the charge pump/capacitor combination shown in Fig. 3.

IV. MODELING

To understand the operation of the proposed ADC structure in Fig. 3, consider the analytical model shown in Fig. 4, which is a direct analogy of the fractional-N PLL model described in [7]. Here the VCO is modeled as an ideal integrator; the multi-modulus divider is modeled as a
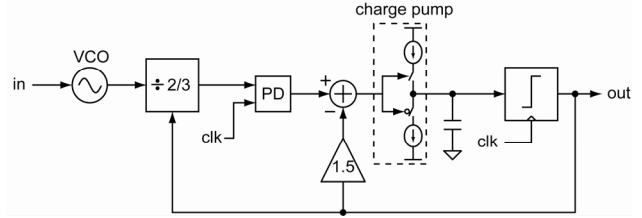
sampler, accumulator, and scaling factor of $1/N_{nom}$; and the phase detector is modeled as a substractor, scaling factor of $\alpha T/(2\pi)$, and an impulse train modulator [7]. Note that T is a sampling clock period and $1/T$ is the sampling frequency which is 800 MHz for the prototype IC presented here. Fig. 4 clearly shows how the quantizer output signal, which is not band-limited, is effectively fed back to ADC input without impacting the actual VCO input. The signal paths from the VCO input and the quantizer output are physically separated, but the output phase of the divider is the difference between the integration of those two signals as shown in Fig. 4. Hence, the divider creates an all-digital negative feedback loop which allows the ADC architecture to operate as a second-order $\Sigma-\Delta$ modulator without the need for fast analog signals at the VCO input. The frequency-domain model is illustrated in Fig. 5.

Given the model in Fig. 4 and Fig. 5, design of the ADC follows that of classical second-order $\Sigma-\Delta$ ADC structures. In particular, the coefficients of the feedback loops in Fig. 4 should be appropriately set to realize second-order noise shaping in a stable manner. Fig. 6 illustrates a simple model for a classical second-order $\Sigma-\Delta$ structure as a point of comparison.
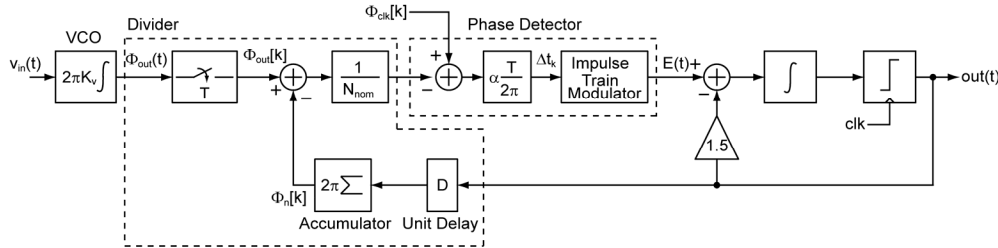

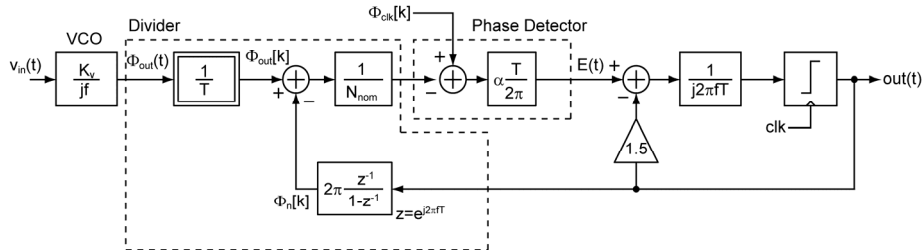Fig. 4. Time-domain model of the proposed second-order CT $\Sigma-\Delta$ ADC.

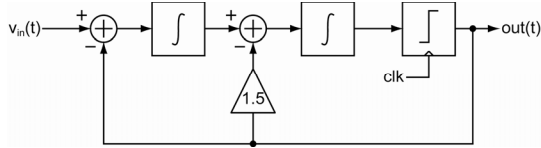Fig. 5. Frequency-domain model of the proposed second-order CT $\Sigma-\Delta$ ADC.

Fig. 6. Model for an ideal second-order CT Σ–Δ ADC.

Fig. 7. Simplified circuit block diagram of the prototype ADC.

V. UNIQUE CONSTRAINTS

The proposed ADC structure introduces an extra constraint over that of a classical Σ–Δ ADC structure, in that the VCO center frequency must be appropriately set. This constraint is imposed by the fact that the phase detector within the proposed structure must operate within its phase locking range (i.e., cycle slipping must be avoided) in order to achieve the desired Σ–Δ noise shaping behavior. As an example, if an XOR phase detector is used, then the theoretical phase locking range of the XOR phase detector is π. In practice, the finite rising and falling times of the output voltage of the XOR further narrow the locking range.

In order to prevent cycle slipping of the phase detector, the average frequency of the divider output should be the same as the clock frequency. Therefore, the center frequency of the VCO should be set to be N_{nom} times the clock frequency, where N_{nom} corresponds to the nominal divide value. As an example, in the prototype presented here, N_{nom} equals 2.5 and the reference clock frequency equals 800 MHz, so the center VCO frequency should be set to 2 GHz.

The phase detector locking range also sets the achievable dynamic range of the proposed ADC. Since the output frequency of the VCO varies by the signal level of its input tuning voltage, a large input signal level causes a rapid phase change that can, in turn, cause the phase difference seen by the phase detector to go outside its locking range. The Σ–Δ loop operation fails if the phase detector incurs cycle slips – this condition corresponds to a classical Σ–Δ ADC becoming unstable due to the saturation of an internal integrator. The behavioral simulation of the proposed architecture shows that the cycle slips occur before saturation of the internal integrator occurs. Therefore, the locking range of the phase detector in this architecture determines the upper limit of the input signal amplitude.

VI. PROTOTYPE

Fig. 7 shows the simplified circuit block diagram of the prototype VCO-based ADC. All digital circuits are implemented with source-coupled logic (SCL) for high speed operation and common-mode noise rejection. The SCL implementation has the benefit of decreasing the rising and falling times of the XOR phase detector, which improves its locking range. The input VCO is implemented with a 3-stage ring VCO which is also implemented differentially to suppress common-mode noise. Additional coarse and fine tuning inputs are included to adjust the center frequency of the VCO. The second-stage integrator is realized with charge pumps and poly capacitors. The current of each charge pump
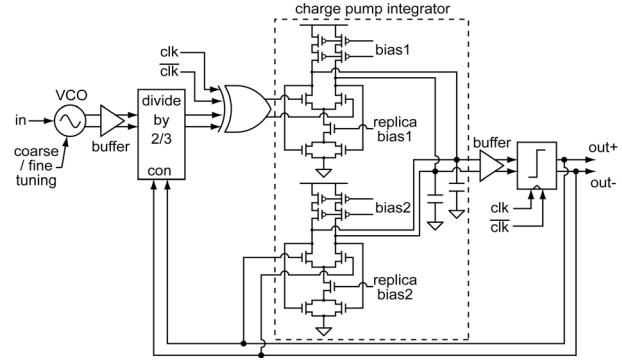
can be controlled externally, so that the gain of the second-stage integrator and the feedback coefficient can be tuned.

Note that the only analog building blocks in Fig. 7 are the buffer for the quantizer, the charge pumps, and the capacitor. The buffer is used as a preamplifier for the quantizer to reduce the occurrence of metastable behavior. The charge pump/capacitor structures function as integrators. These charge pump integrators will have relatively poor DC gain due to leakage currents and low output resistance of the CMOS transistors, especially in future CMOS processes. However, the resolution of the VCO-based ADC presented here does not degrade much by having such poor DC gain in charge pump integrators due to the infinite DC gain of the first-stage integrator implemented with a VCO.

VII. MEASURED RESULTS

The prototype chip was fabricated in a 0.18 μm 1-poly 5-metal digital CMOS process. Fig. 8 shows the die photograph. The total active area is about 0.5 mm^2 including the ring VCO. The total power consumption is 34 mW excluding the VCO and its buffer stage. The VCO and the buffer consume 32 mW and 84 mW, respectively.

The measured output spectrum using a Hann window with –18 dBFS input signal is shown in Fig. 9. The spectrum clearly shows quantization noise shaping. The second harmonic components are about 22 dB lower than the desired input signal due to the nonlinear voltage-frequency relation of the ring VCO and nonlinear operation of the dual-modulus divider. The linearity could be improved in the future
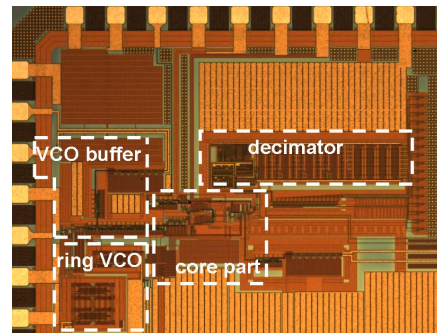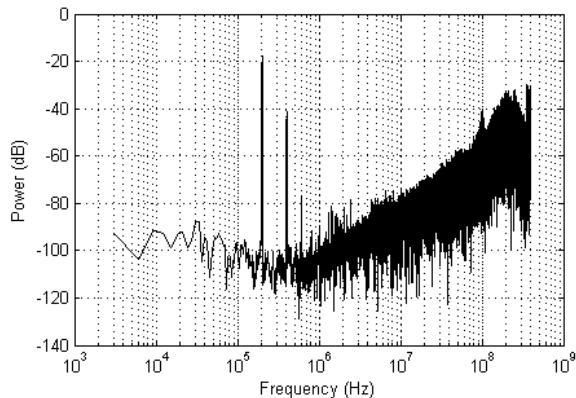

Fig. 8. Die photograph of prototype IC.

Fig. 9. Measured output spectrum with -18 dBFS input.

Sampling frequency		800 MHz
Signal bandwidth		1 MHz
Peak SNR		60 dB (@ V_{in} = 201 kHz)
Peak SNDR		39 dB (@ V_{in} = 201 kHz)
ENOB		9 bit
Power	Core part	34 mW
	VCO	32 mW
	VCO buffer	84 mW
Power supply		1.8 V
Process		0.18 μm 1P5M digital CMOS
Active area		0.5 mm^2

through appropriate design of the VCO tuning characteristic.

In Fig. 10, the measured signal-to-noise ratio (SNR) and signal-to-noise-and-distortion ratio (SNDR) are plotted as a function of the input signal level. The measured SNR drops quickly as the input signal level increases beyond −18 dBFS. The reason for such a drop in the SNR curve is that above a −18 dBFS input signal level, the phase detector begins to cycle slip as described in section V. Similar behavior occurs with classical second order Σ−Δ ADC structures since large inputs eventually cause instability. Note that the phase noise of the ring VCO also limits the SNR because it is not noise-shaped.

The maximum SNR measured is 60 dB over 1 MHz bandwidth. The measured SNDR is much lower than the SNR due to large harmonic components in band. Table 1 summarizes the measured performance of the prototype chip.

VIII. CONCLUSION

A VCO-based ADC that achieves second-order Σ−Δ quantization noise shaping has been presented in this paper. The highly digital architecture makes it possible to realize ADCs with only a small numb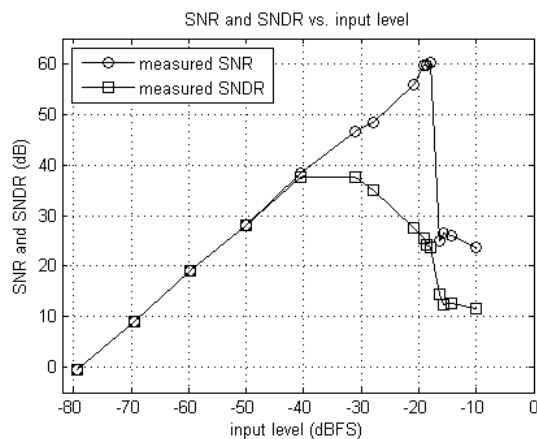er of analog circuits, and could potentially be useful for on-chip signal monitoring for future ASIC chips. The proposed ADC is implemented in a 0.18 μm digital CMOS process and achieves 60 dB SNR over 1 MHz bandwidth with 800 MHz of sampling rate.

ACKNOWLEDGMENTS

Figure 10. Measured SNR and SNDR of the prototype IC.

REFERENCES

[1] E. Alon, Vladimir Stojanović, and M. A. Horowitz, "Circuits and techniques for high-resolution measurement of on-chip power supply noise," IEEE Journal of Solid-State Circuits, vol. 40, no. 4, pp. 820–828, April 2005.

[2] A. Iwata, N. Sakimura, M. Nagata, and T. Morie, "An architecture of delta sigma A-to-D converters using a voltage controlled oscillator as a multi-bit quantizer," IEEE Transactions on Circuits and Systems II, vol. 46, issue 7, pp. 941–945, July 1999.

[3] M. Z. Straayer and M. H. Perrott, "A 10-bit 20MHz 38mW 950MHz CT ΣΔ ADC with a 5-bit noise-shaping VCO-based Quantizer and DEM circuit in 0.13u CMOS," IEEE Symposium on VLSI Circuits, pp. 246–247, June 2007.

[4] Jaewook Kim and Seonghwan Cho, "A time-based analog-to-digital converter using a multi-phase voltage controlled oscillator," IEEE International Symposium on Circuits and Systems, pp. 3934–3937, May 2006.

[5] A. Tritschler, "A Continuous Time Analog-to-Digital Converter With 90μW and 1.8μV/LSB Based on Differential Ring Oscillator Structures," IEEE International Symposium on Circuits and Systems, pp. 1229–1232, May 2007.

[6] W. T. Bax, M. A. Copelan, and T. A. D. Riley, "A single-loop second-order ΔΣ frequency discriminator," IEEE International Symposium on Biomedical Imaging, pp. 301–304, July 2002.

[7] M. H. Perrott, M. D. Trott, and C. G. Sodini, "A modeling approach for Σ-Δ fractional-N frequency synthesizers allowing straightforward noise analysis," IEEE Journal of Solid-State Circuits, vol. 37, no. 8, pp. 1028–1038, August 2002.