A Single-Slope 80MS/s ADC using Two-Step Time-to-Digital Conversion

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Abstract—An 80MS/s analog-to-digital converter (ADC) based on single-slope conversion is presented which utilizes a recently developed gated ring oscillator (GRO) time-to-digital converter (TDC) to achieve an ENOB of 6.45 bits. To save power, the time-to-digital conversion is done in two steps, the first of which is based on coarse time quantization as measured by cycles of an oscillator and the second of which is based on fine time quantization by the GRO TDC. The resulting $0.13\mu m$ CMOS prototype circuit is simple and compact in its implementation and consumes 6.4mW of power.

I. INTRODUCTION

Single-slope conversion or integrating conversion is a classical means of implementing an analog-to-digital converter (ADC) [1], and has the advantage of having a very simple implementation with minimal analog content. The key operating principle of such structures is to translate an input voltage to a ramp in time, and then measure the time duration it takes for the ramp to pass a given threshold voltage. Typically, the time measurement is performed with a digital counter, whose time resolution corresponds to the counter clock period. Since the clock frequencies of even the most modern CMOS processes are typically limited to less than 10 GHz, the time resolution offered by digital counter structures is constrained to be no better than hundreds of picoseconds. As a result, single-slope conversion is often constrained to very low sample rates even when only moderate resolution is desired of the ADC.

Recently, researchers have been investigating alternative approaches to using time-based quantization within an ADC in order to achieve a highly digital ADC implementation. One example of this trend is to tune the frequency of a voltage-controlled oscillator (VCO) according to the input analog voltage, and then measure the period of the oscillator to determine the quantized output value [2]. This approach unfortunately yields limited conversion rates due to the limited frequency of the VCO, and also presents nonlinearity in the ADC due to the nonlinear frequency tuning characteristic of a practical VCO. The conversion rates can be increased by looking at all phases of a multi-phase VCO rather than just its overall output [3], but the nonlinear characteristic still prevails. By surrounding the VCO-based quantizer with an analog feedback loop, the resulting ADC characteristic can be made much more linear [4], [5], but the cost of such an approach is higher analog complexity in the system.

In this paper, we revisit the idea of using a single-slope conversion structure to leverage time-based quantization in the ADC. Rather than using a digital counter as the quantizer element, we instead draw off of recent advances in time-to-digital conversion (TDC) to perform this operation. In particular, we leverage a recently published TDC based on a multipath gated ring oscillator (GRO) structure that achieves better than 10ps of time resolution with a wide dynamic range. To improve the power efficiency, we propose two-step conversion in which a ring oscillator period is used to provide the initial coarse quantization, and the GRO TDC is used to provide fine quantization of the resulting residue. Measured results of the proposed architecture in $0.13\mu m$ CMOS demonstrate 80Ms/s conversion rate with an ENOB of 6.45 bits with a simple, compact ADC structure that has minimal analog complexity.

We begin by showing the basic concept of the proposed ADC, which is composed of a linear voltage-to-time conversion (VTC) and a two-step TDC. We then show the circuit implementation of the linear VTC, followed by details of the two-step TDC. Follwing this discussion, we present a post-processing technique to mitigate the impact of mismatch in the two-step conversion process. Finally, measured results are shown for a custom IC prototype implementing the ADC.

II. THE PROPOSED ADC

Fig. 1 shows the basic concept of the proposed ADC architecture which utilizes a linear VTC and a two-step TDC. The VTC transforms a sampled input voltage to a pulse whose duration is linearly proportional to the input voltage. The duration of the pulse signal is measured by the two-step TDC, which yields a corresponding digital output. By using a two-step architecture for the TDC, the power consumption is reduced while still achieving large range and fine resolution. The key idea is to first perform the time measurement with a coarse TDC that has low power consumption, and then use a fine TDC to measure the resulting residue. We will show that the two step TDC implementation can be achieved with minimal analog complexity.

The key challenges of the ADC are to achieve a linear VTC structure along with an efficient two-step TDC circuit architecture. We discuss each of these issues in this section.

A. Linear Voltage-to-Time Conversion (VTC)

Fig. 2 shows the block diagrams and timing diagrams of the suggested linear VTC. It is composed of a sample-and-hold
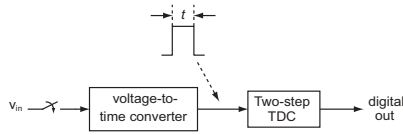
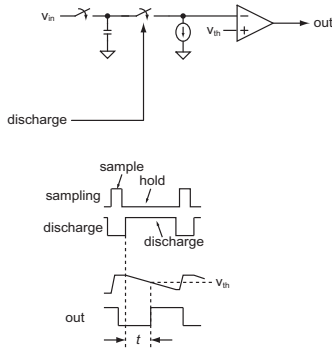Fig. 1.   A/D conversion using a linear VTC and a two-step TDC.

Fig. 2.   Block diagrams and timing diagrams of a linear VTC.

Fig. 3.   Simplified circuit diagrams of a linear VTC.

circuit, a current source, and a comparator. The sample-and-hold circuit charges the sampling capacitor up to the input voltage while the current source is turned off. The current source is then turned on so that the voltage across the sampling capacitor decreases linearly as a function of time. When the voltage of the sampling capacitor crosses the threshold voltage of the comparator, the output of the comparator goes high. Assuming constant current drain on the capacitor, the resulting time duration between turning the current source on and having the comparator go high is linearly related to the input voltage, so that the desired VTC function is achieved.

By quantizing the time duration of the pulse output by the VTC with the two-step TDC, a digital representation of the input voltage is achieved. Therefore, the combination of the VTC and the TDC yields the desired ADC functionality.

A key issue in achieving good linearity in the proposed ADC is to maintain constant current drain on the capacitor within the VTC, which requires high output resistance of the current source. Fig. 3 shows a simplified circuit diagram of the voltage-to-time converter which achieves a high output resistance current source through double cascoding. The drawback of having two cascode devices is limited voltage swing at the output of the current source. However, high output resistance is only needed for voltages above the threshold voltage of the comparator since voltages below that value have no influence on the timing of the comparator decision. Therefore, the threshold voltage of the comparator is simply chosen to be large enough such that the cascode devices are in saturation above its value.

Fig. 3 also depicts the comparator implementation, which consists of a simple cascade of inverters. Although an inverter cannot be used as a general purpose comparator, it is suitable as a threshold-voltage-crossing detector if the input voltage is a constant slope ramp [6]. Several stages of inverters achieve high enough sensitivity as a threshold-voltage-crossing detec-
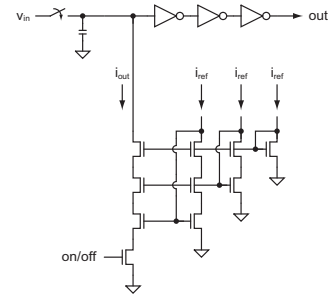
tor, and inverters are easily implemented in advanced CMOS technology. The precise threshold voltage of the inverters cannot be controlled, but the threshold voltage affects only the offset of the voltage-to-time converter, which is easily calibrated out by post-processing in the digital domain.

B. Two-step Time-to-Digital Conversion (TDC)

The fine resolution portion of the two-step TDC corresponds to a multipath gated ring oscillator (GRO) TDC which was first introduced in [7]. The GRO TDC performs time-to-digital conversion by counting transitions of a ring oscillator which is enabled only during the measurement interval. The raw resolution of this TDC corresponds to an inverter delay, but the structure interestingly achieves first order noise shaping of its quantization noise [7]. A further improvement in resolution is achieved by connecting the input for each delay stage to a *combination* of previous delay stages, which is referred to as a multipath GRO TDC as proposed in [8]. By doing so, the delay per stage can be dramatically reduced below that of an inverter. In $0.13\mu m$ CMOS, a multipath GRO TDC yields about 6ps of raw time resolution [8], which is far less than the 35ps inverter delay offered by this technology [7].

A critical issue related to the GRO TDC is that its power consumption increases as the duration of the input pulse signal increases due to the longer time duration that the ring oscillator and transition counting circuits must be active. In order to save power consumption, the proposed ADC utilizes the GRO TDC only to measure the residue of a quantization operation performed by a lower power, coarse TDC. The challenge in achieving this two step conversion is that the time residue cannot be stored, so that the coarse/fine quantization must operate on the same pulse produced by the VTC.

To explain the two-step TDC structure, Fig. 4 displays simplified block diagrams of the overall ADC, and Fig. 5 shows its corresponding timing diagrams. The coarse TDC is composed of an oscillator and a counter. The oscillator's frequency is set to be relatively low so that low-power operation is obtained. The oscillator is enabled to start oscillating at the same moment that the current source is turned on to start discharging the sampling capacitor. A simple digital counter keeps track of the number of cycles that occur for the oscillator while the comparator is still low. At the point at which the comparator output goes high, a register stores the counter output so that
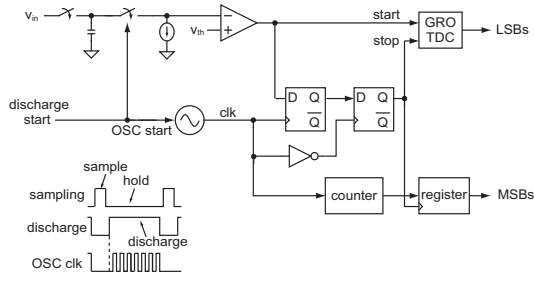
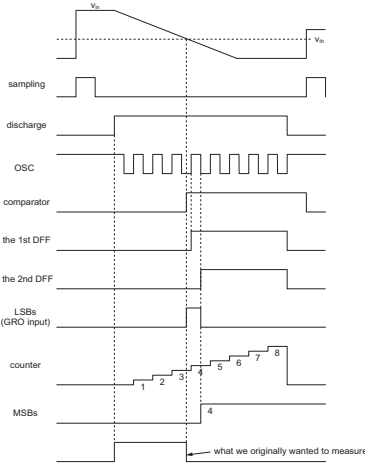Fig. 4.   Simplified block diagrams of the proposed ADC.

Fig. 5.   Timing diagrams of the proposed ADC.

coarse quantization of the pulse duration is achieved. The fine quantization measurement is then performed by measuring the time duration from when the comparator went high to the next edge of the oscillator output, as depicted in Fig. 5. By knowing the oscillator period, the resulting measurement by the GRO TDC can be easily utilized to compute the residual error of the coarse quantization performed by the oscillator. Since the GRO TDC is active for only the short time period, its power consumption is minimized.

One key issue of the GRO TDC is that it requires a minimum input pulse duration to perform correctly since its internal ring oscillator requires a finite amount of time to turn on and off. As shown in Fig. 5, two D flip-flops are utilized to add a half oscillator period to the GRO pulse duration. As such, the minimum pulse duration will be half the coarse oscillator period and the maximum pulse duration will be one-and-a-half coarse oscillator periods.

Because of the addition of the half oscillator period, the final digital word from the GRO TDC includes a corresponding offset value. This offset must be considered during post-processing, as discussed in the next section.

C. Calibration and Post-processing

The key issues in performing post-processing are to calibrate the relative scale factors between the coarse and fine TDC measurements, and to compensate for any systematic second order effects. The key second order effect that we will address
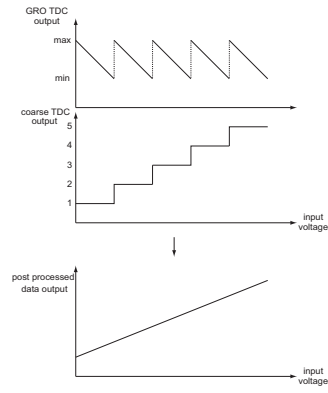

Fig. 6.   Input voltage vs. digital output code of the proposed ADC.

is that the frequency of the ring oscillator used for coarse measurement takes some time to settle to its final frequency after being turned on. The resulting transient in frequency manifests itself as nonlinearity in the coarse measurement. However, since the transient is entirely repeatable, it can be compensated by post-processing as will soon be discussed.

We first address the issue of calibrating the scale factors between coarse and fine TDC measurements. Fig. 6 depicts an example of the GRO and course TDC outputs as a function of input voltage, as well as the desired post-processed data output. As seen in the figure, the minimum and maximum values from the GRO TDC correspond to the half period and one-and-a-half period of the coarse TDC, respectively, as measured in increments of the GRO TDC unit step size. Therefore, to calibrate the relative scale factors between the coarse and fine TDC measurements, we simply need to measure the half period and one-and-a-half period of the coarse TDC oscillator with the GRO TDC. Once the minimum and maximum values of the GRO TDC are obtained, the desired digital output is

$$out = out_{TDC_C} \cdot (max_{GRO} - min_{GRO})$$
$$+ (max_{GRO} - out_{GRO}) \qquad (1)$$

where out_{TDC_C} is the output from a coarse TDC, out_{GRO} is the output from a GRO TDC, max_{GRO} is the maximum value from a GRO TDC, and min_{GRO} is the minimum value from a GRO TDC.

To deal with the issue of the transient in the coarse oscillator frequency, more elaborate calibration is required which involves generating a known waveform at the input of the ADC that spans its full dynamic range, and performing a curve fitting operation to remove the observed nonlinearity. However, one should note that only the coarse TDC need to be calibrated, which greatly simplifies the complexity of this operation. A more careful design of the coarse oscillator should eliminate the need for this calibration in future designs. One could also eliminate this issue by keeping the coarse oscillator on at all times, and then synchronizing the start time of the current source that drains the sample capacitor to the appropriate edges of the coarse oscillator. However, such an approach would increase power consumption.
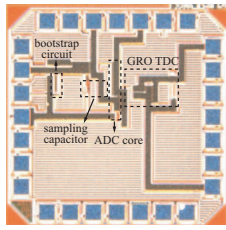
Fig. 7. Die photograph of the prototype IC.

Fig. 8. Output spectrum without calibration of coarse TDC nonlinearity.

Fig. 9. Output spectrum with calibration of coarse TDC nonlinearity.

D. Nonlinearity of GRO TDC

The quantization noise of the GRO TDC is determined by its time resolution, which is set by the delay per stage of its internal ring oscillator, as well as mismatch between the delay per stage across the various stages. While the GRO TDC does offer noise shaping, this property is not of benefit in the Nyquist rate application considered here. However, due to the natural barrel-shifting action through the delay stages in the GRO TDC, the presence of mismatch does not impact the nonlinearity of the ADC due to the noise shaping property of the barrel-shifting action [5], [8]. Therefore, while the GRO TDC does not provide noise shaping advantages in this application, it does provide linearity advantages in the presence of mismatch.

III. MEASURED RESULTS

The prototype custom IC is implemented in $0.13\mu m$ CMOS. A bootstrap circuit is employed for the sample-and-hold switches, and a 20pF sampling capacitor value is chosen. Digital circuits for calibration are included on the IC, though Matlab is used to construct the final digital output sequence of the ADC.

During the calbration phase, a simple digital control circuit is used to measure the minimum and maximum values of the GRO TDC, and these values are retrieved by MATLAB through a USB interface for post-processing of the ADC output as explained in the previous section. nonlinearity of the coarse TDC is measured by applying a full swing sinusoidal wave in the input of the ADC. By using a curve fitting method, the adjusted gains for the coarse TDC are calculated and stored for use by the MATLAB post-processing script.

Fig. 7 shows the die photograph. The total active area is about $0.09mm^2$ including a sampling capacitor.

Fig. 8 shows the 4096 point FFT spectrum with 38MHz input signal at 80MS/s sampling rate without calibration of the coarse TDC non-linearty, and Fig. 9 shows the spectrum with calibration. The maximum ENOB measured is 6.45 bit at 80MS/s sample rate with calibration. The total power consumption is 6.4mW, of which the GRO TDC consumes about 4mW. The calculated figure of merit (FOM) is 0.92 pJ/level.

IV. CONCLUSION

A single-slope ADC which leverages two-step time-to-digital conversion along with post-processing was presented.
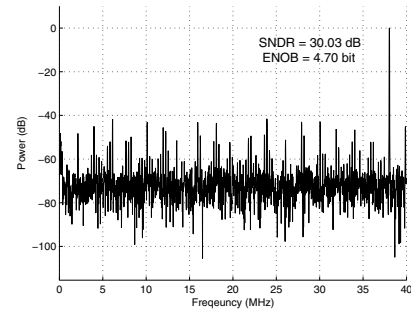
The resulting structure is simple and compact, and the two-step conversion allows a power-efficient means of performing the time-to-digital conversion operation with wide range and high resolution. The overall ADC achieves 6.45 bit of ENOB at 80 MS/s with 6.4mW of power dissipation.

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