A Dual Band 1.8GHz/900MHz, 750kb/s GMSK Transmitter Utilizing a Hybrid PFD/DAC Structure for Reduced Broadband Phase Noise

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Abstract

This paper presents the key circuits of a 1MHz bandwidth, 750kb/s GMSK transmitter. The fractional-N synthesizer forming the basis of the transmitter uses a combined phase-frequency detector (PFD) and digital-to-analog converter (DAC) circuit element to obtain >28dB high frequency noise reduction when compared to classical ΣΔ frequency synthesis. This large reduction in phase noise makes high bandwidth, low noise (-154 dBc/Hz @ 20 MHz offset for 3.565GHz output) synthesis possible, allowing direct modulation transmission of GMSK data at 750kb/s.

Keywords: fractional-N, frequency synthesis, CMOS, GMSK , transmitter, phase noise

Background

Direct modulation of fractional-N synthesizers acting as transmitters has become an active area of research [1]. A key limitation in such systems is that the low-pass filter response of the synthesizer dynamics causes inter-symbol interference in the transmitted data. Techniques have recently emerged that focus on increasing synthesizer bandwidth [1], [2]. The biggest obstacle to achieving high performance in such approaches is the increased output phase noise due to the reduced suppression of quantization noise.

The quantization noise component of fractional-N synthesizers is produced by the fractional-N dithering process. In state-of-the-art ΣΔ fractional-N synthesizers this noise has a high-pass shaped profile, and becomes dominant at offset frequencies higher than the PLL bandwidth. As synthesizer bandwidth is increased, more of the shaped quantization noise feeds through to the output, giving rise to an undesirable noise-bandwidth tradeoff.

Proposed Technique

In [3], we proposed and simulated a fractional-N architecture capable of dramatically lowering quantization noise. The system block diagram is shown in Fig. 1. A new circuit element, the PFD/DAC, combines the functionality of phase detector, charge-pump, and a noise cancellation digital-to-analog converter (DAC) into one circuit. The hybrid structure generates an inherent gain match between the quantization noise signal present in the PFD output and the cancellation DAC, an advantage over other architectures that use a separate DAC cancellation path [1], [2]. Also, unlike a prior approach to combine these circuits [4], the proposed PFD/DAC accounts for internal mismatch sources, and is therefore capable of high levels of noise rejection. A detailed system model of PFD/DAC operation is presented in the modeling paper [3].

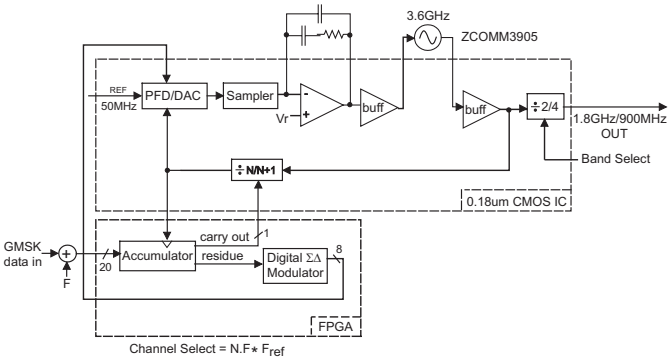

Fig. 1 Transmitter System Block Diagram

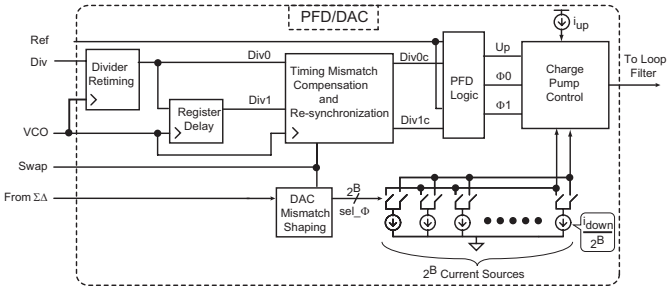

Fig. 2 PFD/DAC Block Diagram

In this paper, we present circuit design techniques for implementing the proposed PFD/DAC structure, and show measured results of a custom 0.18um CMOS fractional-N synthesizer that utilizes the PFD/DAC to achieve 750kbit/s in-band modulation at 1.8GHz/900MHz while simultaneously achieving -160/-166 dBc/Hz phase noise at 20 MHz offset.

PFD/DAC Circuitry

The PFD/DAC block diagram and operation is depicted in Fig. 2. The charge-pump circuitry is controlled by a phase/frequency detector logic block that compares the reference input to the divider output before and after it is delayed by one VCO period. This dual comparison generates a PFD/DAC output which is proportional to the phase error signal (in time) as well as the desired DAC cancellation

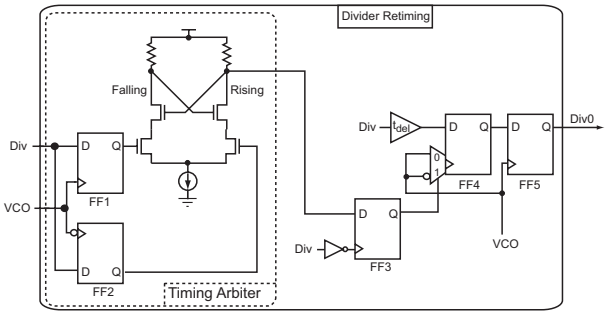

Fig. 3 Divider Retiming Circuit

signal (in magnitude). In order to properly cancel the quantization noise we desire [5]

$$-\varepsilon\alpha_{dac}T_{dac}I_{dac} = \varepsilon\alpha T_{vco}I_{cp} \quad (1)$$

where ε is the instantaneous quantization error ($0 < \varepsilon < 1$), α the PFD gain, I_{cp} the charge-pump current, T_{vco} the VCO period, α_{dac} the DAC gain, I_{dac} the full-scale DAC current, and T_{dac} the time the DAC is pulsed on. Eqn. 1 shows that the ultimate goal of the PFD/DAC is to create a charge pulse that is proportional to $T_{vco}I_{cp}$ weighted by the instantaneous quantization error. By combining the PFD and DAC into one circuit, the PFD/DAC technique achieves inherent matching between the two sides of Eqn 1.

Three primary design challenges present themselves when implementing the PFD/DAC structure. A description of each challenge, and our proposed solutions are discussed in this section.

A. Divider Resynchronization

To generate a one VCO period wide charge window, the divider signal is compared to the reference signal before and after it is delayed by one VCO period as shown in Fig. 2. High speed, multi-modulus divider architectures are asynchronous in nature, and exhibit a highly variable propagation delay. The divider must be retimed to the VCO before being clocked by the register delay cell of Fig. 2, which presents the challenge of avoiding meta-stability in the retiming flip-flop.

To avoid meta-stability in the retiming flip-flop, we propose the architecture of Fig. 3, where all flip-flops are resistively loaded, differential logic unless otherwise noted. The key idea of this approach is to *dynamically* choose either the rising or falling edge of the VCO output for retiming based on *detection* of which edge minimizes the likelihood of meta-stability. To allow either retiming edge signal to be used, the divider output edge is clocked on both rising and falling clock edges of the VCO into flops FF1 and FF2. For detection, a differential arbiter, which utilizes a cross-coupled latching structure, is used to determine which clock edge corresponds to a valid output.

The output from the arbiter is sampled on the divider falling edge by a low speed flip-flop, FF3, which forms a simple control FSM for register FF4. To provide timing margin, the divider input to FF4 is delayed by approximately

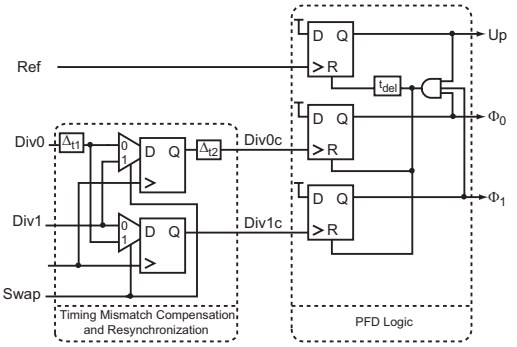

Fig. 4 Timing Mismatch Compensation and PFD Logic

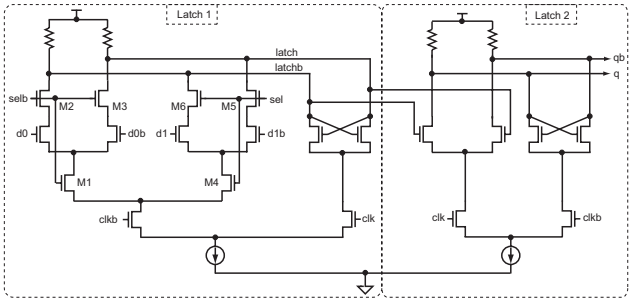

Fig. 5 High Speed Differential Flip-Flop With Mux Input

a flip-flop setup-and-hold time via the t_{del} block, and the divider is retimed on the opposite edge output from the arbiter. This ensures proper retiming across all possible asynchronous delays through the divider. FF5 acts as a final clean-up stage by always retiming the divider output on a rising edge so that the retimed divider signal will be in phase with the delayed divider signal used by the PFD/DAC. Hspice simulations indicate that the arbiter resolution is on the order of a few ps, which is more than enough granularity since there is a half-cycle delay between arbiter inputs.

The proposed divider resynchronization approach differs from proposals in [1] and [6] in that divider output phase and potential meta-stability is measured directly, and progressive retiming logic is avoided.

B. Phase Swap Circuitry

Fig. 4 shows the circuitry used to implement the timing mismatch compensation and PFD logic blocks depicted in the system diagram of Fig. 2. A key non-ideality in the circuit is mismatch between the two phase paths *Div0* and *Div1*,which is represented by Δ_{t1}, and results in the charge pulse window equaling to $T_{vco}+\Delta_{t1}$, rather than T_{vco}. This timing mismatch leads to a gain mismatch in Eqn. 1, and results in incomplete quantization noise suppression.

To mitigate the effect of timing mismatch, two techniques are implemented in the timing mismatch compensation and re-synchronization block. The first is to apply retiming to eliminate the effect of Δ_{t1}. There will now be a time mismatch, Δ_{t2}, referred to the *output* of the retiming flip-flops. The second technique is to swap the phase paths, so that both the divider and delayed divider signals will see the same average delay and the average time window becomes equal to T_{vco}. Note that it is important that the swap action appear

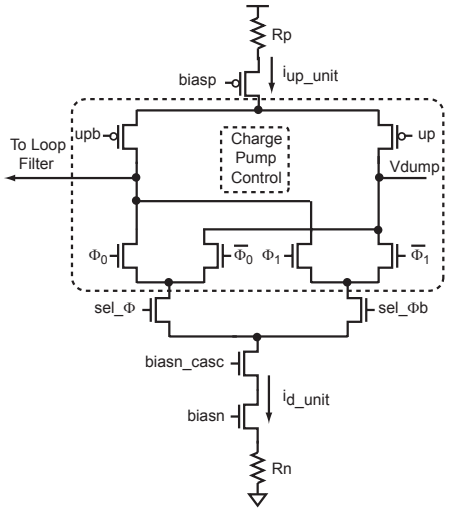

Fig. 6 Charge-pump Unit Element

random with a mean value of 0.5 so that Δ_{t2} is truly averaged between the two paths. For this reason, swap control is done via a 25 register (low power CMOS) linear feedback shift register (LFSR) random number generator clocked at the reference frequency.

Fig. 5 shows the high speed differential flip-flop architecture used in the timing mismatch compensation block. Typically, only transistors M1 and M4 are used in the first latch stage if an input multiplexer function is desired. However, without transistors M2, M3, M5, M6, there will be a change in loading at the internal nodes *latch* and *latchb* as the de-selected phase signals switch. These transistors eliminate this state mismatch, reducing residual timing error Δ_{t2}.

The PFD logic shown in Fig. 3 is that of a simple tri-state detector, where the Up signal reset has been delayed by t_{del} to improve phase detector linearity.

C. DAC Unit Element Design

The key source of mismatch in the charge-pump portion of the PFD/DAC is device mismatch between the unit elements comprising the charge-pump. For this reason, a DAC mismatch compensation block is used, as shown in Fig. 2. This block consists of a thermometer decoder and data weight averaging (DWA) circuit, which work to shape mismatch noise to high frequencies. The output control signals (*sel_Φ*) choose which phase path each unit element is associated with. Detailed simulations of the DWA are presented in [5] and suggest that the mismatch noise is well below the quantization noise when the mismatch compensation block is employed.

The unit elements themselves must simultaneously exhibit low noise and work at high speed. Fig. 6 depicts the proposed unit element current sources. A differential architecture is chosen for high speed operation. The control signal from the DAC mismatch shaping block steers $i_{d\text{-}unit}$ to be delivered either on *Φ0* or *Φ1*. As the phase paths in the timing block are swapped, the control signals must also be swapped. This is done by processing the control signals through a mux and inverter. To reduce current noise, degeneration resistors are used [7]. This reduces drain current noise as

$$i_{cpn}^2 \Rightarrow i_{cpn}^2 /(1+gmR_n + R_n / r_o)^2 \qquad (2)$$

where gm is the current source transistor transconductance, R_n is the degeneration resistor, and r_o the transistor output resistance. The tradeoff is noise introduced by Rn and lost headroom. We chose R_n = 5kOhm and i_{down}=39uA, for a 200mV drop across the resistors. Hspice noise simulations show R_n induced current noise is insignificant, and low frequency noise reduction by degeneration is approximately 20dB.

The charge pump output is single ended, and so when the current is not used, it is dumped to a known voltage, V_r. An active loop filter is used to minimize the impact of charge-pump finite output impedance modulation on its output current. Shown in Fig. 1, the active filter employs an op-amp in feedback. The voltage seen by the charge-pump is equal to V_r, meaning both sides of the differential structure in Fig. 6 see equal voltage conditions during operation.

Transmitter Architecture

We now look at a target application for the synthesizer - a direct in-band modulated GMSK transmitter, shown in Fig. 1. To allow flexibility in testing, the VCO, loop filter, and 1st order ΣΔ modulators are implemented off-chip. A 7 bit PFD/DAC is employed by the synthesizer, and a sampling network is inserted between the PFD/DAC output and the loop filter to reduce the impact of reference feed-through on the output spectrum.

Since GMSK uses phase modulation, a dual band transmitter is obtained by having a simple band select divider after the 3.6GHz VCO. Dividing by 2 or 4 achieves 1.8GHz or 900MHz bands, respectively. The GMSK data modulation index is multiplied by 2 or 4 so that, after the divide operation occurring in the band select divider, the data is properly formatted.

Measured Results

Fig. 7 is a die photo of the fabricated 0.18um CMOS synthesizer. Table I presents a list of specifications.

The synthesizer is first tested with an un-modulated input. Fig. 8 shows measured phase noise plots comparing the PFD/DAC synthesizer to a classical 2nd order ΣΔ fractional-N synthesizer. Measurements were taken with an Aeroflex PN9000B phase noise measurement system. With synthesizer bandwidth set to be 1MHz, the phase noise of the classical synthesizer is dominated at intermediate to high offset frequencies by quantization noise. The PFD/DAC reduces this noise by > 28dB at a 10MHz offset frequency! Noise is -98dBc/Hz at 200kHz offset frequency, and -154dBc/Hz at 20MHz for a 3.565GHz output. This is equivalent to -160dBc/Hz and -166dBc/Hz for the 1.8GHz and 900MHz bands, respectively.

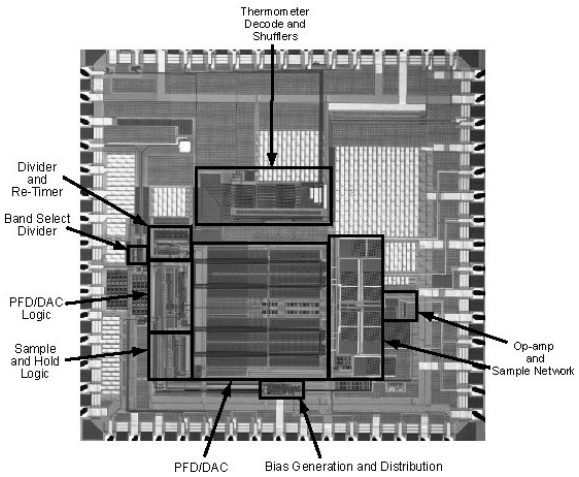

Fig. 7 Chip Microphotograph

Process	0.18um CMOS (National Semiconductor)
Data Rate	750kb/s GMSK (900MHz / 1.8GHz Bands)
Reference	50MHz
Phase Noise (3.6GHz output)	-98dBc/Hz @ 100kHz -154dBc/Hz @ 20MHz
Chg-pump Current	5mA at 7bit resolution
Analog Power	51mA @ 1.8V = 92mW
Digital Power	3.6mA @ 1.5V = 5.4mW
VCO, Ref, and I/O buffer power	37mA @ 1.8V = 66mW
Chip Area	2.7X2.7mm (1.8X1.5mm active)

Table I. Chip Specifications

Table II compares the PFD/DAC synthesizer with two recent synthesizers that use a separate cancellation DAC to reduce phase noise. In the table, noise measurements have been normalized to 2.1GHz. Noise at a 10MHz offset is compared to demonstrate the ability of the PFD/DAC to reduce the impact of quantization noise, which is dominant at high offset frequencies. Note that the PFD/DAC achieves excellent noise performance with very simple divider and DAC control.

Fig. 9 shows measured output spectra and demodulated eye diagrams for the transmitter in the 1.8GHz and 900MHz bands respectively. The eye diagrams were measured using an HP 89440A Vector Signal Analyzer. By reducing the impact of quantization noise and achieving a high bandwidth, the PFD/DAC synthesizer is able to achieve a very high data rate while achieving excellent phase noise performance.

Acknowledgements

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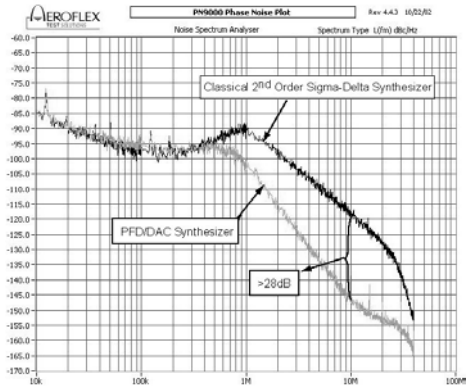

Fig. 8 Measured Phase Noise at 3.565GHz

	Div Control	DAC Control	BW	Noise @10MHz
[1]	2nd Order ΣΔ	3rd Order ΣΔ	460kHz	-133dBc/Hz
[2]	3rd Order ΣΔ	2nd Order ΣΔ	700kHz	-135dBc/Hz
This Work	1st Order ΣΔ	1st Order ΣΔ	1MHz	-151dBc/Hz

Table II. Synthesizer Comparison Table

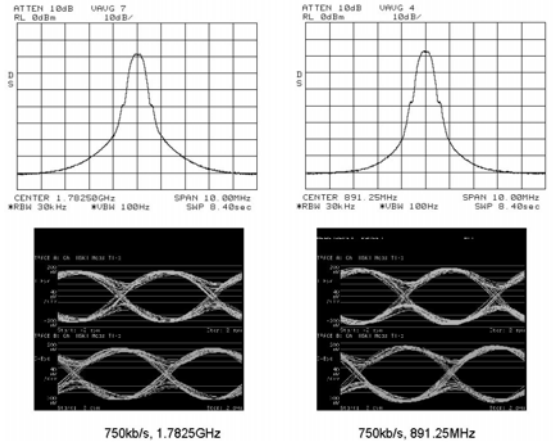

Fig. 9 Output Spectra and Eyes at 891 MHz and 1.78 GHz

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