Bandwidth Extension of Low Noise Fractional-N Synthesizers

Scott E. Meninger, Michael H. Perrott

Massachusetts Institute of Technology, Cambridge, MA, 02139, USA

***Abstract* — This paper examines issues with extending the bandwidth of fractional-N synthesizers. Quantization noise is shown to be the limiting factor in state-of-the-art fractional-N synthesis. A re-framing of the noise model used to analyze synthesizer phase noise leads directly to a methodology to enable high bandwidth synthesis. We present measured results from a synthesizer based on the proposed methodology that demonstrates >25dB broadband phase noise reduction compared to a state-of-the-art ΣΔ synthesizer. Finally, we draw conclusions about the future direction of fractional-N synthesis.**

***Index Terms* — Frequency Synthesis, fractional-N, phase noise, sigma-delta, jitter.**

I. Introduction

Frequency synthesis is an important technique used in a wide variety of communications systems. Ideally, a synthesizer has high bandwidth and low phase noise, which will be shown to be in direct conflict. The classical ΣΔ fractional-N frequency synthesizer is depicted in Fig. 1. This structure corresponds to a phase-locked-loop (PLL), where a low frequency reference is compared by a phase/frequency detector (PFD) to a divided down voltage controlled oscillator (VCO) output. The error pulses produced by the PFD control a charge-pump, whose output is then filtered and used to control the VCO. Fractional-N synthesizers simultaneously achieve fine resolution and high bandwidth by dithering the divide value between integer values (N and N+1 in Fig. 1) to achieve a fractional divide value, N.F.

Dithering introduces quantization noise into the synthesizer, negatively impacting phase noise performance. The ΣΔ fractional-N synthesizer [1] of Fig. 1 uses a ΣΔ modulator to dither the divider, shaping the quantization noise to high frequencies. This shaped noise is then filtered by the PLL low-pass dynamics. As Fig. 1 shows, a noise-bandwidth tradeoff arises. As the PLL bandwidth is increased, more quantization noise appears at the output. In order to achieve a given noise specification, the bandwidth must be lowered. This noise-bandwidth tradeoff contradicts the goal of fractional-N synthesis of increasing bandwidth!

We will examine issues with increasing bandwidth and maintaining low noise. Since quantization noise is the limiting factor to obtaining high bandwidth synthesis, we focus on ways to minimize its impact. A synthesizer architecture that achieves a high quality gain match between the noise and a cancellation signal [2] will be discussed, with new measured results presented. This architecture borrows concepts from ΣΔ digital-to-analog converter (DAC) design. A new model which draws a parallel between the fractional-N synthesizer and a ΣΔ DAC provides insight about the effectiveness of the new architecture. Finally, we examine the impact of extended bandwidth on intrinsic synthesizer noise sources.

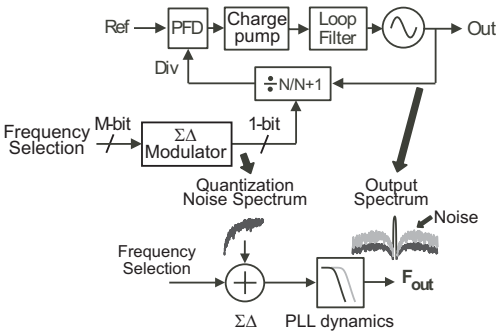

Fig. 1 Noise-bandwidth tradeoff in ΣΔ fractional-N synthesis

II. Noise Modeling

Phase noise performance can be separated into two components: *intrinsic* noise and *quantization* noise. Intrinsic noise is due to circuit elements present in any PLL, including reference input jitter, reference feed-through, charge-pump noise, and VCO phase noise. Quantization noise, which is caused by dithering, is particular to fractional-N synthesizers, and our key focus.

A. Quantization Noise

Fig. 2 presents the noise model for a ΣΔ synthesizer derived in [3]. In the model α is the PFD gain, I_{cp} the charge-pump current, K_V the VCO gain, T the reference frequency source's period, G(f) the low-pass filter response of the closed loop PLL dynamics, and N_{nom} the average divide value (N.F). The power spectral density (PSD) of the quantization noise appearing at the *output* of

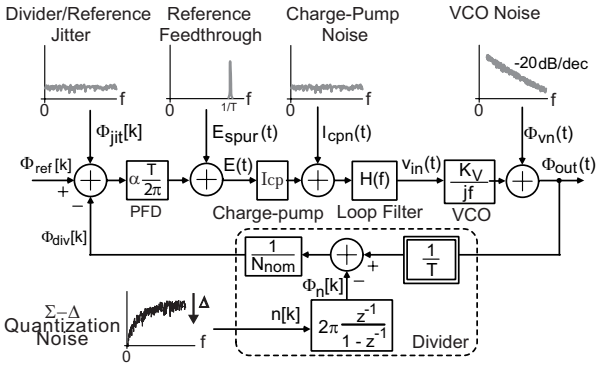

Fig. 2 Noise model for ΣΔ synthesizer from [3]

the synthesizer (after being filtered by the PLL dynamics) is [3]

$$10\log\left(\frac{\Delta^2}{12}\left|T \bullet G(f)\right|^2\left((2\pi)^2\left(2\sin(\pi fT)\right)^{2(K-1)}\right)\right) \text{ dBc/Hz} \quad (1)$$

where K is the order of the ΣΔ modulator used, a MASH ΣΔ structure is assumed, and Δ is the quantization step-size. In a ΣΔ synthesizer Δ = 1, because the phase quantization takes place via the divider, which is incremented in units of the VCO period.

Examination of Eqn. 1 reveals that options for reducing this noise are to increase K, decrease T, or decrease Δ. Increasing K means more complex ΣΔ circuitry and introduces a steeper noise shaping profile, requiring a higher order loop filter for attenuation. Decreasing T is a good option if the ΣΔ circuitry can operate at higher frequencies, but requires a high quality, high frequency, reference source.

Reducing Δ offers a large potential benefit because it decreases quantization noise by Δ^2. To decrease Δ, we re-examine classical phase interpolation based (PI) fractional-N synthesis [4]. Fig. 3 presents a model for a PI synthesizer, based on the noise model of Fig. 2. In PI synthesis, an accumulator (equivalent to a 1st order ΣΔ modulator [1]) is used as the dithering modulator, and a cancellation DAC is used to cancel the quantization noise. As the model shows, the DAC is feed-forward in nature, and a very good gain match must exist in order to cancel the quantization noise. We require

$$-\varepsilon_{S1}\alpha_{dac}T_{dac}I_{dac} = \varepsilon_{S1}\frac{\alpha T I_{cp}}{N} = \varepsilon_{S1}\alpha T_{vco}I_{cp} \quad (2)$$

where Tvco is the VCO period. Eqn. 2 shows that the charge delivered by the DAC, $-\varepsilon_{S1}\alpha_{dac}T_{dac}I_{dac}$ must match the error charge $\varepsilon_{S1}\alpha T_{vco}I_{cp}$, where ε_{S1} is simply a function weighting the error charge caused by the fractional-N process, and varies between 0 and the quantization step-

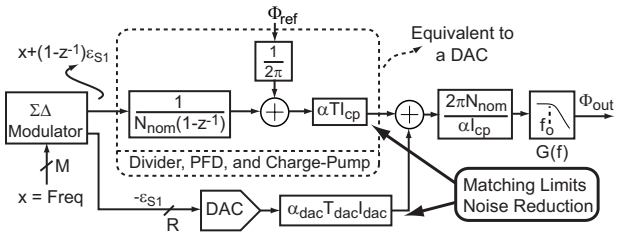

Fig. 3 New model for PI fractional-N synthesizer

size, Δ = 1. Eqn. 2 also shows that the fundamental charge packet of importance in the system is equal to $\alpha T_{vco}I_{cp}$.

These observations lead to several informative conclusions. First, the cancellation charge should be referenced to a single VCO period and full-scale charge-pump current for maximum effect. This is not the case in classical PI synthesis. Because T_{vco} is very small (typically 100's of ps to 10ns), T_{dac} is usually set to be many VCO periods so that the DAC output can settle [5], [6]. This requires the DAC to have even more resolution to counteract a large T_{dac}.

Second, any difference between the feed-forward DAC path and error signal results in a gain error, and incomplete cancellation. Gain mismatch is the limiting factor in classical PI synthesis. Recent approaches have used separate cancellation DAC paths, and large T_{dac}, and are therefore limited in their ability to cancel the quantization noise.

Finally, in classical PI synthesis the DAC is not noise shaped, and so the remaining error after cancellation has a white PSD, placing even more burden on DAC resolution. This conclusion becomes obvious once we realize that the model of Fig. 3 is directly analogous to a MASH ΣΔ DAC [7].

B. Proposed Solution

Fig. 4 shows our proposed solution [2], and Fig. 5 a new model of the synthesizer. If we embed the cancellation DAC inside the same circuit blocks where the error signal is produced, we can obtain an *inherent* gain match between them. Now the left and right hand sides of Eqn. 2 are matched! As suggested in the previous section, we also use ΣΔ control of the DAC to obtain good low frequency noise performance.

The PFD, charge-pump and DAC are now one structure, which we denote the PFD/DAC. The proposed PFD/DAC is different from prior attempts at combining these circuits [8], in that it accounts for mismatch sources internal its structure. System details and behavioral simulations of the architecture are presented in [2].

Once the quantization noise represented by ε_{S1} is cancelled, the quantization noise output PSD is expressed

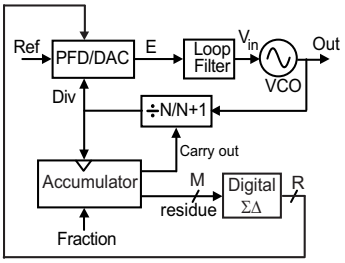

Fig. 4 Block diagram of PFD/DAC synthesizer

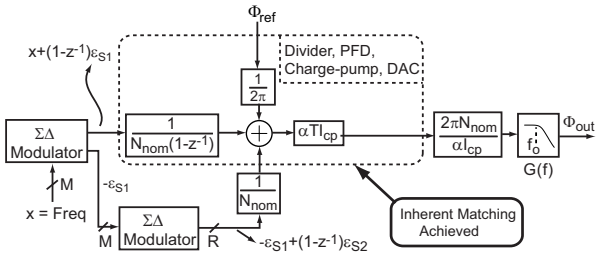

Fig. 5 New model for PFD/DAC synthesizer

exactly as in Eqn. 1, with the exception that now Δ is reduced by a factor of 2^R, ($\Delta \rightarrow \Delta/2^R$), where R is the number of bits controlling the cancellation DAC in the PFD/DAC.

C. Intrinsic Noise

Bandwidth extension also has an impact on intrinsic noise. Table I summarizes system noise sources. Sources such as substrate, supply, and bond-wire coupling are not included, since their transfer functions depend on process and layout.

Reference jitter induced phase noise is proportional to N_{nom}^2. We therefore desire to lower N_{nom}. A lower divide value implies a higher reference frequency to maintain the same output frequency. This suggests that a low-noise, high frequency reference source is desired. One promising solution is to use a multiplying delay locked loop (MDLL) as the reference. MDLLs offer less potential phase noise than VCOs by eliminating noise accumulation occuring in the VCO.

Charge-pump induced phase noise is improved by decreasing device noise, and decreasing N_{nom}. While device noise is technology limited, clever circuit design can improve performance somewhat. Increasing the full-scale value of charge-pump current, assuming current noise remains constant, also improves noise performance, but there are practical limits as to how much I_{cp} can be increased.

VCO noise is limited by technology advances. On-chip inductors have Q's of 10-20, limiting noise performance. MEMs resonators have been explored as a possible

Noise Source	**PSD**	**Desired Change**
Reference Jitter	$TN_{nom}^2 \lvert G(f)\rvert^2 \phi_{jitt}^2$	$\downarrow N$
Charge-Pump	$\left(\frac{2\pi N_{nom}}{\alpha I_{cp}}\right)^2 \lvert G(f)\rvert^2 i_{cpn}^2$	$\downarrow N \downarrow i_{cpn}^2 \uparrow I_{cp}$
VCO	$\lvert 1-G(f)\rvert^2 \phi_{vn}^2$	$\uparrow BW \downarrow \phi_{vn}^2$
Quantization	Eqn. 1	$\downarrow \Delta, \downarrow N \uparrow K$

Table I. Noise sources in a fractional-N synthesizer

alternative and potentially offer very high Q (~1000's), with the added cost of area and integration challenges. One promising area of research is the digital VCO [9], which does not overcome the issue of VCO noise itself, but offers the possibility of direct digital VCO control, and the elimination of the charge-pump and its noise. Raising synthesizer bandwidth also reduces VCO induced phase noise, reinforcing our desire to obtain a high bandwidth synthesizer.

III. Measured Results

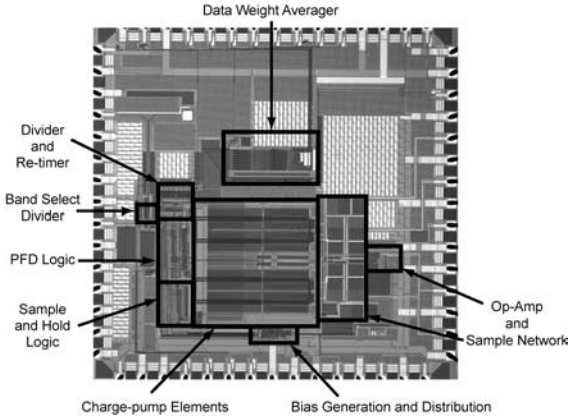

Fig. 6 Fabricated 0.18um PFD/DAC Chip

Here we show measured results for a fabricated PFD/DAC synthesizer whose chip microphotograph is shown in Fig. 6. In order to allow flexibility in testing, the VCO, loop filter, and ΣΔ modulators are implemented off-chip. A 7 bit PFD/DAC is used, with the divider and high speed PFD structures designed for a 3.6GHz VCO frequency. The synthesizer reference input frequency is 50MHz.

Fig. 7 shows a phase noise measurement comparing the PFD/DAC synthesizer with a classical 2nd order M.A.S.H. ΣΔ synthesizer. Quantization noise is reduced by > 25dB at a 10MHz offset frequency! Fig. 8 is a noise suppression plot, demonstrating that the PFD/DAC synthesizer

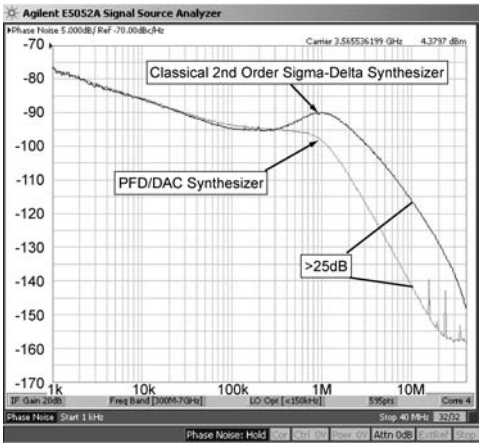

Fig. 7 Measured phase noise plot

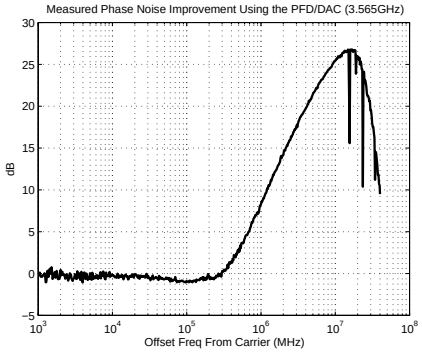

Fig. 8 Measured noise suppression using the PFD/DAC

attenuates quantization noise significantly, while achieving a very high (1MHz) bandwidth. Very recently, in [5] and [6], a high order noise shaped cancellation DAC and high order ΣΔ synthesizer configuration have been proposed. Noise suppression is limited in these cases by the separate DAC cancellation path and gain mismatch. Table II compares the PFD/DAC synthesizer with [5] and [6]. All phase noise numbers have been normalized to 2.1GHz.

As Table II shows, the PFD/DAC is able to obtain excellent results, simultaneously achieving a 1MHz bandwidth and excellent phase noise levels, while using simple 1st order ΣΔ modulators as divider and DAC control. Therefore, this technique is very promising.

IV. Conclusions

The goal of achieving low levels of phase noise and high bandwidth simultaneously is an active and exciting area of research. As bandwidth is extended and noise levels reduced, new opportunities arise at the system level. In particular, transmitters where the synthesizer is directly modulated with data, high bandwidth means a higher data rate is possible. We believe that a combination of the reduction of quantization step-size Δ via the PFD/DAC

	Div Control	DAC Control	BW	Noise @10MHz
[5]	2nd Order ΣΔ	3rd Order ΣΔ	460 kHz	-133dBc/Hz
[6]	3rd Order ΣΔ	2nd Order ΣΔ	700kHz	-135dBc/Hz
This Work	1st Order ΣΔ	1st Order ΣΔ	1MHz	-151dBc/Hz

Table II Comparison of PFD/DAC with prior work

architecture (R = 3 to 5 bit), combined with a higher on-chip reference frequency (100's of MHz to GHz) generated by an MDLL offers the best overall potential benefit. Combinations of these techniques with more digital sub-systems, such as a digital VCO, are also promising.

Acknowledgements

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