A Low Noise Programmable Clock Multiplier based on a Pulse Injection-Locked Oscillator with a Highly-Digital Tuning Loop

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***Abstract* — This paper introduces a pulse injection-locked oscillator (PILO) that provides low jitter clock multiplication of a clean input reference clock. A mostly-digital feedback circuit provides continuous tuning of the oscillator such that its natural frequency is locked to the injected frequency. The prototype uses a 50 MHz reference input to generate a 3.2 GHz output with integrated phase noise, reference spur, and estimated deterministic jitter of 134 fs (rms), - 63.4 dBc, and 211 fs (peak-to-peak), respectively.**

***Index Terms* — correlation, injection locked oscillators, jitter, phase locked loops, time measurement.**

I. Introduction

There has recently been increasing interest in CMOS circuits that leverage injection-locked oscillators, including frequency dividers [1], clock and data recovery circuits [2], and clock multipliers [3]. However, in each of these cases, the injected oscillator is not continuously tuned to the input signal while the injection-locking is taking place. Instead, the tuning voltage is either kept constant [1], adjusted according to a replica VCO in a PLL [2], or initially tuned to bring the natural frequency of the oscillator to a value close to the desired multiple of the injection frequency before injecting the signal into the oscillator with enough power to ensure locking [3].

The lack of tuning presents a potential problem in a practical context, especially for sub-harmonic injection locked oscillators such as [3], where the oscillator is locked to a *harmonic* of the input signal. In this case, the need to achieve an adequate injection power level such that injection-locking is maintained across thermal variations will potentially undermine the ability to achieve a low power implementation. While Injection-Locked Phase-Locked Loops (ILPLL) can provide continuous tuning during injection [4], they are prone to increased frequency spurs due to the mismatch between the injection and the PLL paths. A similar issue occurs with realigned PLLs as described in [5].

This paper aims to address the issue of continuous tuning of sub-harmonic injection locked oscillators by presenting a pulse injection-locked oscillator (PILO) structure combined with a recently introduced tuning technique [6] to provide tracking of the natural frequency of the injection-locked oscillator to the desired multiple of the injection source frequency. The highly-digital tuning technique practically eliminates detector path mismatch and analog loop non-idealities such as current mismatch in the charge pump, resulting in drastically reduced frequency spurs and, therefore, greatly reduced deterministic jitter [6].

II. Proposed Pulse Injection-Locked Oscillator

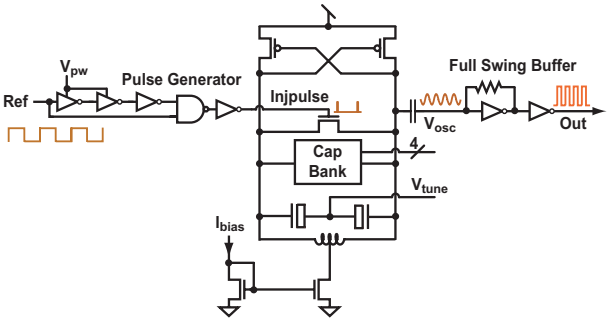

Fig. 1 Proposed PILO circuit.

Fig.1 illustrates the prototype PILO circuit in which injection locking of the LC tank of the oscillator is achieved by periodically shorting the tank with a switch that is driven by a train of narrow pulses. The pulse train frequency is set to a sub-multiple of the desired frequency (so that the PILO essentially performs integer-N frequency multiplication), and the width of the pulses is set to be much less than the period of oscillation so that the quality factor of the tank, Q, is not severely degraded. To achieve low jitter at the PILO output, the reference source must also have low jitter since its noise will be mostly passed to the oscillator output [5].

As shown in Fig. 1, the pulse generator consists of digital gates that generate the narrow pulses by performing an AND operation on the reference signal, *Ref,* and a delayed and inverted version of *Ref*. The injected pulse drives an NMOS transistor that shorts the differential output of the VCO. The VCO is biased from an NMOS current mirror through the middle tap of the

inductor and includes a varactor made of n-poly/n-well MOSCAP devices and a four-bit MIM capacitor bank that is used to increase the tuning range without a large tuning gain. The VCO-buffer consists of two inverters, the first of which is biased in feedback through a large resistor, which provide a squared version of the VCO output.

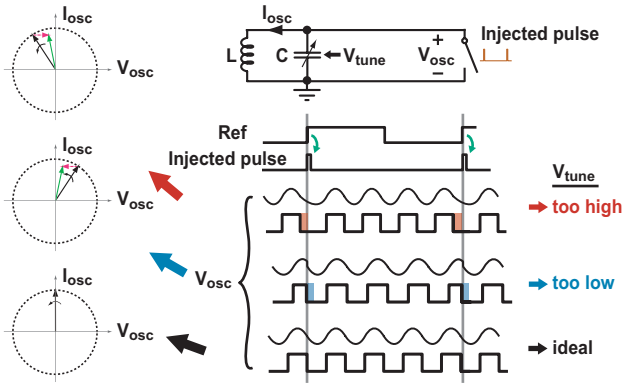

Fig. 2 Impact of frequency tuning on PILO output.

Although subharmonic injection locking is well understood [8], the following analysis facilitates an intuitive understanding of the PILO operation and offers a linearized context to model its phase noise using [5]. Proceeding with this analysis, Fig. 2 shows phasor diagrams that are normalized to the peak voltage and current of the tank, in which the phase vector periodically rotates around the unit circle as the energy of the tank alternates between the inductor and the capacitor. If the shorting pulse occurs when V_{osc} equals zero, it will have no effect (assuming the pulse is very narrow). On the other hand, if the shorting occurs before or after the zero crossing, the oscillator phase will be pushed towards the zero crossing point such that its phase is either advanced or delayed. When the oscillator is injection-locked, this periodic phase shifting will cause the average frequency to match the desired frequency even if the natural frequency of the oscillator is slightly different than the injection source frequency. However, since the injection is occurring at a sub-multiple of the oscillator frequency, the presence of such periodic phase shifting due to frequency offset will lead to a different cycle time for the oscillator during the injection cycle as compared to the free-running cycle time, and thereby induce deterministic jitter and frequency spurs at the output of the PILO.

The PILO injection effectiveness, β of the model in [5], and thus the injection bandwidth is affected by the amount of charge transferred due to the shorting operation. The smaller the resistance of the shorting switch, the higher the shorting current, and hence the higher the transferred charge. Increasing the width of the shorting pulses also increases the transferred charge, and hence increases β. However, this increase in β is at the expense of lowering the average Q of the tank, which effectively increases the VCO phase noise. In addition, a wider shorting pulse will have a larger residual effect even when injected at a zero crossing, and thus will result in larger residual deterministic jitter and reference spurs. As shown in Fig. 1, the supply lines of the first two inverters in the pulse generator, V_{pw}, can be adjusted to change the delay of those inverters, and thus the width of the shorting pulses, in order to study its effect on the PILO.

III. Tuning Error Detection

The aim of the feedback circuit is to sense the tuning error (manifested as deterministic jitter), and then tune the natural frequency of the LC oscillator (through its varactor) such that this tuning error is driven toward zero and the natural and injected frequencies become locked.

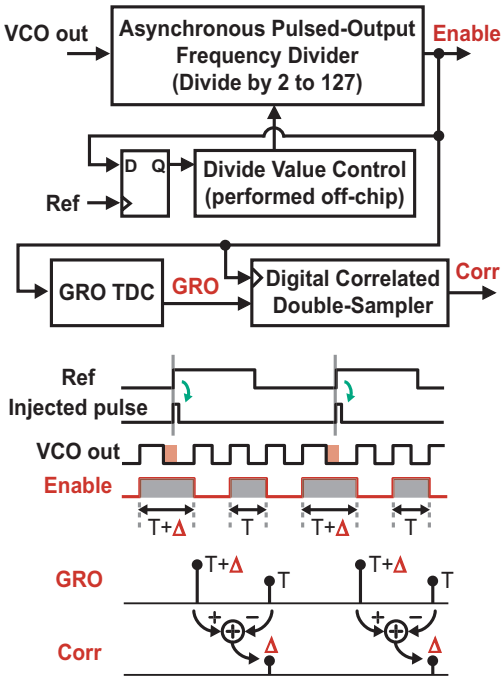

Fig. 3 Proposed technique of measuring deterministic jitter of the PILO output.

Fig. 3 illustrates the technique by which deterministic jitter due to pulse injection is measured, which is very similar to the method proposed in [6]. First, a frequency divider is used to produce an *Enable* pulse train that contains two pulses per reference cycle. The first pulse corresponds to the oscillator cycle period during which the injection occurred, and the second corresponds to the free-running cycle period. A gated ring oscillator (GRO)

time-to-digital converter (TDC), whose basic structure is described in [6,7], is used to measure the time periods of each pulse. The difference between those periods, Δ, is then determined by a digital correlated double-sampling circuit which simply subtracts the pairs of measured time values each reference period. By continuously tuning the varactor input voltage of the injection-locked oscillator such that average value of Δ goes to zero, the naturally running frequency of the oscillator will become locked to the desired multiple of the reference frequency.

In Fig. 3, note that the divider used to generate the *Enable* signal is similar to [9]. However, since the *Enable* pulses need to capture the period of specific cycles, the divider is stepped until an *Enable* pulse occurs during the injected cycle. This is accomplished by using a register that detects the presence of the *Enable* pulse, and a simple algorithm implemented off-chip that controls the divider, as shown in Fig. 3.

IV. Implemented Prototype

Fig. 4 shows a block diagram of the proposed prototype of the continuously tuned PILO circuit, which provides details of the feedback circuit used to tune the varactor of the LC oscillator such that the average value of Δ becomes zero. As shown in the figure, the prototype system consists of a custom 0.13 µm CMOS IC, an FPGA board, and an off-chip 16-bit DAC with a passive RC filter at its output. The prototype uses a 50 MHz reference input to generate an output at 3.2 GHz (and up to 4 GHz).

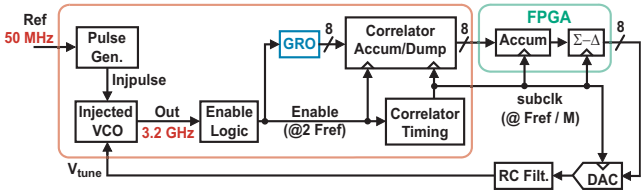

Fig. 4 PILO prototype and its frequency tuning feedback circuit.

The 0.13 µm IC, which contains the circuits in Figures 1 and 3, sends the correlator output to the FPGA, and provides an input varactor tuning port to adjust the natural frequency of the injection-locked LC oscillator. The correlator output can optionally be filtered and decimated by an accumulate-and-dump operation to reduce the rate of subsequent blocks. The FPGA first accumulates the correlator output, and then passes the resulting signal into a digital first-order Sigma-Delta modulator, which reduces the required DAC resolution to 8 bits (for the given RC filter bandwidth). The Sigma-Delta output is fed into the off-chip DAC, and its output is then fed into a passive RC filter (with 500 kHz bandwidth) that feeds into the varactor of the injection-locked LC oscillator.

V. Measured Results

Fig.5 shows the die photo of the custom 0.13 µm CMOS IC, which contains active circuit area of 0.4 mm^2. The power dissipation of the chip, not counting the output buffers, is 28.6 mW.

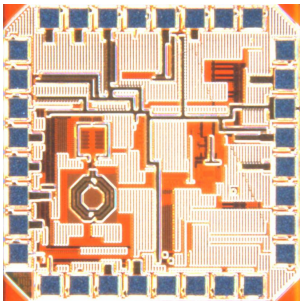

Fig.5 Die photo.

Fig. 6 displays measured phase noise from an Agilent E5052A signal source analyzer under the conditions of open-loop tuning of the PILO (where its natural frequency was manually tuned to match the injection frequency), and closed-loop tuning of the PILO using the feedback technique described above. The integrated phase noise (from 1 kHz to 40 MHz) is 101 fs (rms) for the open-loop tuned case, and 134 fs (rms) for the closed-loop tuned case. Note that the impact of the reference spur is not included on those values. As observed in Fig. 6, the open-loop tuned PILO achieves low phase noise at low frequencies due to the fact that injection-locking leads to suppression of the low frequency VCO phase noise [5, 8].

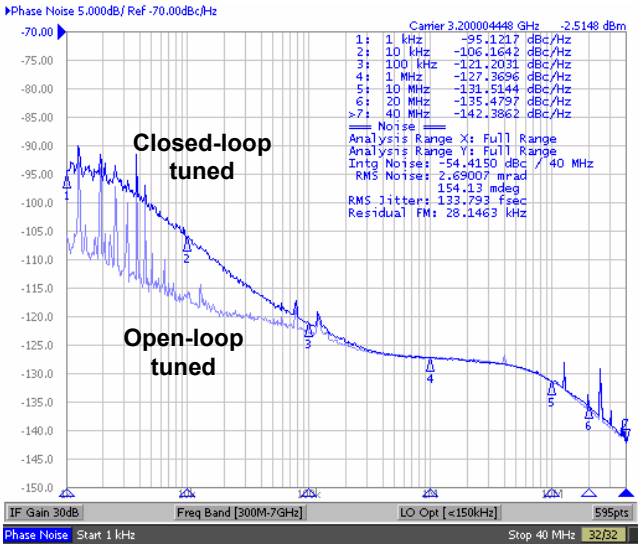

Fig. 6 Measured phase noise for the open-loop and closed-loop tuned PILO (at 3.2 GHz).

In contrast to the open-loop tuned PILO, the closed-loop tuned PILO in Fig. 6 has higher noise at lower frequencies due to the measurement noise induced by the GRO TDC, but represents a more practical implementation in which the natural oscillator frequency is automatically locked to the desired multiple of the injected frequency. The bandwidth of the closed-loop tuning is digitally set, and lowering it to reduce measurement noise does not result in the increased area or leakage encountered in analog loops. However, the loop bandwidth needs to be set high enough to track thermal variations, and is digitally set to about 2 kHz in this case.

Fig. 7 shows the phase noises of the open-loop tuned PILO in comparison to the reference source. Note that the open-loop tuned PILO exhibits -10 dB/decade roll-off at lower frequencies, which is the result of suppressing the -30 dB/decade roll-off of the free-running VCO at those frequencies, in addition to slight phase noise contribution from the reference source.

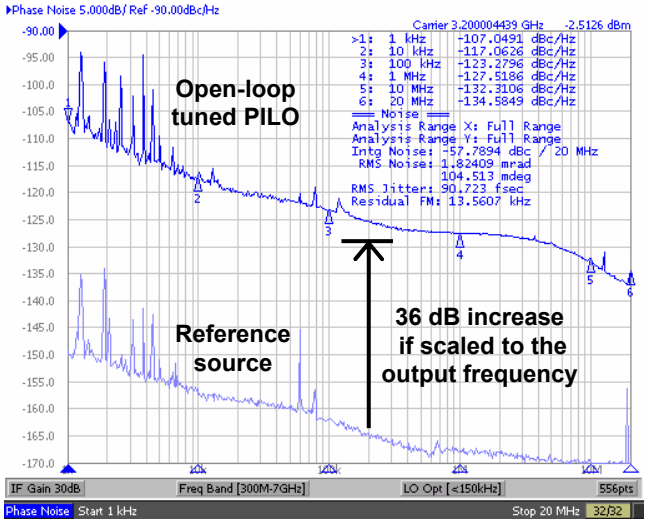

Fig. 7 Measured phase noise for the open-loop tuned PILO (at 3.2 GHz) and the reference source (at 50 MHz). Note that scaling the phase noise of the reference to the output frequency would increase it by 36 dB, i.e. 20 $\log_{10}$(3.2 GHz / 50 MHz).

Deterministic jitter, Δ, can be estimated from reference spurs in the measured output spectrum [6] using Equation (1), which is based on Fourier series analysis.

$$\Delta \approx T_{out} \times 10^{Spur(dBc)/20} \qquad (1)$$

T_{out} is the ideal output period, while *Spur* is the level of the reference spur, measured in units of dBc.

Fig. 8 shows the –63.4 dBc reference spur that was measured by an Agilent 8595E spectrum analyzer. Using Equation (1), the deterministic jitter is estimated at approximately 211 fs (peak-to-peak).

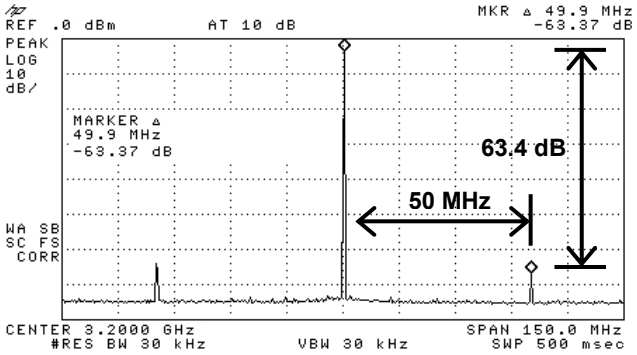

Fig. 8 Measured spurious performance of the close-loop tuned PILO (at 3.2 GHz).

ACKNOWLEDGEMENT

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