A Programmable MEMS-Based Clock Generator with Sub-ps Jitter Performance

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Abstract

A MEMS-based clock generator achieves sub-ps jitter in 0.18um CMOS. Key enabling techniques include a 48MHz MEMS oscillator, a reference doubler, a linear XOR-based PFD, a switched-resistor loop filter using accumulation mode NMOS varactors, and native NMOS devices with an RC filter. The overall output at 156.25MHz achieves an integrated phase jitter of 668fs rms over an integration bandwidth of 10kHz-20MHz.

Introduction

Virtually all electronic devices require an accurate clock, which traditionally has been provided by quartz crystals. Recently, programmable MEMS-based clocks have become available which leverage scalable semiconductor technology to combine high-Q MEMS resonators with a fractional-N PLL to achieve temperature compensation and continuous frequency programmability as shown in Fig. 1 [1]. This approach leads to many benefits, including the utilization of standard plastic packaging in which the MEMS die is wire bonded to a 0.18um CMOS die, direct access to the low cost, high volume manufacturing infrastructure of ICs, and short lead times through programmability. MEMS-based clocks have also shown temperature stability of <30ppm across the industrial temperature range [1]. However, a key challenge has been improving jitter performance to reach a wider application space. We address this challenge by 1) achieving a low noise 48MHz MEMS oscillator consisting of the wire-bonded MEMS die and circuits on the 0.18um CMOS die and by 2) utilizing several circuit techniques to minimize quantization, power supply, thermal and 1/f noise contributions of the fully integrated fractional-N PLL on the same 0.18um CMOS die.

System Architecture and PLL Circuit Techniques

The block diagram of the clock generator system is shown in Fig. 1. The output frequency can be programmed continuously between 1-330MHz. The MEMS oscillator produces a 48MHz reference clock with a phase noise <-140dBc/Hz at 10kHz offset. The PLL loop bandwidth is optimally set at 1MHz to balance the contributions from various noise sources as shown in Fig. 2, thereby enabling sub-ps integrated phase jitter across a 10kHz-20MHz bandwidth.

To lower the impact of quantization noise from the Sigma Delta modulator, the frequency doubler allows the modulator to operate at twice the reference frequency. This also halves the feedback divider ratio such that the reference, divider, and loop filter noise are correspondingly reduced [2].

To minimize the impact of Sigma Delta noise folding and to achieve high phase detector linearity, the traditional tri-state PFD is abandoned in favor of the XOR-based PFD shown in Fig. 3. In contrast to the tri-state PFD, which has three states and requires excellent matching for Up/Down charge pump currents to avoid linearity issues, the XOR-based PFD is inherently linear over a very wide operating range since it only has two possible states.

While the XOR-based PFD could be applied to a charge pump loop filter, it is beneficial to consider a switched-resistor loop filter [1] instead to lower the impact of 1/f noise. As shown in Fig. 4, 1/f noise is often reduced in charge pumps with degeneration resistors [4]. A switched-resistor can be viewed as an extreme case of degeneration such that 1/f noise is significantly lowered when compared to a charge pump.

Fig. 5 shows the switched-resistor loop filter topology, which consists of an inverter driving a passive RC network with polysilicon resistors and area-efficient accumulation-mode NMOS varactors. The impact of nonlinear capacitance versus voltage for C_1, C_2, and C_3 is reduced since the DC bias in steady state operation causes strong accumulation in these devices. Though C_f does not sustain a non-zero DC bias during steady-state operation, simulations and measurements confirm that the voltage deviations across C_f are small enough that its nonlinear capacitance to voltage characteristic does not cause significant noise folding of the Sigma-Delta quantization noise.

To reduce the impact of supply noise, a series of techniques are used. First, sensitive analog circuits are designed to operate at 1.5V in this 1.8V process to allow headroom for low noise 1.5V regulators. Separate 1.5V regulators then create segregated power domains for critical blocks requiring more isolation. A solid low-impedance ground plane (as opposed to a star-ground network) is poured in layout to short all the analog grounds of each power domain together and minimize any ground voltage differences within the chip. The solid ground plane also promotes a ground-based design methodology for low noise. Finally, native NMOS devices with RC filtering are used to further attenuate regulator noise, provide supply isolation, and reinforce a ground-referenced design. Native NMOS RC filters are used in the loop filter and all-PMOS LC-VCO, both of which are ground-based designs.

Measured Results

The programmable MEMS-based clock generator is implemented in 0.18um CMOS (Fig. 6). Of the total die area, the loop filter consumes 0.08mm^2, the native NMOS RC filter consumes 0.085mm^2, the LC-VCO consumes 0.4mm^2, and the rest of the PLL consumes 0.065mm^2 of area.

Fig. 7 is the measured output phase noise of the oscillator at 156.25MHz output and the MEMS oscillator at 48MHz. In this configuration, the chip consumes 34mA 3.3V under no load conditions, and can operate down to 1.7V. As seen, the overall output phase noise characteristic is dominated by the MEMS noise at low frequency and not by 1/f noise of the PLL. Integrated phase jitter from 10kHz to 20MHz yields 668fs rms.

This level of jitter performance enables a wider application space for programmable MEMS-based timing, including SONET clocking and 10Gbit Ethernet.

References

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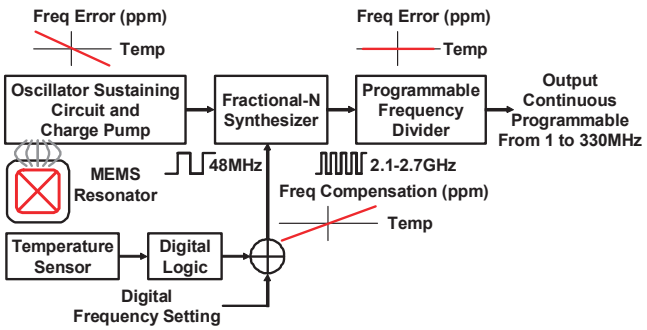

Fig. 1 MEMS-based clock generator consisting of MEMS die bonded to a 0.18um CMOS die containing all of the above circuits.

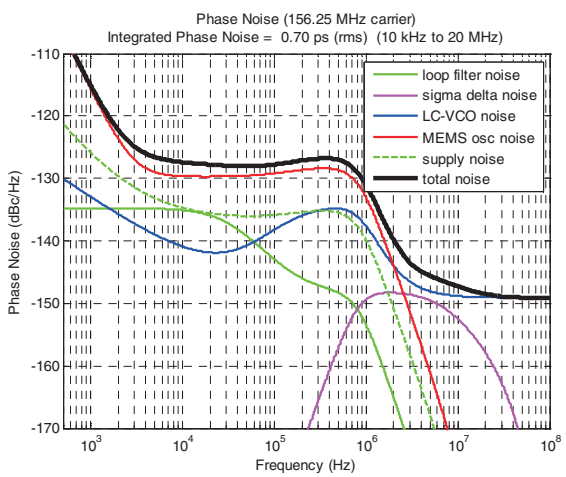

Fig. 2 Noise contributions to PLL phase noise at 156.25MHz output.

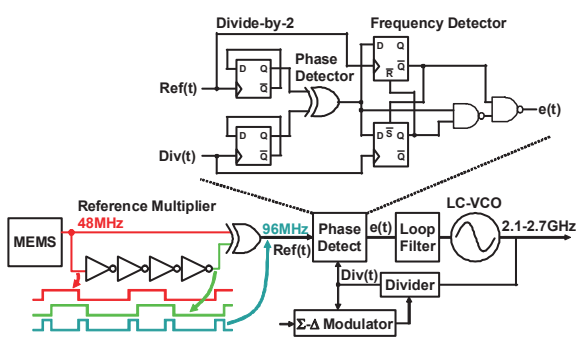

Fig. 3 Reference frequency doubler with XOR-based PFD.

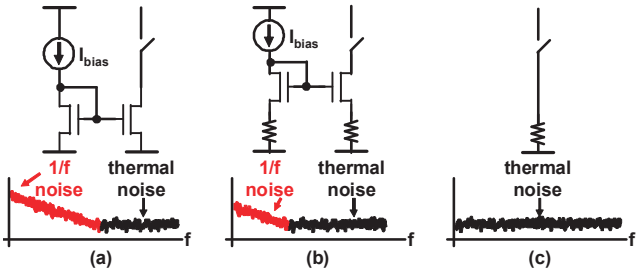

Fig. 4 Noise spectra for (a) charge pump, (b) degenerated charge pump, (c) switched-resistor.

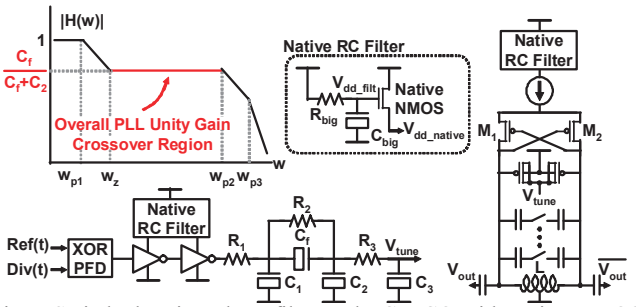

Fig. 5 Switched-resistor loop filter and LC-VCO with native NMOS supply filtering.

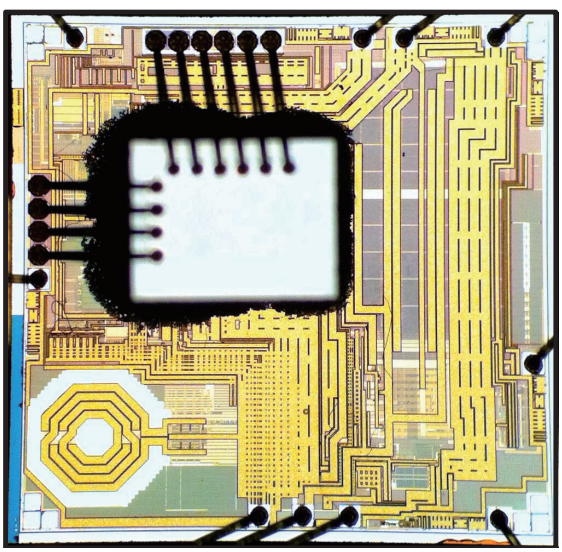

Fig. 6 Chip photo with MEMS resonator on top of 0.18u CMOS die.

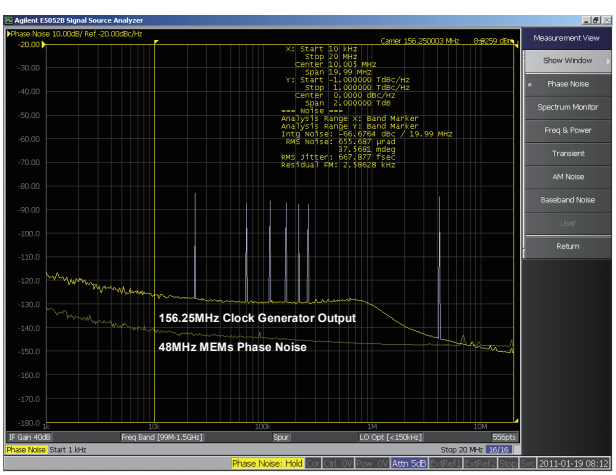

Fig. 7 Measured clock generator output phase noise at 156.25MHz and MEMS oscillator phase noise at 48MHz output.