A NUMERICAL DESIGN APPROACH FOR HIGH SPEED, DIFFERENTIAL, RESISTOR-LOADED, CMOS AMPLIFIERS

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ABSTRACT

A simple numerical procedure is introduced to allow straightforward design of high speed, resistor loaded, differential amplifiers in modern CMOS processes whose device characteristics dramatically depart from traditional square law characterisitics. The analytical form of the procedure allows for an intuitive perspective of the varying gain-bandwidth product for such amplifiers. Calculations based on the method are compared to Hspice simulated results based on a 0.18u CMOS process. Its application to the design of high speed, source-coupled logic (SCL) gates and latches is also discussed.

1. INTRODUCTION

CMOS analog design techniques have traditionally assumed square law characteritics for device I-V curves when calculating the impact of device properties on circuit performance. However, the square law assumption is quickly becoming highly inaccurate with the introduction of finer line width processes due to nonideal effects such as velocity saturation. As a result, the accuracy of traditional design equations is steadily degrading, and analog designers are in need of alternate approaches to such formulations.

Thus far, there have been two responses to dealing with changing device characteristics in the analog design community. The first has been to assume square law I-V characteristics in calculations, and then rely on a simulator such as SPICE to tweak in final device parameter adjustments. Unfortunately, the square law is rapidly becoming inaccurate to the point that the analytical calculations are practically useless — all design time is then spent on SPICE simulations. Such an approach removes intuition from the designer's grasp, leads to a lengthy design process (since many tweaks are required), and often leads to suboptimal performance. The second approach is to completely automate the analog design process — the user simply specifies performance specifications and some possible topologies, and customized software takes care of the rest [1]. Unfortunately, while very useful for the design of standard analog blocks, such an approach removes creativity from the designer's grasp and offers little intuition for the creation of new circuit topologies.

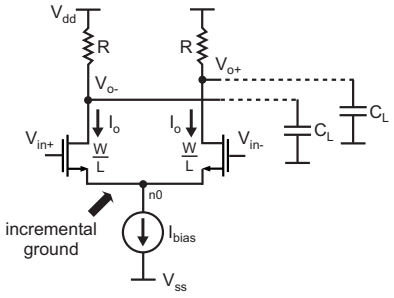

Fig. 1. Differential amplifier used in calculations.

We propose an alternate approach to this issue — develop numerical procedures for designing specific classes of circuits which resemble hand analysis, but use simulated device characteristics in place of analytical expressions. By sticking with procedures similar to hand analysis, much intution can be gained about design tradeoffs. By using simulated device characteristics, the results are made accurate so that little or no tweaking is required in SPICE.

This paper applies the above philosophy to the design of high speed, resistor-loaded, differential amplifiers. These structures are tremendously useful in circuit applications whose speed requirements exceed the abilities of full-swing logic circuits. Implications for the design of SCL latches, registers, and gates are also discussed.

2. BACKGROUND

Figure 1 displays a resistor-loaded, differential amplifier used in high speed applications. The resistors are often realized within a reasonably small area using unsilicided polysilicon, and introduce less capacitance than other loads such as triode PMOS devices or diode-connected NMOS devices. Further increases in bandwidth can be achieved at the expense of chip area by introducing inductors into the loads [2].

Design of resistor-loaded amplifiers entails choosing appropriate device sizes and resistance values given three design specifications:

- Allowable power dissipation: I_{bias}
- Desired voltage swing: V_{sw}
- Desired DC voltage gain: $|A_v|$

An additional specification for the amplifier is its bandwidth — its value is constrained by choice of the above three specifications as well as the load that the amplifier is required to drive (assumed capacitive). We define intrinsic bandwidth (BW) as the amplifier bandwidth that results when the amplifier drives an identical stage without additional wiring capacitance. Since actual circuits contain wiring capacitance, the intrinsic bandwidth offers only an upper bound on achievable performance, but is still a very useful metric. Note that, to achieve the maximum bandwidth, the transistor length, L, will always be assumed to be set to its minimum value for the discussion to follow.

Figure 1 allows us to relate the first two design specifications to other circuit parameters. When zero differential input voltage is applied to the amplifier, the bias current through each transistor is observed to be

$$I_o = I_{bias}/2.$$

As the input differential voltage is varied, the current through each resistor ranges between 0 and I_{bias}. Therefore, the maximum single-ended voltage swing at the amplifier output is

$$V_{sw} = I_{bias}R = 2I_oR \tag{1}$$

The third design specification, DC gain, is derived about the bias point of zero differential input voltage using the small signal transistor model shown in Figure 2. Here we have assumed that node $n0$ in Figure 1 is at incremental ground as the differential voltage is varied. Ignoring capacitance for this DC calculation, we write

$$|A_v| = g_m(R||\frac{1}{g_{ds}}) \;\Rightarrow\; g_m = |A_v|/R + |A_v|g_{ds} \tag{2}$$

Unfortunately, evaluation of the above equation requires calculation of g_m and g_{ds} as a function of the device bias current and size. As pointed out earlier, hand calculations assuming square law I-V characteristics prove inaccurate for this task. Our proposed method of addressing this issue is described in the following section.

3. PROPOSED APPROACH

We will now show that we can create a design framework in which all design calculations revolve around the solution of just one key variable given the three constraints described earlier. This key variable is current density, and is defined as

$$I_{den} = \frac{I_o}{W},$$

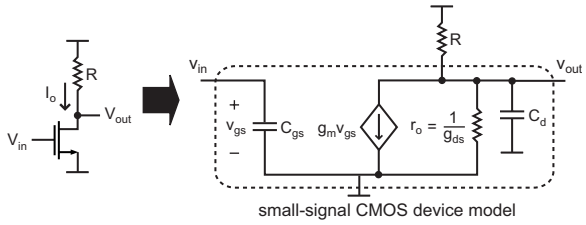

Fig. 2. Small signal model for amplifier.

where W is the width of the transistor as indicated in Figure 1.

Two key relationships involving current density will now be derived. The first is a gain/swing constraint formulation that will set the value of I_{den}. The second is a gain-bandwidth product expression that incorporates the impact of I_{den}.

3.1. Derivation of Gain/Swing Constraint Formulation

Given a fixed transistor length, $L = L_{min}$, both the g_m and g_{ds} values of a CMOS device are dependant primarily on the transistor width, W, and bias current I_o. Given a fixed value for I_o, as set by power dissipation requirements, it is straightfoward to sweep W of the device in SPICE to obtain simulated plots of $g_m(I_o, W)$ and $g_{ds}(I_o, W)$. We then define $g_{m0}(I_{den})$ and $g_{ds0}(I_{den})$ as

$$g_{m0}(I_{den}) = g_m(I_o, W)/W, \;\; g_{ds0}(I_{den}) = g_{ds}(I_o, W)/W \tag{3}$$

Let us now revisit the swing and gain constraints discussed in the Background section. Combining Equation 1 and Equation 2, we obtain

$$g_m = \frac{2|A_v|}{V_{sw}}I_o + |A_v|g_{ds}.$$

We relate g_m and g_{ds} to the simulated characteristics defined in (3) as

$$Wg_{m0}(I_{den}) = \frac{2|A_v|}{V_{sw}}I_o + |A_v|Wg_{ds0}(I_{den}).$$

Dividing through by W, we obtain the key gain/swing constraint formulation as a function of current density:

$$g_{m0}(I_{den}) = \frac{2|A_v|}{V_{sw}}I_{den} + |A_v|g_{ds0}(I_{den}) \tag{4}$$

The above expression states that current density is completely set by the choice of gain, swing, and the simulated g_m, g_{ds} curves.

3.2. Derivation of Gain-Bandwidth Tradeoff

To examine the tradeoff between gain and intrinsic bandwidth, we first note that the capacitive load can be approxi-

mately related to the amplifier device size as

$$C_L = WC_{L0} = W(C_{gs0} + C_{d0}), \tag{5}$$

where C_{L0} is the simulated capacitive load normalized to an effective W equal to one. Justification for the above expression follows from the fact that the amplifier is driving an identical structure for its load and that both C_{gs} and C_d scale linearly with the device width, W.

Calculation of the intrinsic bandwidth is computed as

$$BW(rad/s) = \frac{1}{RC_L} = \frac{2I_{den}}{V_{sw}C_{L0}}. \tag{6}$$

The amplifier gain is found through algebraic manipulation of Equation 4:

$$|A_v| = \frac{g_{m0}(I_{den})}{(2/V_{sw})I_{den} + g_{ds0}(I_{den})}. \tag{7}$$

The gain-bandwidth product is then found by combining the above two expressions:

$$|A_v| \cdot BW = \frac{g_{m0}(I_{den})}{C_{L0}} \frac{1}{1 + V_{sw}g_{ds0}(I_{den})/(2I_{den})}. \tag{8}$$

Given g_{ds0} is negligibly small, the above expression reverts to the classic g_m/C expression familiar to analog designers. However, one must note that g_m is a function of current density — the implications of this point will be brought home in the following section.

4. INTUITIVE INSIGHTS FROM METHOD

The first useful insight of the proposed method is that it provides an intuitive picture of the dependance of gain-bandwidth product on current density. Figure 3 displays a gain-bandwidth plot for a 0.18u NMOS device according to Equation 8. Each curve utilized a $g_{m0}(I_{den})$ curve and estimate of C_{L0} generated in Hspice from a SPICE model file for the 0.18u CMOS process. The top curve assumes $g_{ds} = 0$, while the bottom one includes its effect based on $g_{ds0}(I_{den})$ generated from Hspice. In either case, we see that gain-bandwidth product is increased as current density is increased, so that high current density is desirable in high speed applications.

The second useful insight of the proposed method is that it reveals that current density is not a free variable — it is determined by the gain and swing requirements of the amplifier as well as the $g_{m0}(I_{den})$ and $g_{ds0}(I_{den})$ characteristics of the device. Figure 4 displays a graphical interpretation of Equation 4 in setting the current density. Ignoring the influence of $g_{ds0}(I_{den})$, the current density is determined as the intersection of the $g_{m0}(I_{den})$ curve for the CMOS process with a straight line whose slope is $2|A_v|/V_{sw}$. As gain is increased relative to a given voltage swing, the line slope is increased and I_{den} must be reduced. Combining

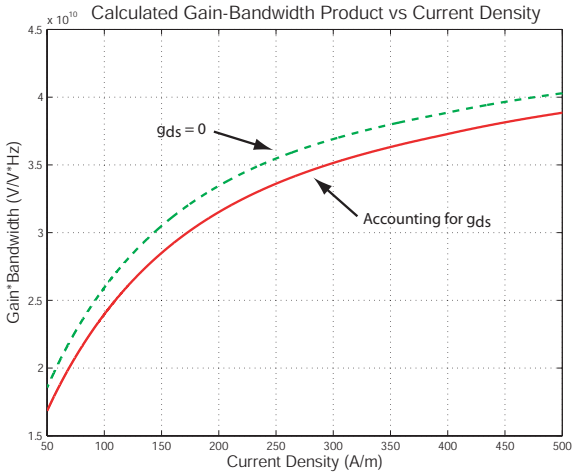

Fig. 3. Calculated Gain-Bandwidth product vs I_{den}.

this observation with Figure 3, we see that higher gains lead to reduced gain-bandwidth products.

Note that the impact of finite output conductance, $g_{ds0}(I_{den})$, is to add to the straight line whose slope is $2|A_v|/V_{sw}$, which leads to further reduction of the resulting current density setting. Therefore, finite output conductance degrades the achievable gain-bandwidth product of the differential amplifier structure.

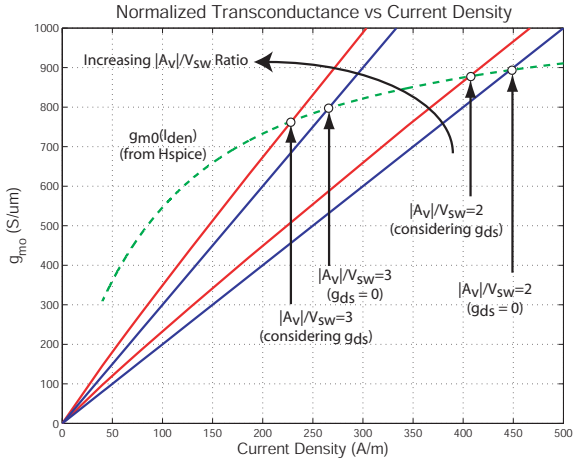

Fig. 4. Current density settings versus gain/swing.

5. RESULTS

The proposed procedure was used to design several differential amplifiers in a 0.18u CMOS process (only NMOS devices were used) with varying gain values. The swing and power dissipation were held constant at $V_{sw} = 1$V and $I_{bias} = 2$mA, respectively, and the bandwidth was calcu-

lated based on Equation 6. Table 1 displays a comparison of the calculated gain and bandwidth values to the Hspice simulation results. In the Hspice simulation, the amplifier has the same topology as shown in Figure 1 and is loaded by an identical amplifier stage whose output is set to a constant voltage in order to eliminate Miller effect on the capacitive load it presents.

Target Gain	Calculated BW (GHz)	Simulated Gain	Simulated BW (GHz)
2.00	14.45	2.03	13.74
3.00	8.30	3.02	8.17
4.00	5.18	4.00	5.31
5.00	3.27	4.98	3.48
6.00	1.99	5.97	2.19

Table 1. Calculated vs simulated amplifier performance.

Table 1 reveals that the proposed design procedure is quite accurate with respect to achieving the desired gain for the amplifier. The calculated versus simulated bandwidth values are not as accurate, but are still within $\pm$ 10 % of each other. The discrepancy in bandwidth is likely due to the fact that the capacitive load is not strictly a linear function of W as assumed in Equation 5.

6. APPLICATION TO SCL DIGITAL CIRCUITS

It is interesting to note that high speed digital structures also make use of such differential amplifier structures. Figure 5 illustrates a high speed SCL latch and a NAND/AND gate. The differential amplifiers embedded in such structures are turned on or off based on other differential pairs below them. When turned on, their behavior corresponds to that of the basic differential amplifier structure.

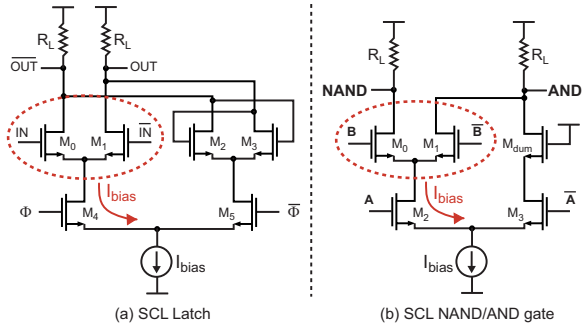

Fig. 5. Digital high speed circuits.

We have found that the following heuristic design method works well for such circuit structures:

1. Use the proposed method to design the differential amplifier portion of the structure with given gain, swing, and bias current requirements. We have found that a choice of gain in the range of 1.25 to 1.75 works well (the swing and bias current values depend on the application). In the latch example of Figure 5 (a), this step yields sizes for M_0 and M_1.

2. Choose identical sizes for transistors that feed off the same diff pair as the differential amplifier above. In the latch example, this would lead to M_2 and M_3 having the same sizes as M_0 and M_1.

3. Choose sizes that are roughly 20 % larger for the transistors that feed the above differential pairs. In the latch example, the widths of M_4 and M_5 would then be set to be 20% higher than the widths of M_0 and M_1 (L should be minimum in all cases). Note that this progressive scaling technique is commonly applied in digital design (see page 298 of [3]) — the value of 20% is not necessarily optimal but has worked well for us in practice.

7. CONCLUSIONS

This paper presented a simple numerical technique to design high speed differential amplifiers with resistor loads without relying on square law assumptions for the CMOS devices. By combining hand analysis with SPICE generated data, intuition of such issues as gain-bandwidth product properties is achieved while still obtaining highly accurate design calculations. Calculations from the method were compared to Hspice simulations, and reveal that the formulations are highly accurate with respect to achieving desired gain, and reasonably accurate for bandwidth estimation. A heuristic extension of the method can be applied to high speed SCL logic gates and latches.

8. REFERENCES

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