A Clockless, Multi-Stable, CMOS Analog Circuit

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***Abstract*— A CMOS analog circuit topology is presented that provides a number of stable operating points based on a laddered inverter quantizer (LIQAF) circuit. An input voltage sets the initial voltage state value when a CMOS transmission gate is turned on, and the voltage state then settles to the nearest stable operating point once the CMOS transmission gate is turned off. The proposed analog circuit achieves its stable operating levels through nonlinear, continuous-time feedback with a circuit that requires only a single supply voltage. An IC prototype demonstrates a 10-level version of the multi-stable circuit with an area of 0.015mm^2 in 0.18µm CMOS and current consumption of 300µA at 1.4V and <45µA at 1V supply for a pair of the multi-stable circuits.**

Keywords*— laddered inverter , LIQAF, multi-stable analog circuit, static analog memory, nonlinear analog circuit, analog neural network, DAC trimming circuit, quantizer, storage element

I. INTRODUCTION

Multi-stable analog circuits have been a topic of interest as a means of better understanding biological systems [1] and for storing parameter values within analog neural networks and fuzzy systems [2]. In addition, such circuits could also be useful for analog trimming of current sources for digital-to-analog converters (DACs) [3] and charge pumps used within analog phase-locked loop (PLL) circuits.

A variety of such "analog memory" circuits have been reported in the literature [4-8], with a common approach being the storage of charge on a capacitor through a sample-and-hold circuit [9] as shown in Figure 1(a). Unfortunately, charge leakage in such systems leads to very limited hold times of a given voltage state. Refresh techniques, which require a clock signal, have been suggested in [7] and [8] to increase the hold time of the charge on a capacitor, but involve significant design efforts in maintaining the charge value with low error. Alternatively, an analog-to-digital converter (ADC) and digital-to-analog converter (DAC) are combined to achieve indefinite hold times [2] as shown in Figure 1(b), but multiple current branches are utilized for the ADC which leads to increased current consumption. A clockless, multi-stable, CMOS analog circuit [4], as shown in Figure 1(c), achieves a relatively simple implementation, but requires multiple reference voltages.

Similar to the approach in [4], the "analog memory" circuit presented in this paper utilizes a nonlinear analog circuit to achieve multiple stable operating points. However, rather than using inverters in combination with multiple reference voltages as shown in Figure 1(c), a recently introduced Laddered Inverter Quantizer/Amplifier/Filter (LIQAF) circuit [10], [11] is employed that operates using only a single supply voltage. The LIQAF circuit is combined with a transmission gate and nonlinear feedback structure similar to [4] in order to achieve the desired multi-stable behavior. Overall, the proposed structure requires four more transistors than [4] to achieve four levels (as shown in Figure 1(c)), but has the same incremental cost as [4] in that it requires four transistors for each additional level. The proposed design offers advantages of allowing low voltage operation and simplified wiring complexity since multiple reference voltages are not required.

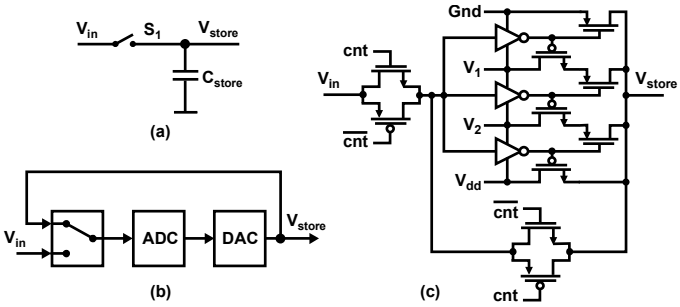

Fig. 1 Previous analog memory circuits: (a) storing charge on a capacitor with a sample-and-hold circuit, (b) combining an ADC and DAC, (c) utilizing a multi-stable analog circuit [4].

The reminder of this paper is organized as follows. Section II provides an overview of the LIQAF circuit. Section III presents the proposed multi-stable analog circuit. Section IV presents the measured results of the prototype IC. Finally, Section V concludes.

II. LIQAF CIRCUIT

To gain an understanding of the LIQAF circuit, consider the simplified structure shown in Figure 2 in which only two-output levels are implemented. As indicated in Figure 2, we can view this circuit as a combination of two CMOS inverters that have different ratios of NMOS versus PMOS gate lengths, which yields the shifted DC characteristics shown in the figure. To explain, note that when V_{in} is low and both outputs are high, transistor M_1 is inactive such that V_{out1} transitions with increasing V_{in} according to a CMOS inverter characteristic with one NMOS device and two series PMOS devices. In contrast, when V_{in} is high and both outputs are low, M_2 is inactive such that V_{out2} transitions with decreasing V_{in} according to a CMOS inverter characteristic with two series NMOS devices and one PMOS device. Since V_{out1} cannot transition high unless V_{out2} is also high, and V_{out2} cannot transition low unless V_{out1} is also low, the LIQAF circuit provides guaranteed monotonicity in the quantizer characteristic regardless of the presence of mismatch. Note that one should not confuse the curves shown in Figure 2 with the

phenomenon of hysteresis — they instead correspond to the DC characteristic of the structure that is independent of the previous state of the input.

The number of LIQAF outputs can be readily increased, as depicted in Figure 3 for a ten-output example. As shown in the figure, SPICE simulations indicate robust operation of the LIQAF circuit across a wide range of supply voltages.

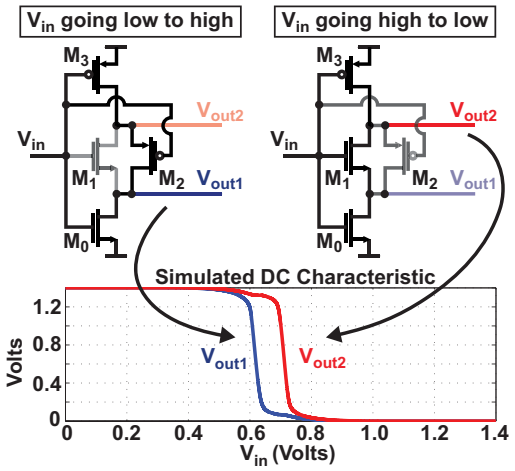

Fig. 2 Basic principles of a two-output LIQAF circuit.

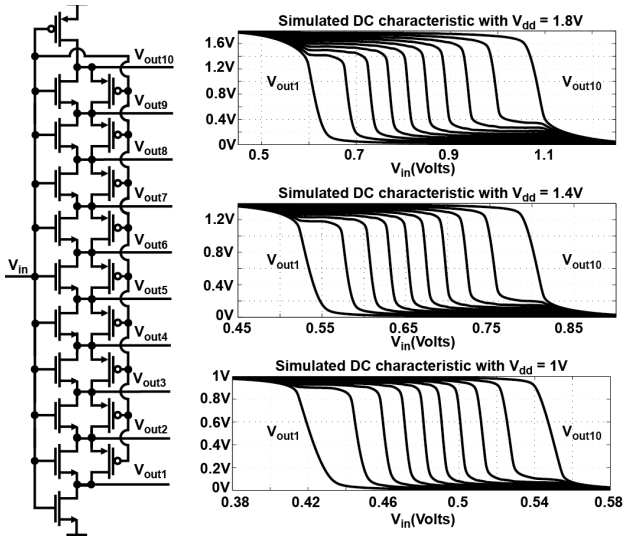

Fig. 3 Ten-output LIQAF circuit along with its simulated DC characteristic with supply voltages of 1V, 1.4V, and 1.8V.

III. Proposed Multi-Stable Analog Circuit

To explain the key operating principles of the proposed multi-stable analog circuit, we begin with a 2-level version based on the two-output LIQAF circuit shown in Figure 2. As shown in Figure 4(a), the LIQAF circuit is augmented with a transmission gate and nonlinear feedback attached to each output. Setting *cnt* to be high turns on the transmission gate such that $V_q(t)$ is set by $V_{in}(t)$, and setting *cnt* to be low turns off the transmission gate such that the nonlinear feedback causes $V_q(t)$ to settle to the nearest stable operating point. Similar to [4], nonlinear feedback is achieved by connecting an NMOS and PMOS device in series from each LIQAF output to the input, with the gates of these devices being driven by neighboring LIQAF outputs. Since the series NMOS and PMOS devices turn on with a logic 1 and 0 level, respectively, the LIQAF quantizer characteristic is leveraged to enable the appropriate feedback connection to achieve the multi-stable operating point characteristic. To demonstrate the operation of the circuit, Figure 4(b) displays its SPICE simulated transient response, which reveals that two stable operating points are achieved. Note that the asymmetry in settling time is due to the fact that the output impedance at node $V_q(t)$ decreases at higher voltage values.

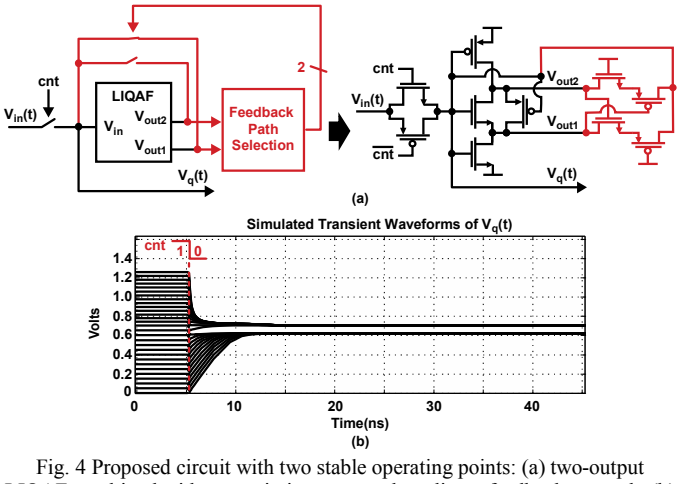

Fig. 4 Proposed circuit with two stable operating points: (a) two-output LIQAF combined with transmissiont gate and nonlinear feedback network, (b) SPICE simulated response demonstrating two steady-state operating points.

The number of stable operating points of the proposed multi-stable circuit is increased by using a LIQAF circuit with a greater number of outputs. As shown in Figure 5, ten stable operating points are achieved in the prototype circuit by using a ten-output LIQAF, as was shown in Figure 3, and correspondingly extending the nonlinear feedback circuit. Note that increasing the number of stable operating points does not lead to a proportional increase in current since all of the devices share the same current. In practice, the circuit will typically encounter some amount of load resistance, such as the input impedance of the test instrument used to measure the voltage state of the circuit as indicated in Figure 5. Fortunately, the nonlinear feedback accommodates such resistive loading so long as the load resistance is reasonably high in value, though the value of the load resistance will have an impact on the operational voltage supply range of the circuit. Overall, one should note the relative simplicity of the proposed circuit in achieving multi-stable operating point behavior.

Figure 5 indicates relatively large device widths being used within the circuit, which were chosen in order to facilitate easy testing of the device since the larger widths allow for less impact from the loading effect of the test instrument. SPICE simulations indicate functionality of the 10-level circuit at near minimum device widths, so that area and power could likely be significantly reduced compared to the prototype circuit presented in this paper. Also, the LIQAF circuit can be potentially expanded beyond ten outputs in order to increase the number of stable operating points.

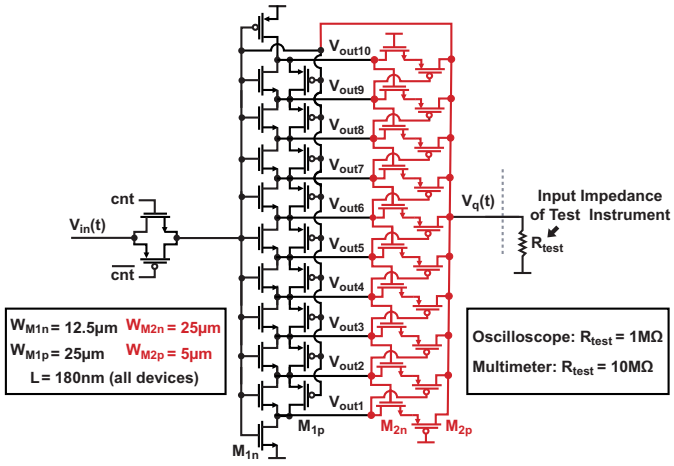

Fig. 5 Prototype circuit with ten stable operating points.

IV. MEASURED RESULTS

The prototype multi-stable circuit shown in Figure 5 was fabricated in a 180nm CMOS process and has an area of 0.015mm^2 as indicated in the die photo shown in Figure 6. Operation of the circuit was confirmed over a 1.3V to 1.8V supply range in the presence of the oscilloscope 1MΩ load resistance, and over a 1.0V to 1.5V supply range in the presence of the multimeter 10MΩ load resistance. Beyond these voltage ranges, the primary mode of failure of the circuit is to lose stability points at the ends of its range, as will be discussed later. For simplicity, most of the measurement results will be shown using a supply voltage of 1.4V, which is the mid-point between the 1.3V to 1.5V operational range for both load resistance cases.

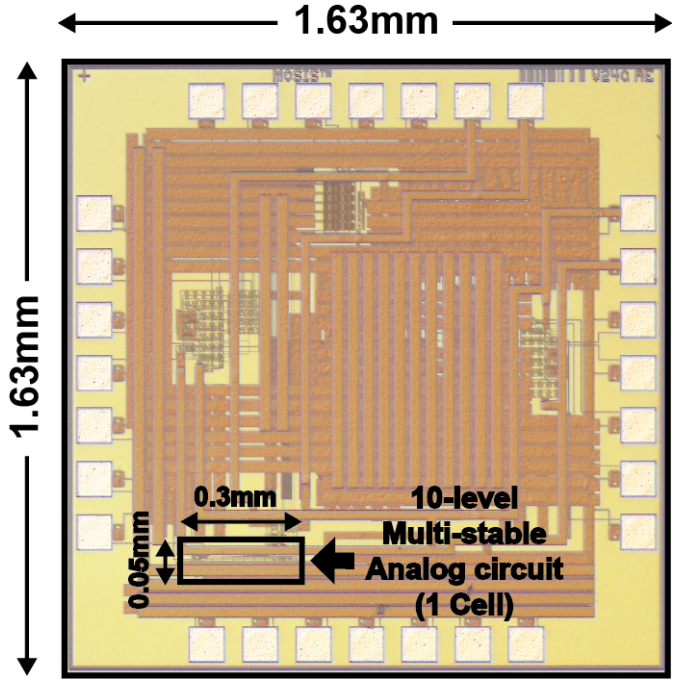

Fig. 6 Die photo of the prototype IC implementing the multi-stable analog circuit shown in Figure 5.

Figure 7 shows the measured DC characteristic at each of the LIQAF outputs (i.e. V_{out1} to V_{out10}) for the circuit shown in Figure 5 assuming 1.4V supply voltage. These measurements were performed by utilizing switches, which are not shown for simplicity, that individually connect each LIQAF output to a test pin on the prototype IC. The results shown in Figure 7 confirm the quantization behavior of the LIQAF circuit despite the presence of loading from the nonlinear feedback network.

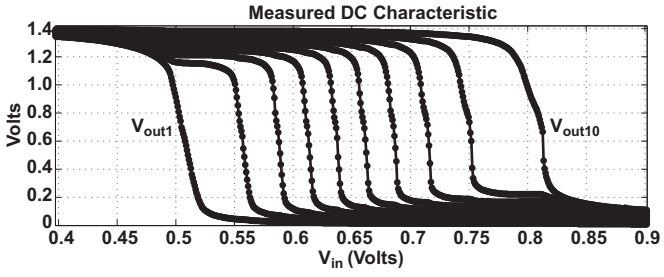

Fig. 7 Measured DC characteristic of the ten-output LIQAF circuit shown in Figure 5.

Figure 8 shows measured transient waveforms of node $V_q(t)$ for the overall multi-stable circuit shown in Figure 5 assuming 1.4V supply voltage and oscilloscope loading of 1MΩ. This figure confirms settling to the nearest stable operating point as the transmission gate is turned off. Note that the input voltage is swept from 0 to 1.4V in Figure 5, but the output is limited to a maximum value of 1.3V due to contention between the nonlinear feedback and the transmission gate.

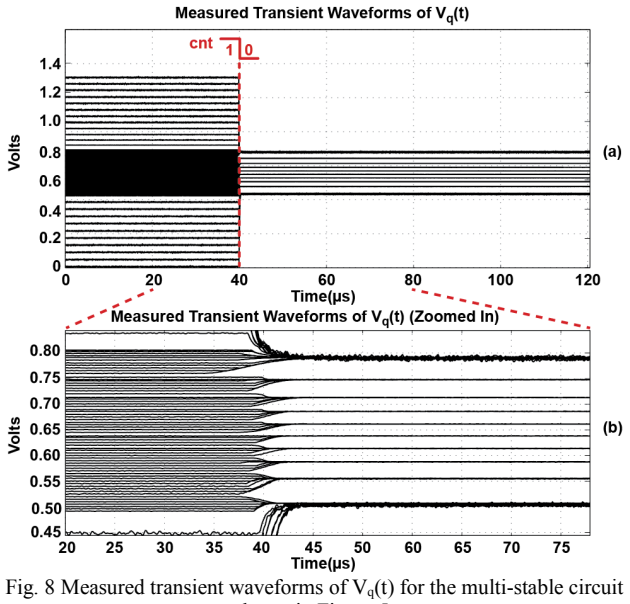

Fig. 8 Measured transient waveforms of $V_q(t)$ for the multi-stable circuit shown in Figure 5.

Figure 9 shows the measured DC characteristics of the multi-stable analog circuit shown in Figure 5 for three values of supply voltage assuming multimeter loading of 10MΩ. At a supply voltage of 1.8V, we see the soft nature of failure when operating beyond the valid supply range, which is the loss of the top/bottom stability points (i.e., V_{out1} and V_{out10}) in being active. In this case, there is one missing level corresponding to

V_{out1}. All levels are active for the valid supply range of 1V to 1.5V, with the preferred voltage being 1V to reduce the power consumption.

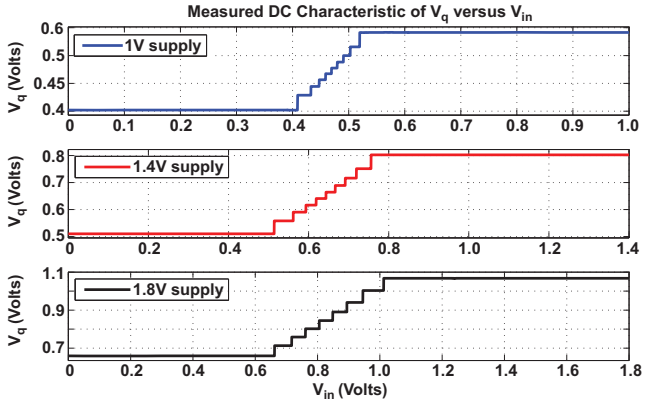

Fig. 9 Measured DC characteristics from the custom IC.

Figure 10 shows the power consumption of two identical multi-stable circuits connected in parallel at supply voltages of 1V, 1.4V, and 1.8V. Here the power consumption was measured at three stability points corresponding to the bottom, middle, and top levels.

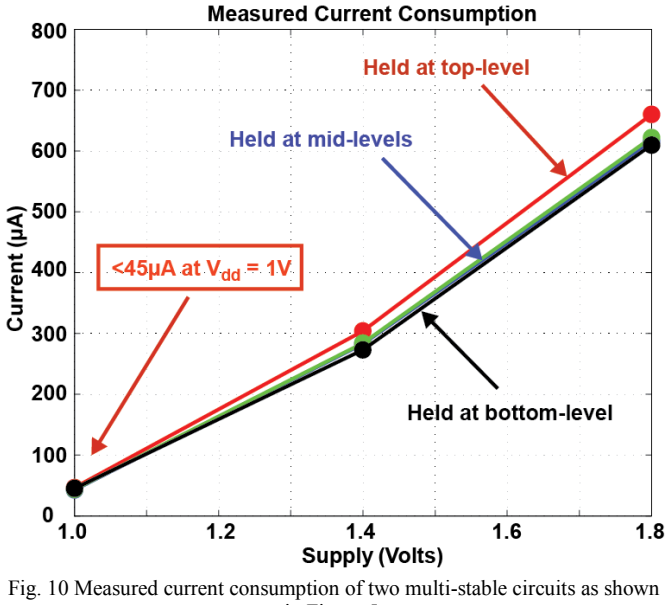

Fig. 10 Measured current consumption of two multi-stable circuits as shown in Figure 5.

V. Conclusions

This paper presented a multi-stable analog CMOS circuit that is achieved by combining a LIQAF circuit with a transmission gate and nonlinear feedback within a standard 180nm CMOS process. This approach leads to a relatively simple circuit implementation that requires only a single supply voltage rather than multiple reference voltages. The proposed multi-stable circuit could be useful in setting parameter values in analog neural network and fuzzy logic systems, as well as for analog circuit trimming of current sources for DACs and PLLs.

VI. Acknowledfments

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