A 4th Order Continuous-Time ΔΣ ADC with VCO-Based Integrator and Quantizer

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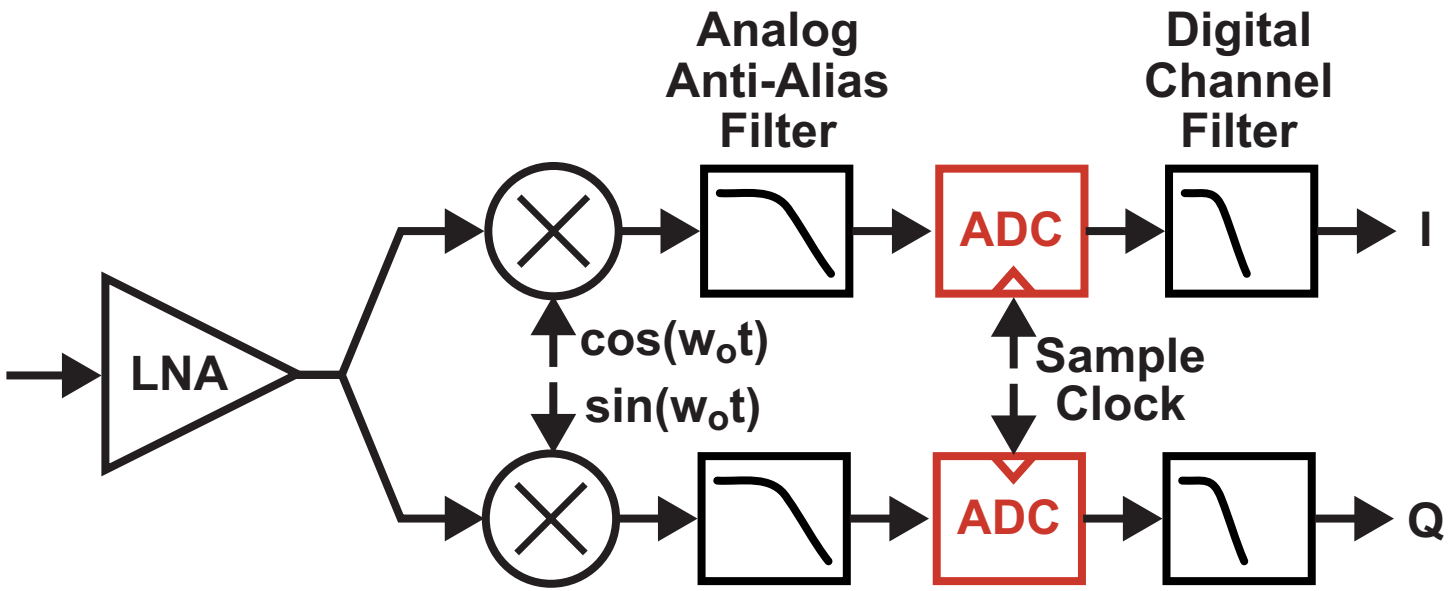
Matt Park[1], Michael H. Perrott[2]

[1] Massachusetts Institute of Technology, Cambridge, MA USA

[2] SiTime Corporation, Sunnyvale, CA, USA

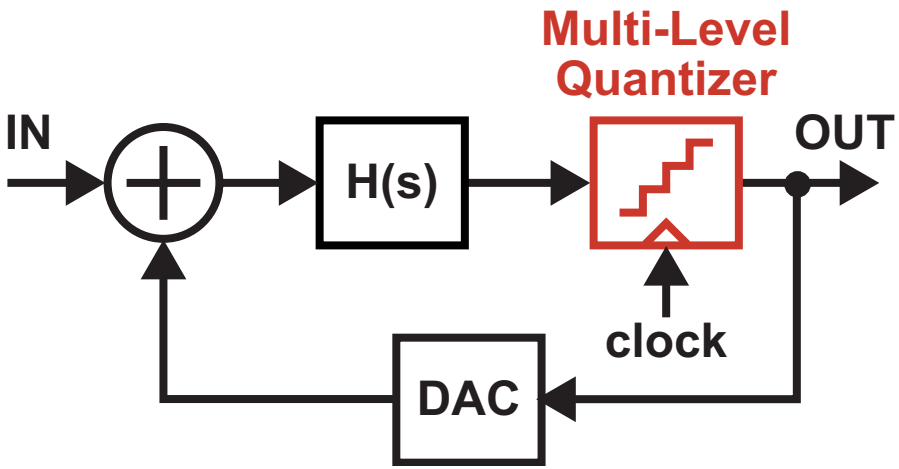
Motivation



- A highly digital receive path is very attractive for achieving multi-standard functionality
- A key issue is achieving a wide bandwidth ADC with high resolution and low power
  - Minimal anti-alias requirements are desirable for simplicity

Continuous-Time Sigma-Delta ADC structures have very attractive characteristics for this space

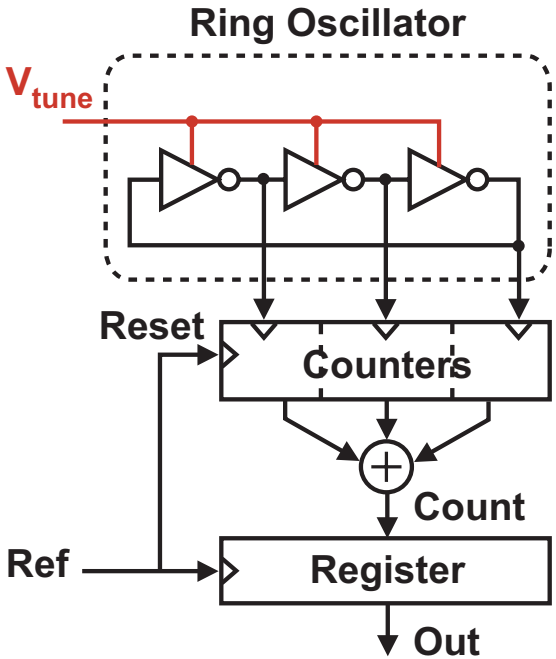
A Basic Continuous-Time Sigma-Delta ADC Structure



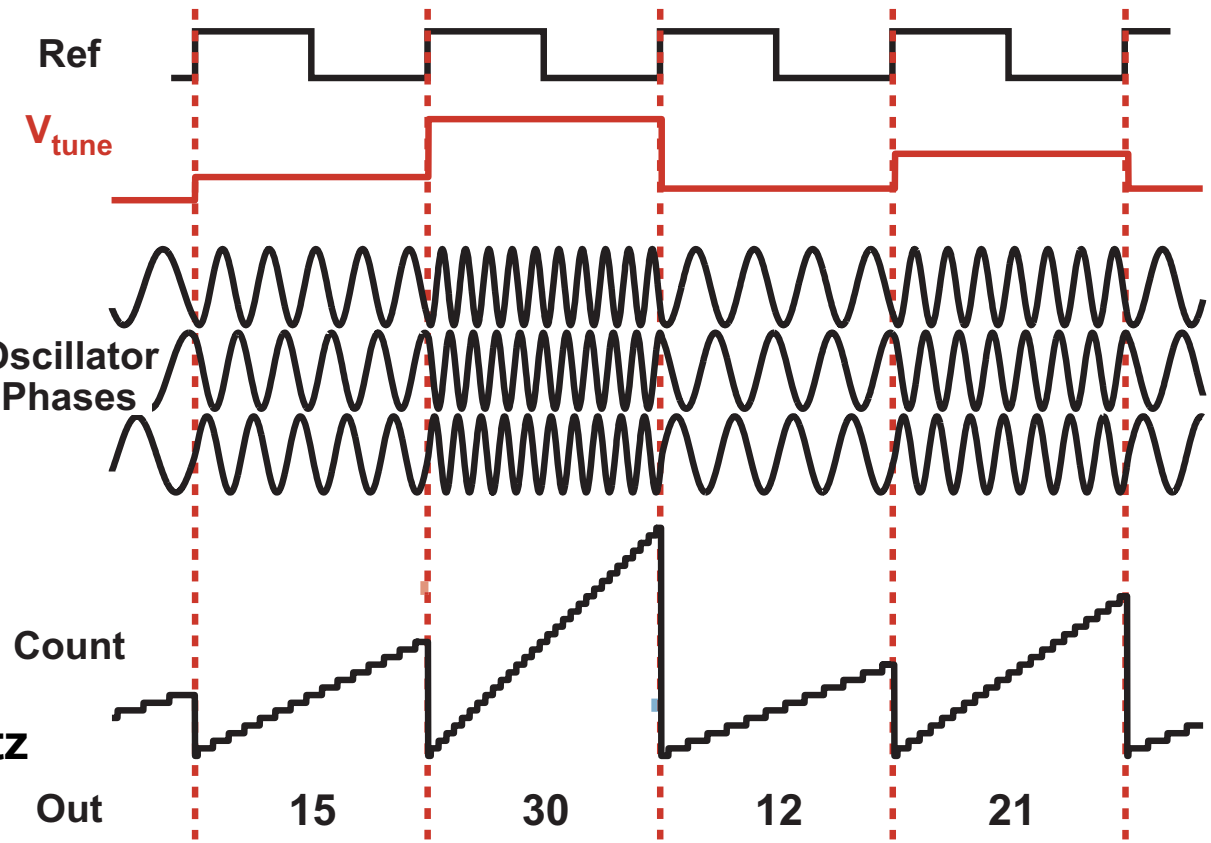
- Sampling occurs at the quantizer *after* filtering by *H(s)*
- Quantizer noise is shaped according to choice of *H(s)*
  - High open loop gain required to achieve high SNR

We will focus on achieving an efficient implementation of the multi-level quantizer by using a ring oscillator

Application of Ring Oscillator as an ADC Quantizer

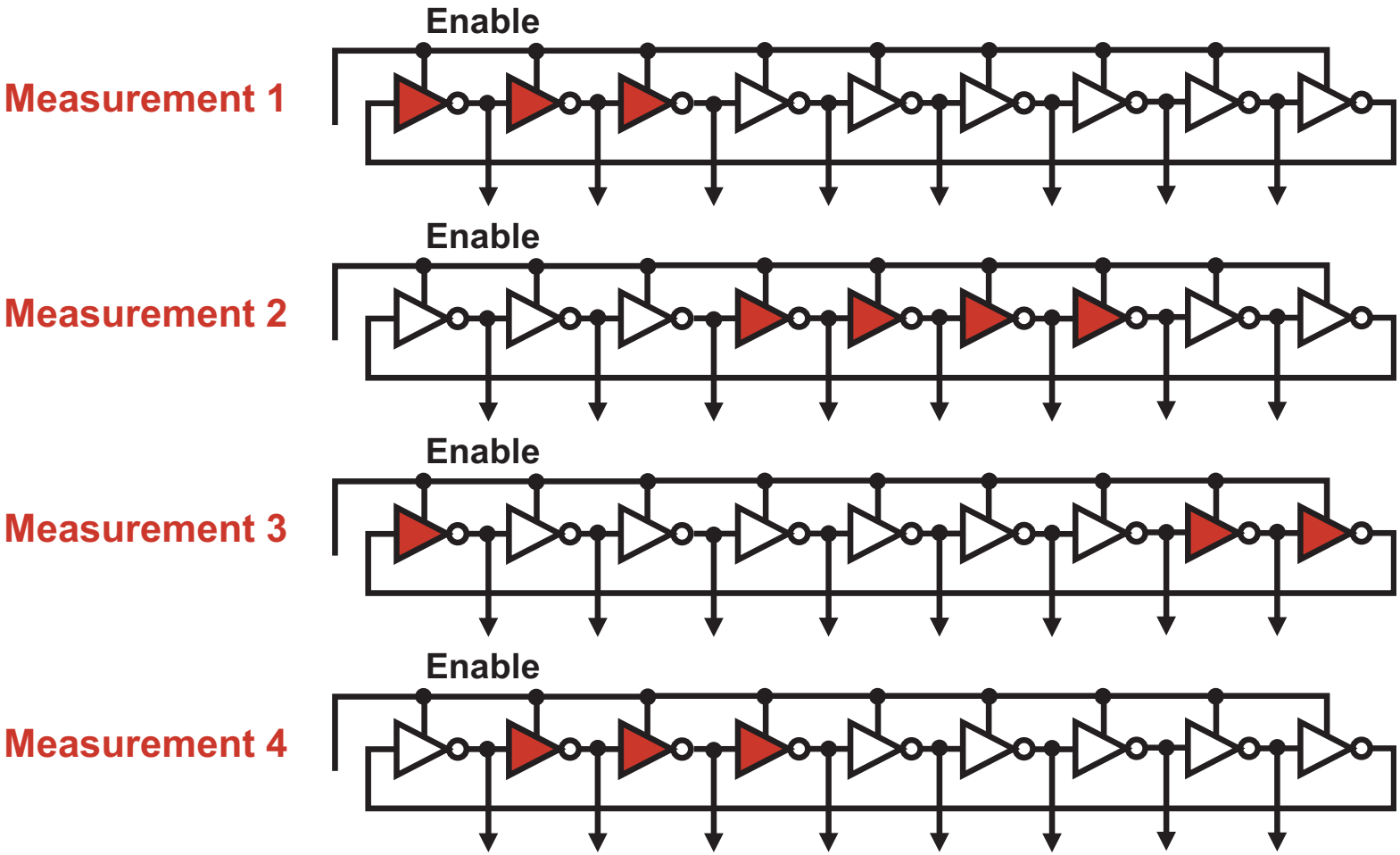


Similar approaches:
Alon, Stojanovic, Horowitz
JSSC 2005
Kim, Cho, ISCAS 2006



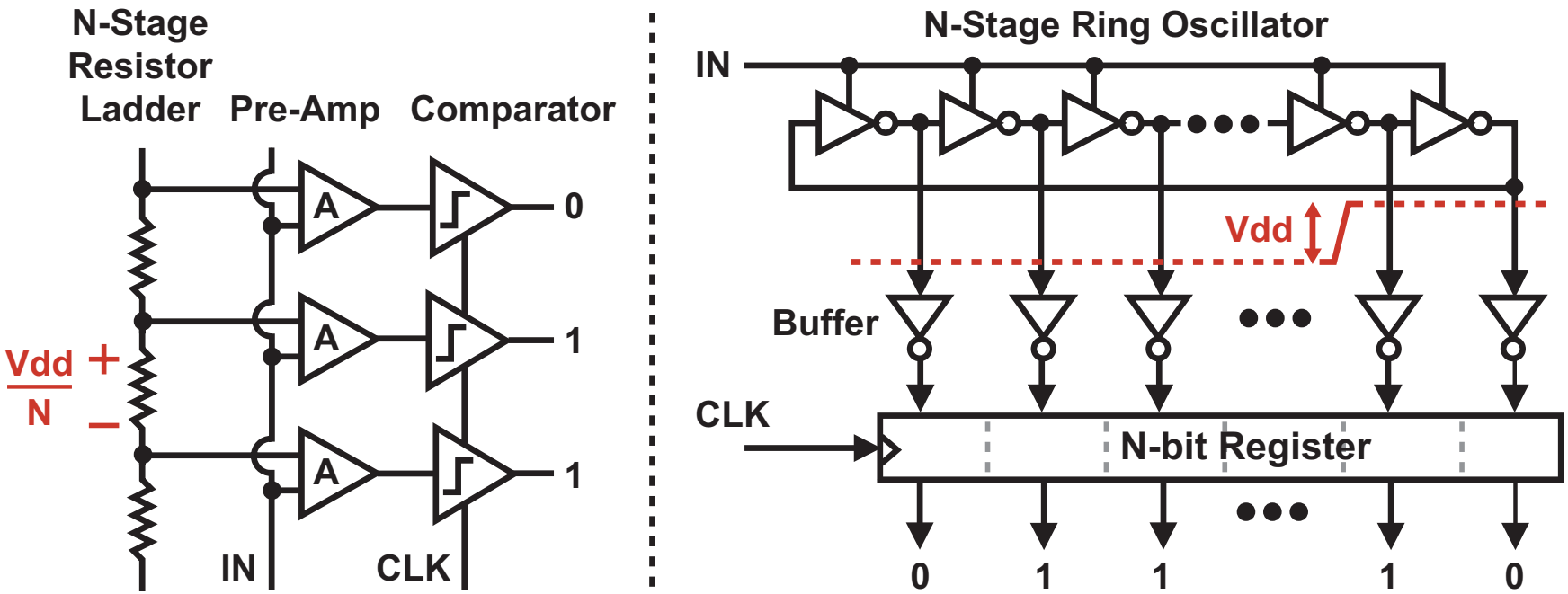
- **Input: analog tuning of ring oscillator frequency**
- **Output: count of oscillator cycles per Ref clock period**

VCO-Based Quantizer Also Shapes Delay Mismatch



- Barrel shifting through delay elements
  - Mismatch between delay elements is first order shaped

Benefits of VCO-based Quantization

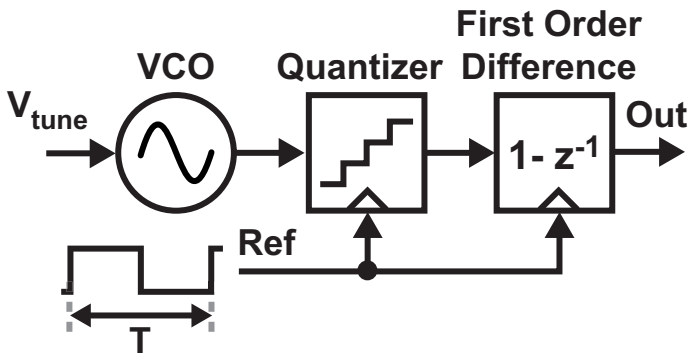


- Much more digital implementation
  - No resistor ladder or differential gain stages
- Offset and mismatch is not of critical concern
- Metastability behavior is improved

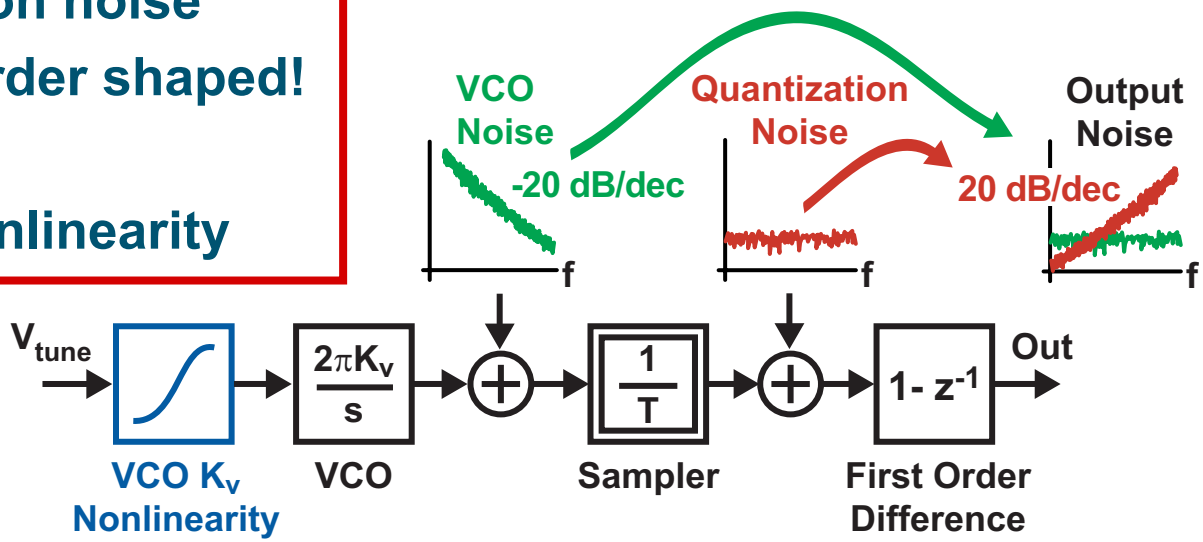
Implementation is high speed, low power, low area

Frequency Domain Model of VCO Quantizer

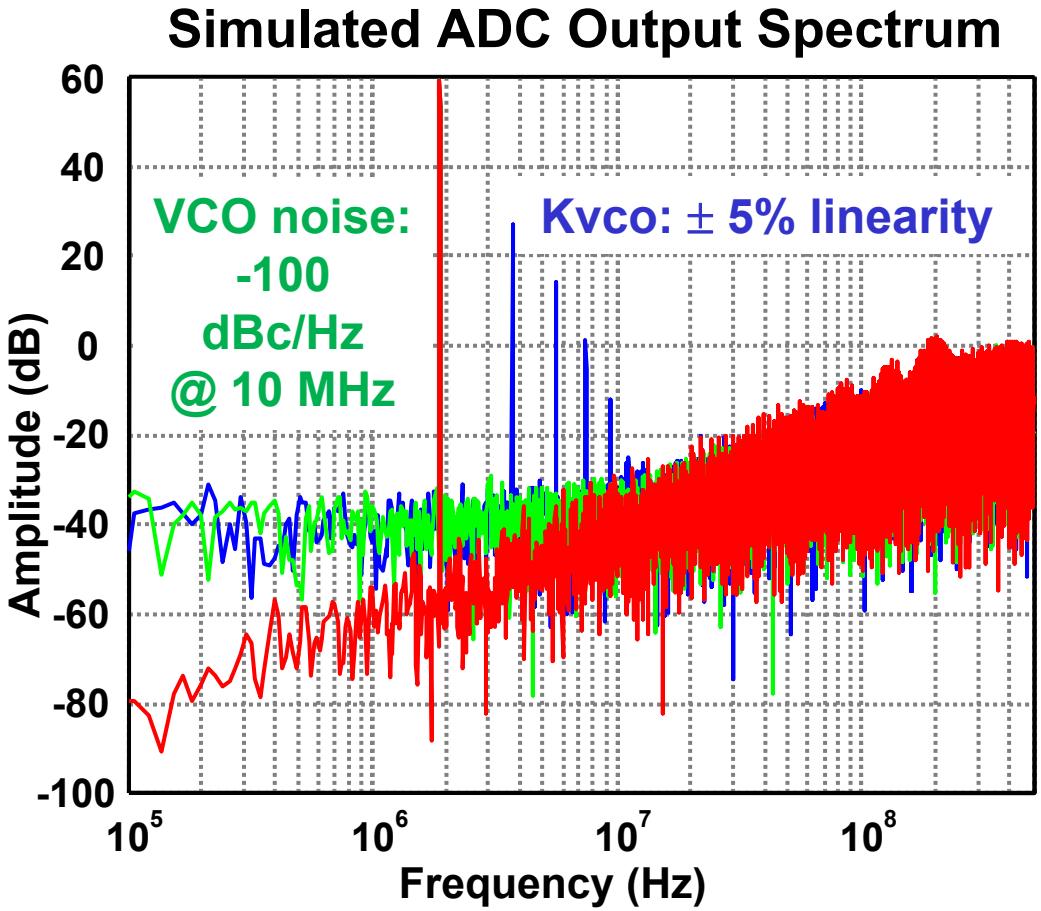
- VCO modeled as integrator and K_v nonlinearity
- Sampling of VCO phase modeled as scale factor of 1/T
- Quantizer modeled as addition of quantization noise



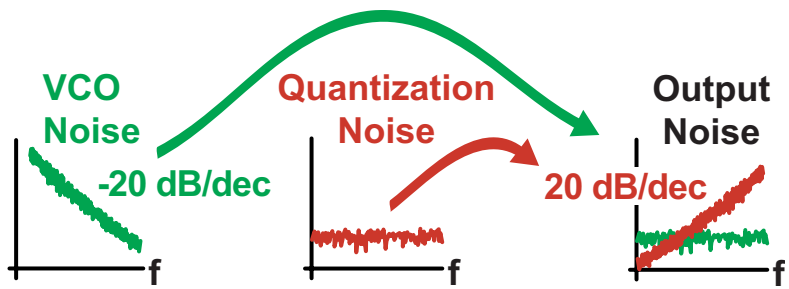
- Key non-idealities:
  - Quantization noise
    - First order shaped!
  - VCO noise
  - VCO K_v nonlinearity



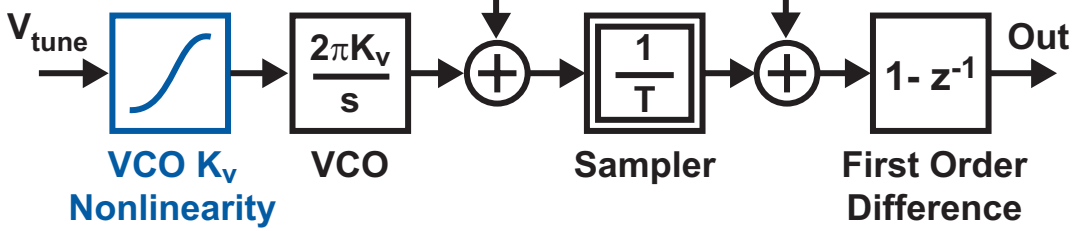
Example SNDR with 20 MHz BW (1 GHz Sample Rate)



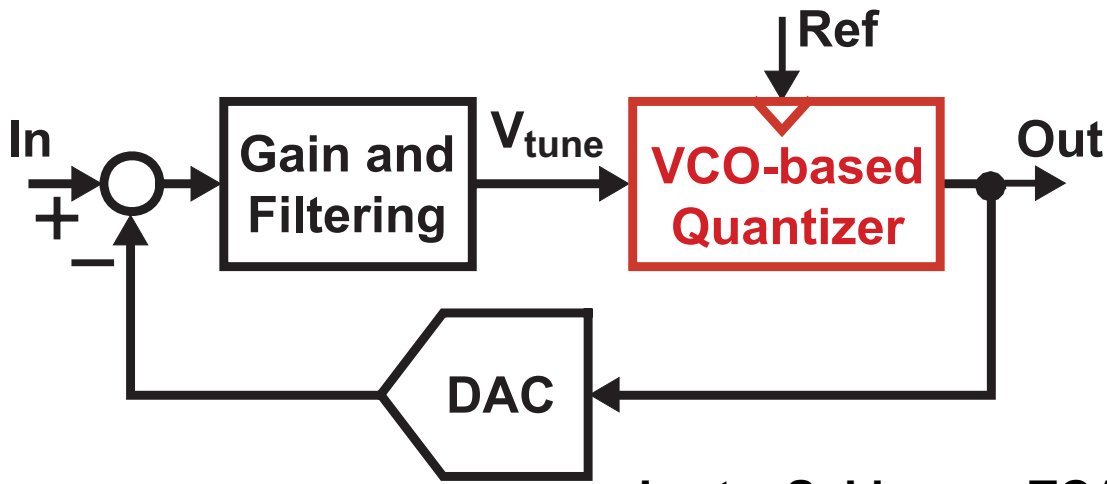
Conditions	SNDR
Ideal	68.2 dB
VCO Thermal Noise	65.4 dB
VCO Thermal + Nonlinearity	32.2 dB



VCO K_v nonlinearity is key SNDR bottleneck



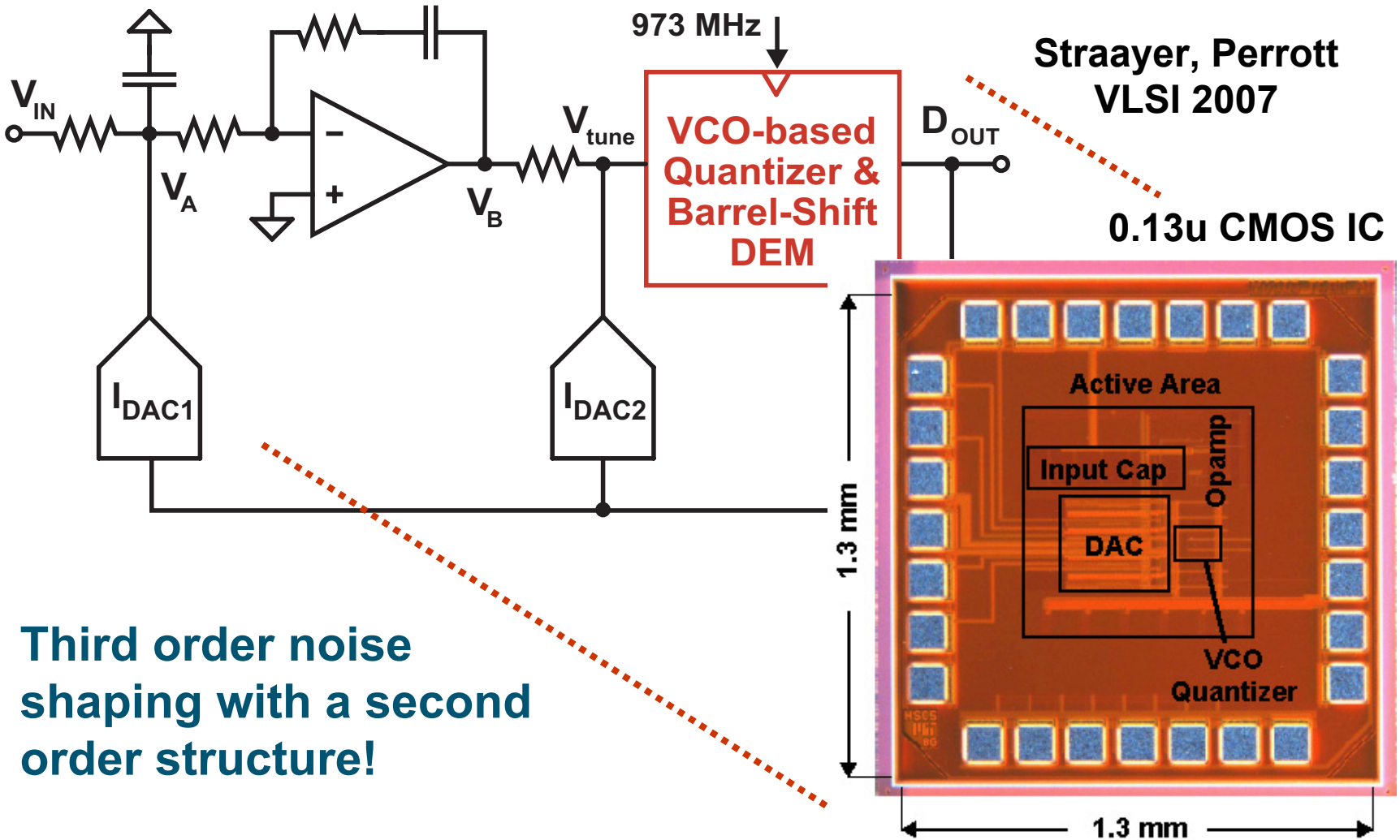
Reducing the Impact of Nonlinearity using Feedback



Iwata, Sakimura, TCAS II, 1999
Naiknaware, Tang, Fiez, TCAS II, 2000

- Place VCO-based quantizer within a continuous-time Sigma-Delta ADC structure
  - Quantizer nonlinearity suppressed by preceding gain stage

A Second Order Continuous-Time Sigma-Delta ADC

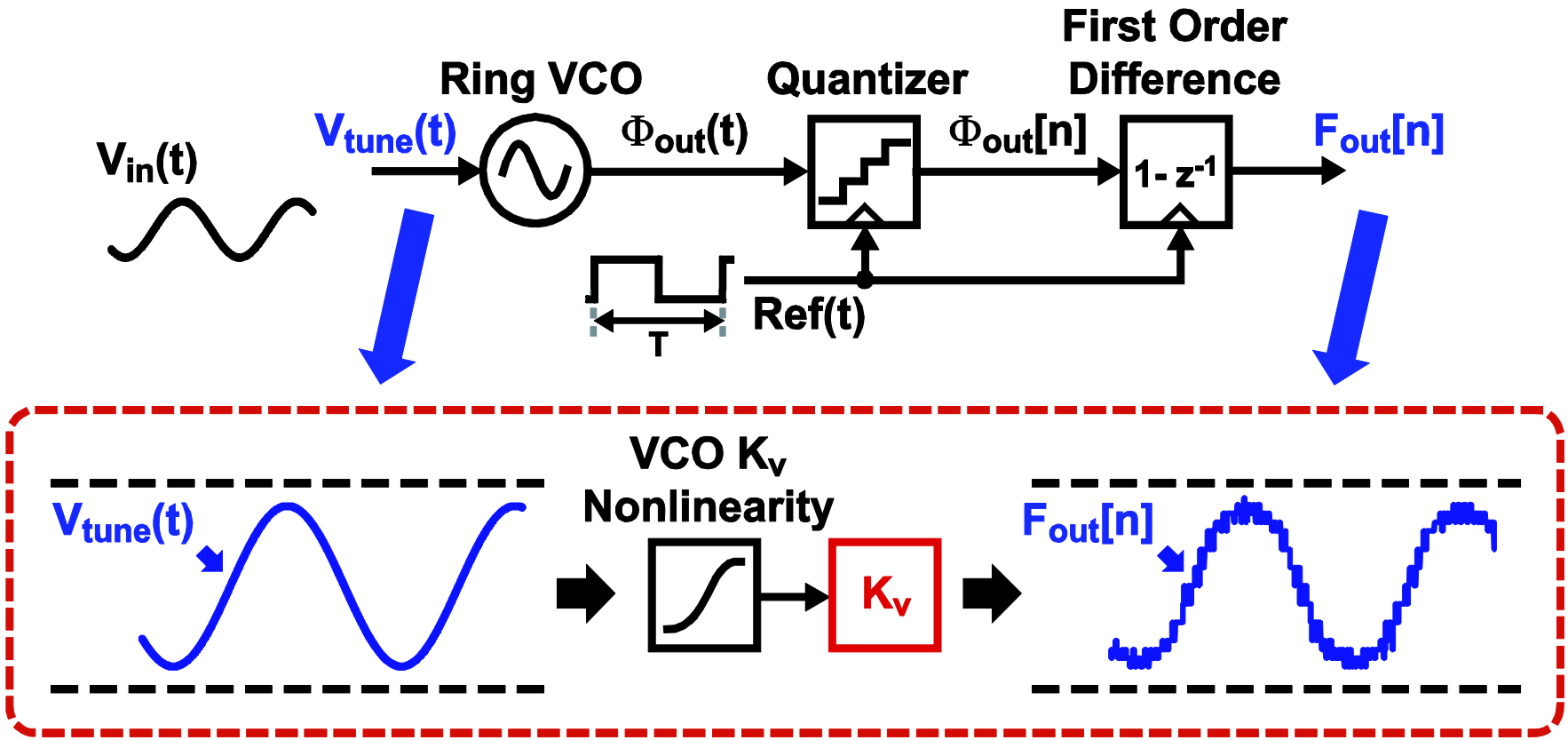


- Third order noise shaping with a second order structure!

Peak SNDR limited by Kv non-linearity to 67 dB (20 MHz BW)

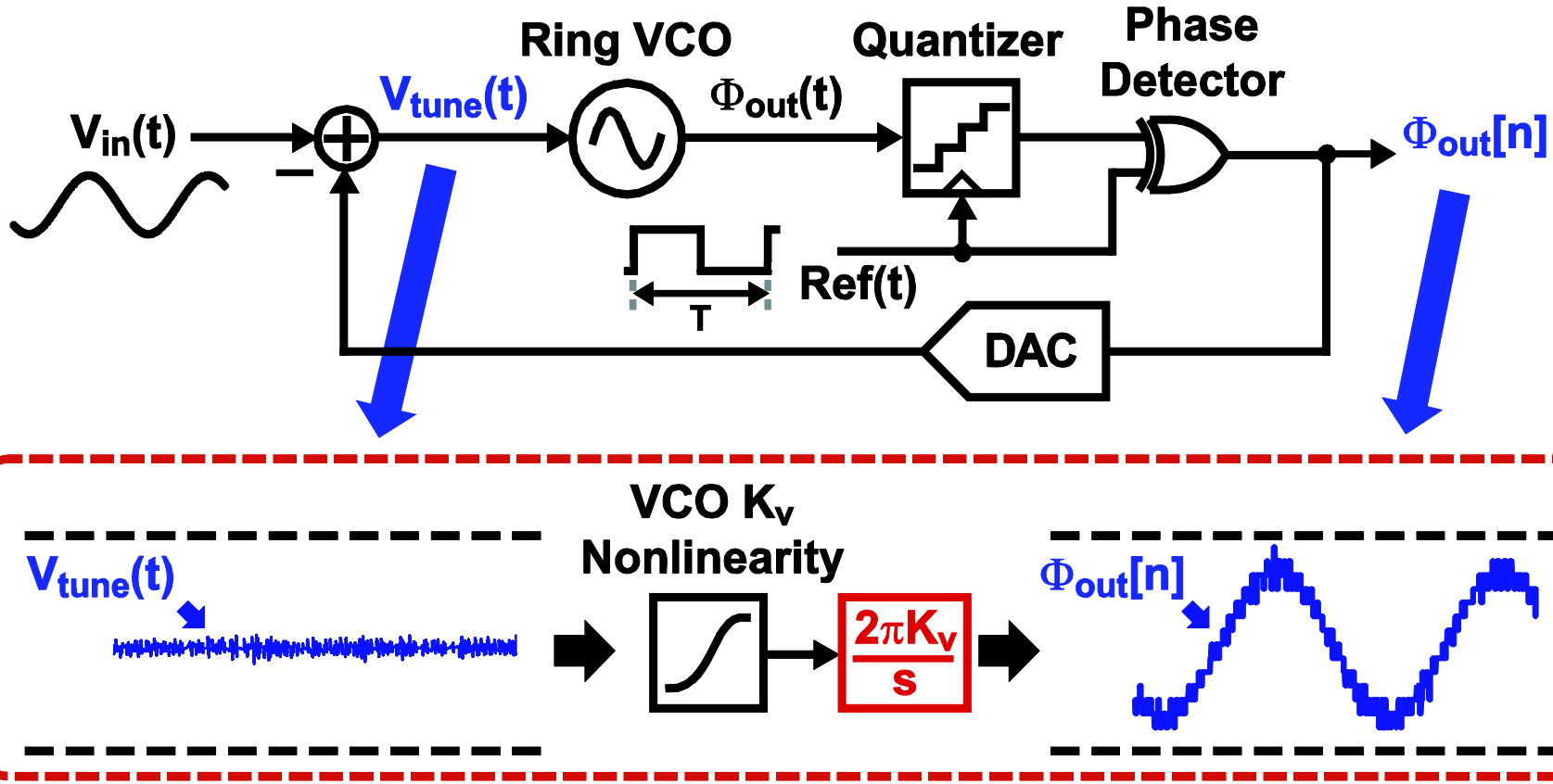
How Do We Overcome K_v Nonlinearity to Improve SNDR?

Voltage-to-Frequency VCO-based ADC (1st Order Σ–Δ)



- In prior work, VCO *frequency* is desired output variable
  - Input must span the entire non-linear voltage-to-frequency (K_v) characteristic to exercise full dynamic range
  - Strong distortion at extreme ends of the Kv curve

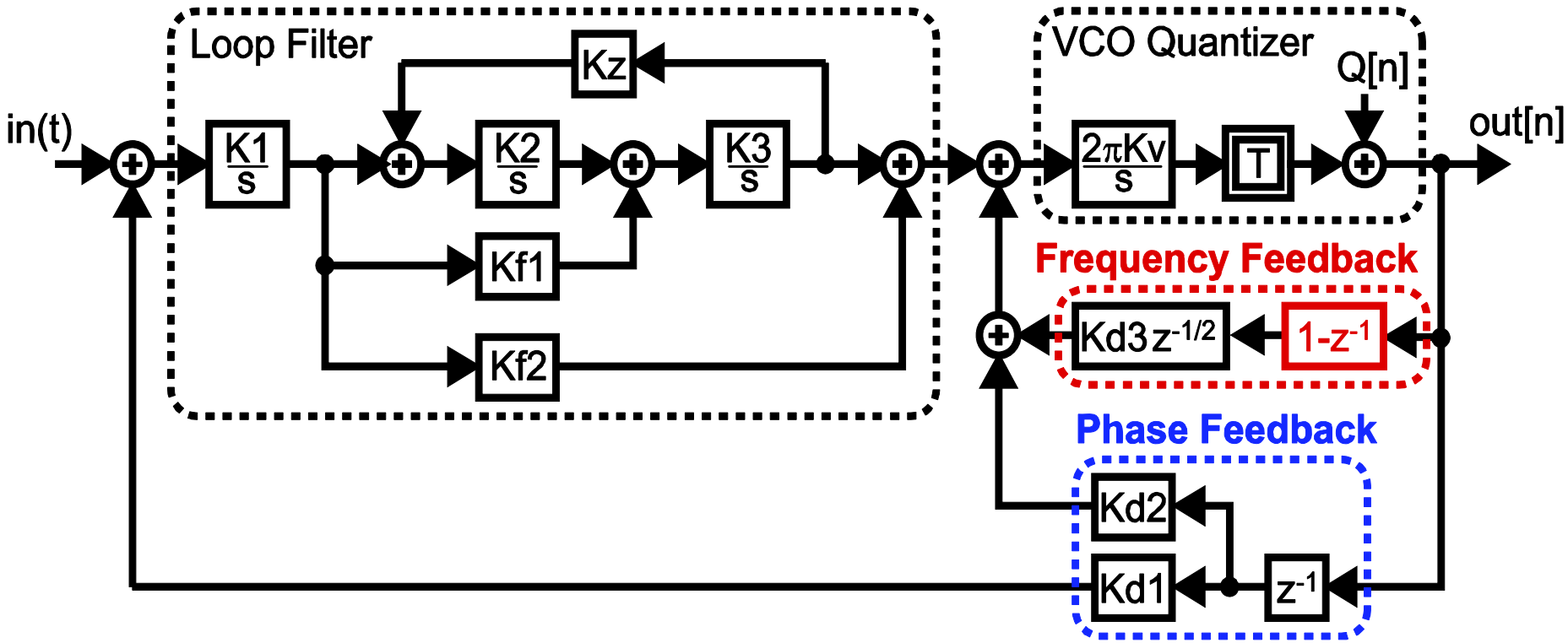
Proposed Voltage-to-Phase Approach (1st Order Σ–Δ)



- VCO output *phase* is now the output variable
  - Small perturbation on V_{tune} allows large VCO phase shift
  - VCO acts as a CT integrator with *infinite* DC gain

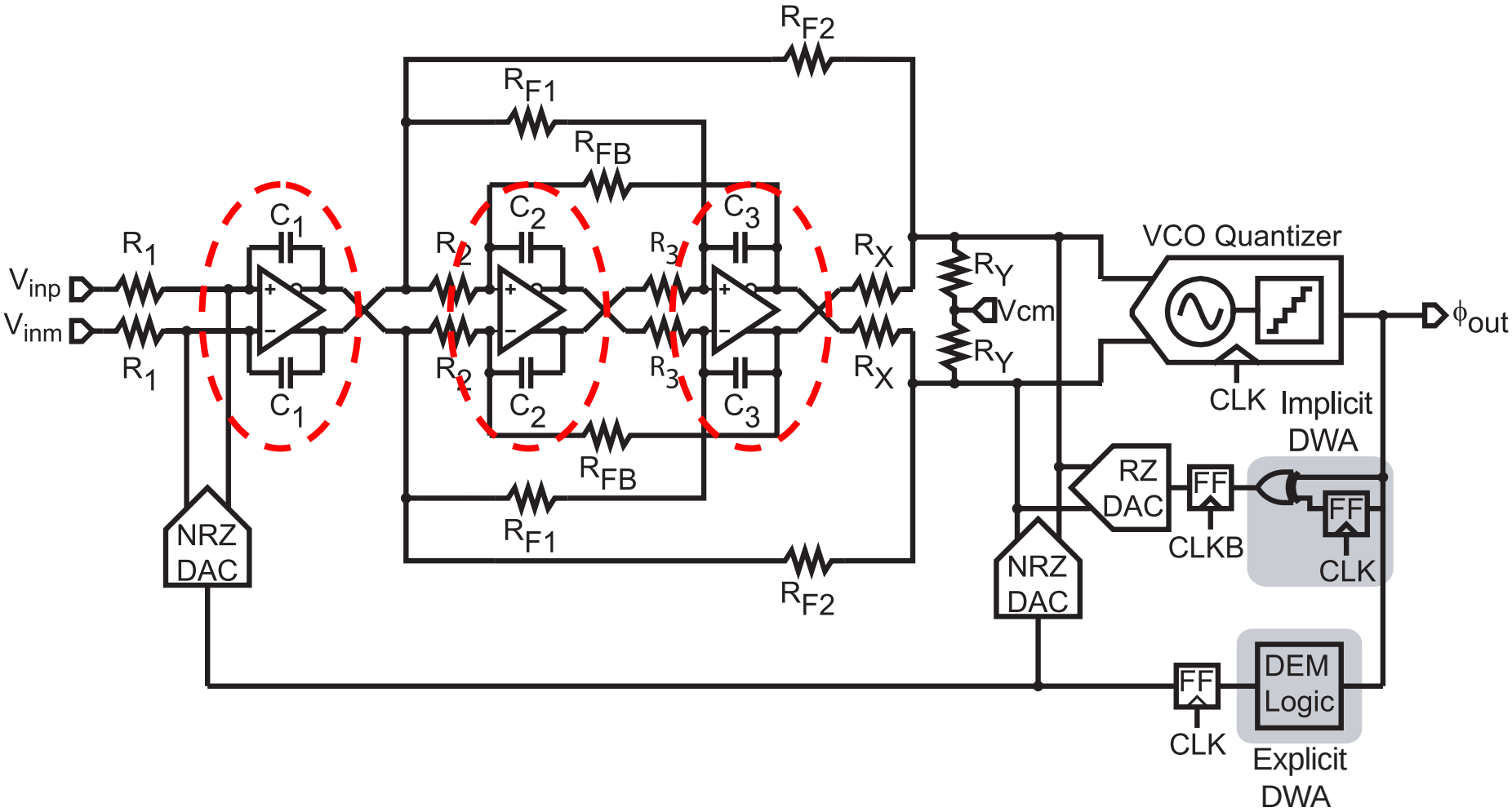
High SNDR requires higher order Σ–Δ …

Proposed 4th Order Architecture for Improved SNDR



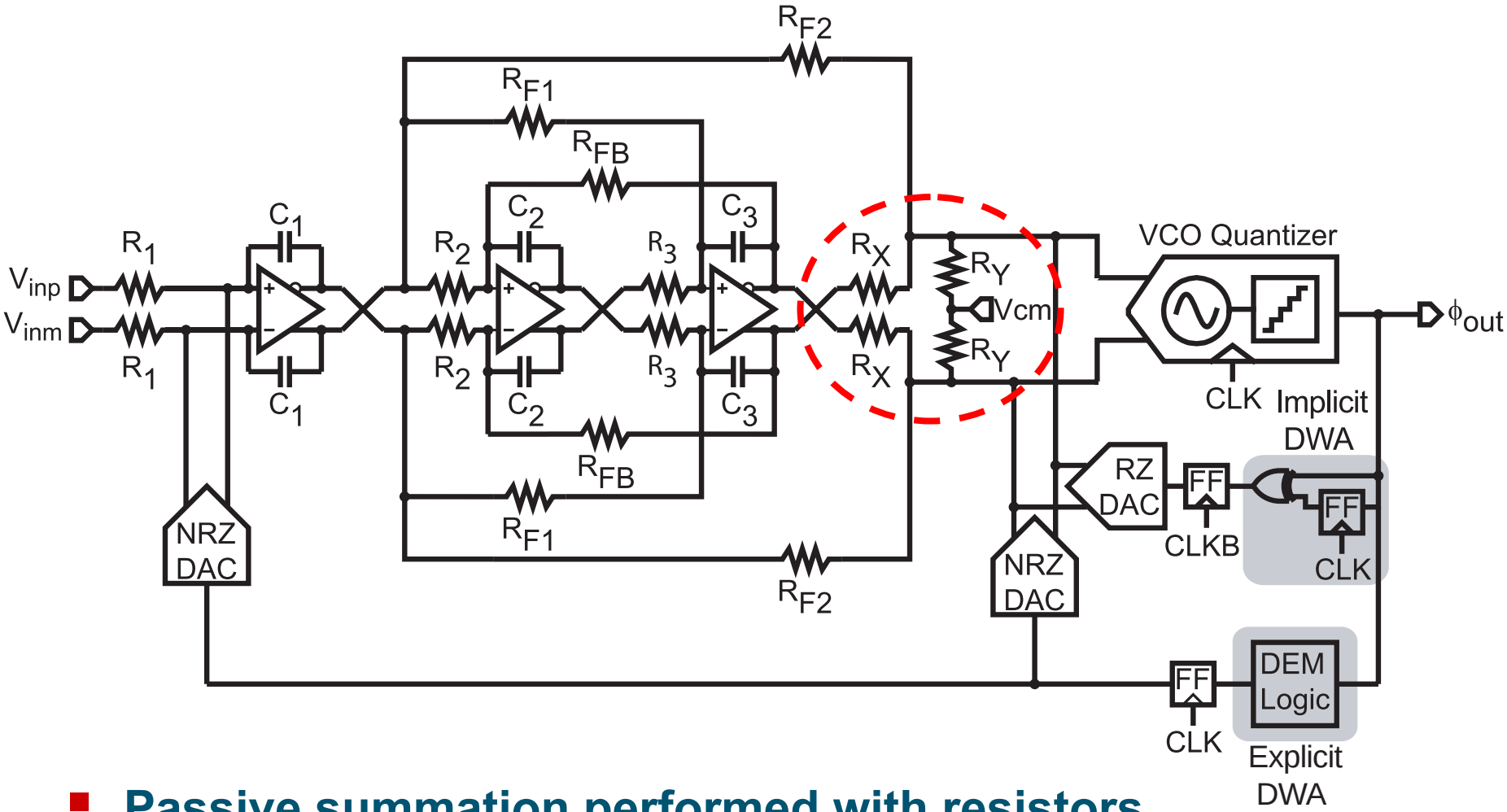
- Goal: ~80 dB SNDR with 20 MHz bandwidth
  - Achievable with 4th order loop filter, 4-bit VCO-based quantizer
  - 4-bit quantizer: tradeoff resolution versus DEM overhead
- Combined frequency/phase feedback for stability/SNDR

Schematic of Proposed Architecture



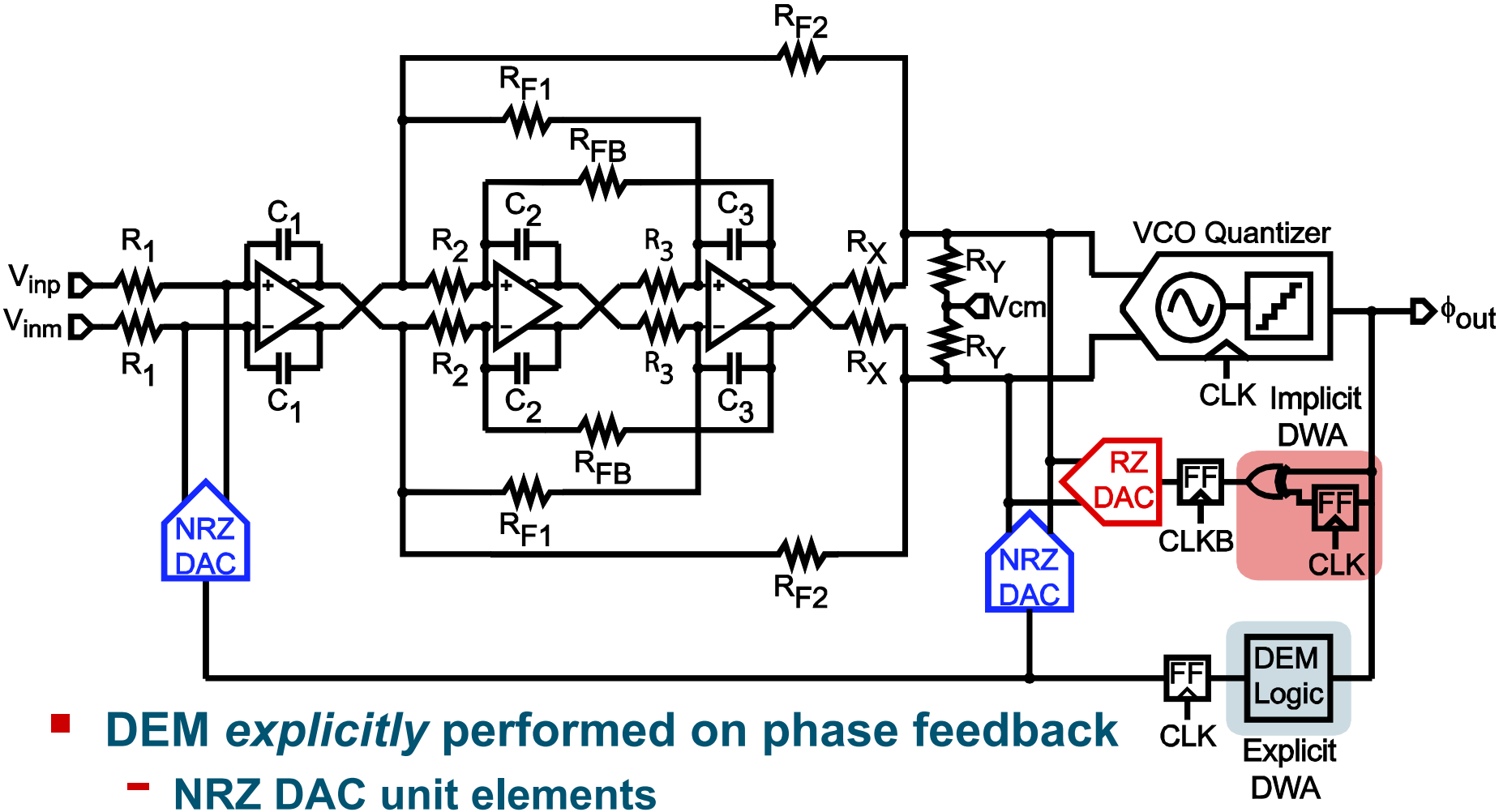
- **Opamp-RC integrators**
  - **Better linearity than Gm-C, though higher power**

Schematic of Proposed Architecture



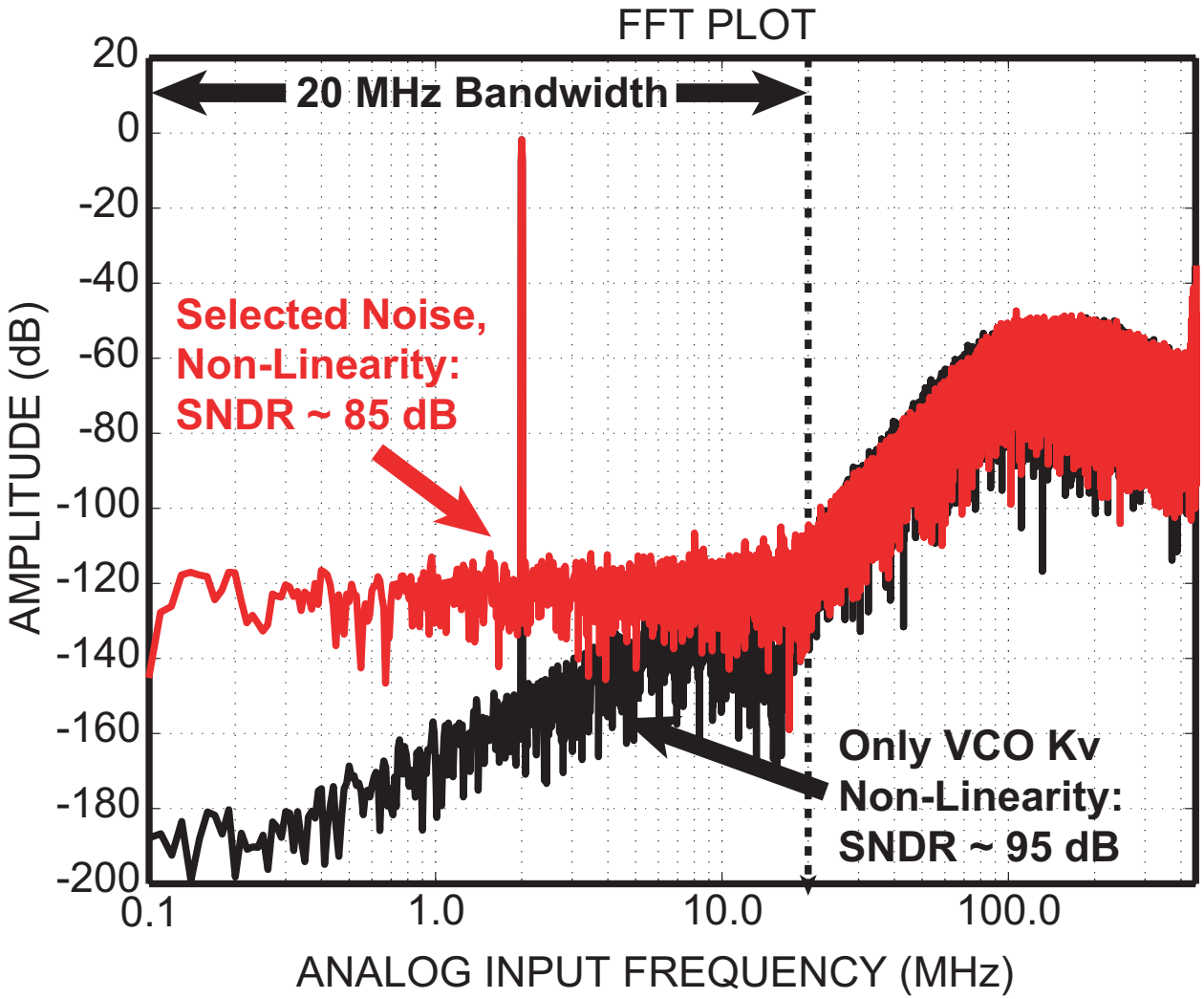
- Passive summation performed with resistors
  - Low power
  - Must design carefully to minimize impact of parasitic pole

Schematic of Proposed Architecture



- DEM *explicitly* performed on phase feedback
  - NRZ DAC unit elements
- DEM *implicitly* performed on frequency feedback
  - RZ DAC unit elements (Note: Miller, US Patent (2004))

Behavioral Simulation (available at www.cppsim.com)



Key Nonidealities

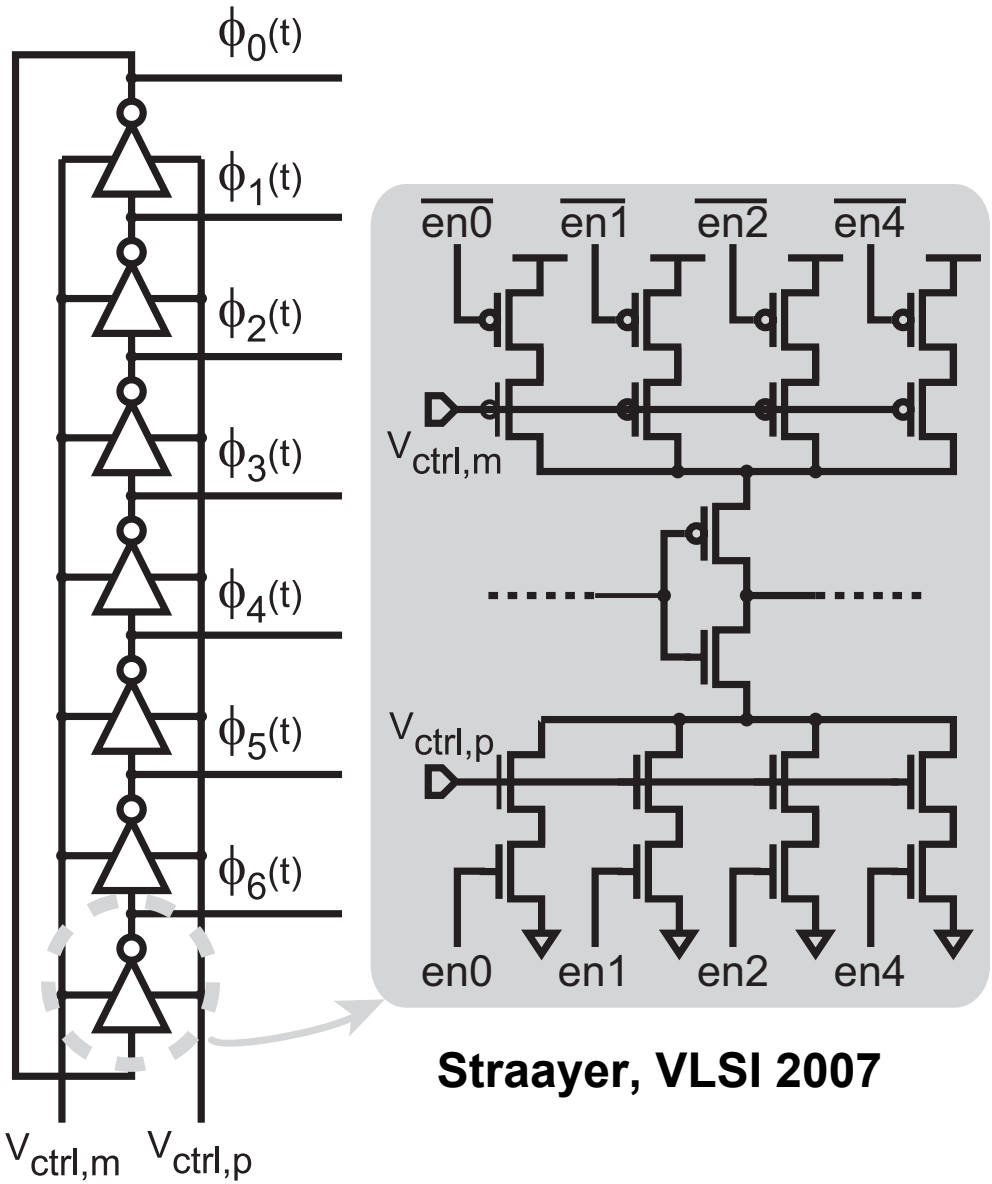
- VCO Kv non-linearity
- Device noise
- Amplifier finite gain, finite BW
- DAC and VCO unit element mismatch

85 dB SNDR!

VCO nonlinearity is *not* the bottleneck for achievable SNDR!

Circuit Details

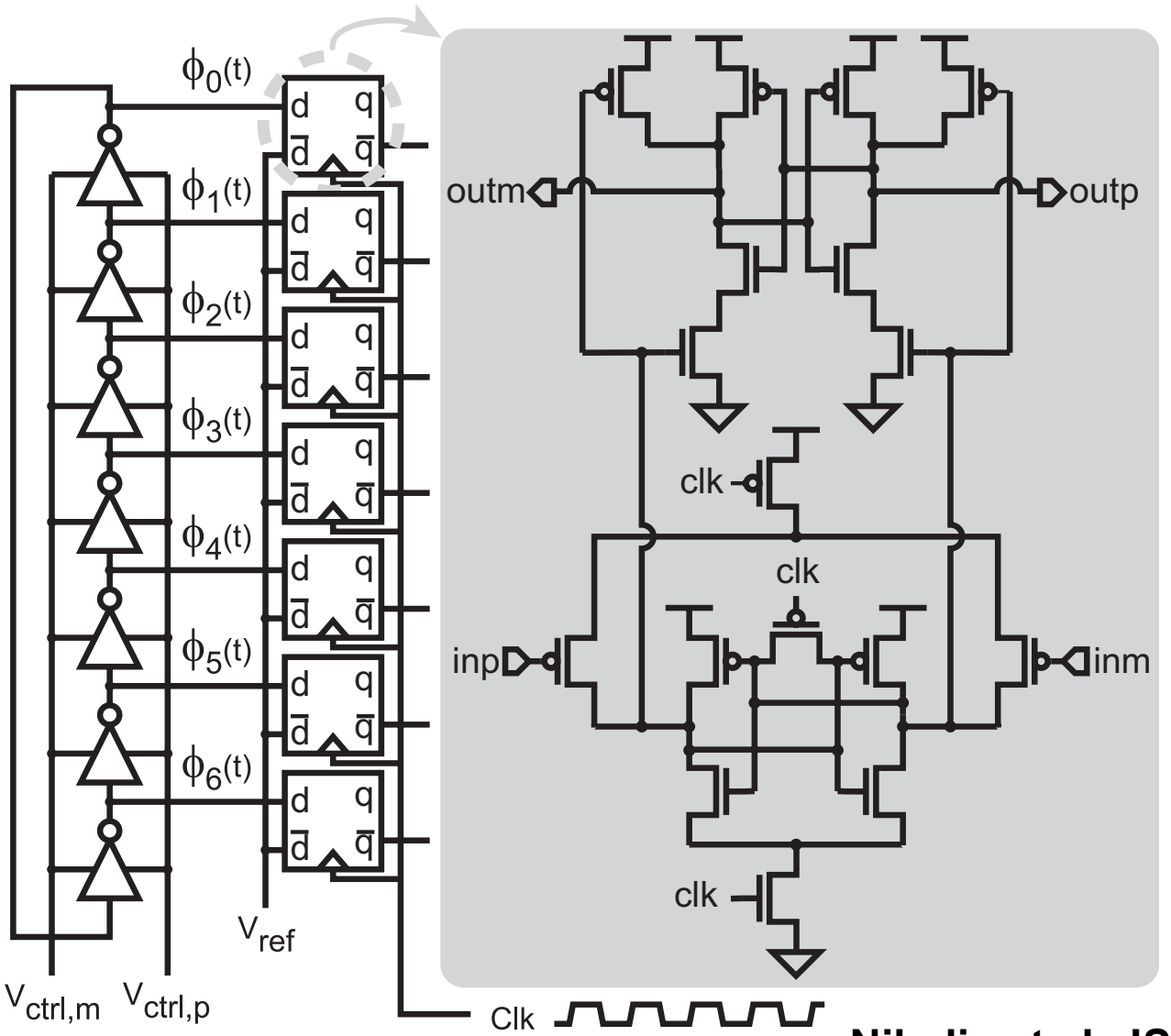
VCO Integrator Schematic



Straayer, VLSI 2007

- **15 stage current starved ring-VCO**
  - **7 stage ring-VCO shown for simplicity**
  - **Pseudo differential control**
  - **PVT variation accommodated by enable switches on PMOS/NMOS**
- **Rail-to-rail VCO output phase signals (VDD to GND)**

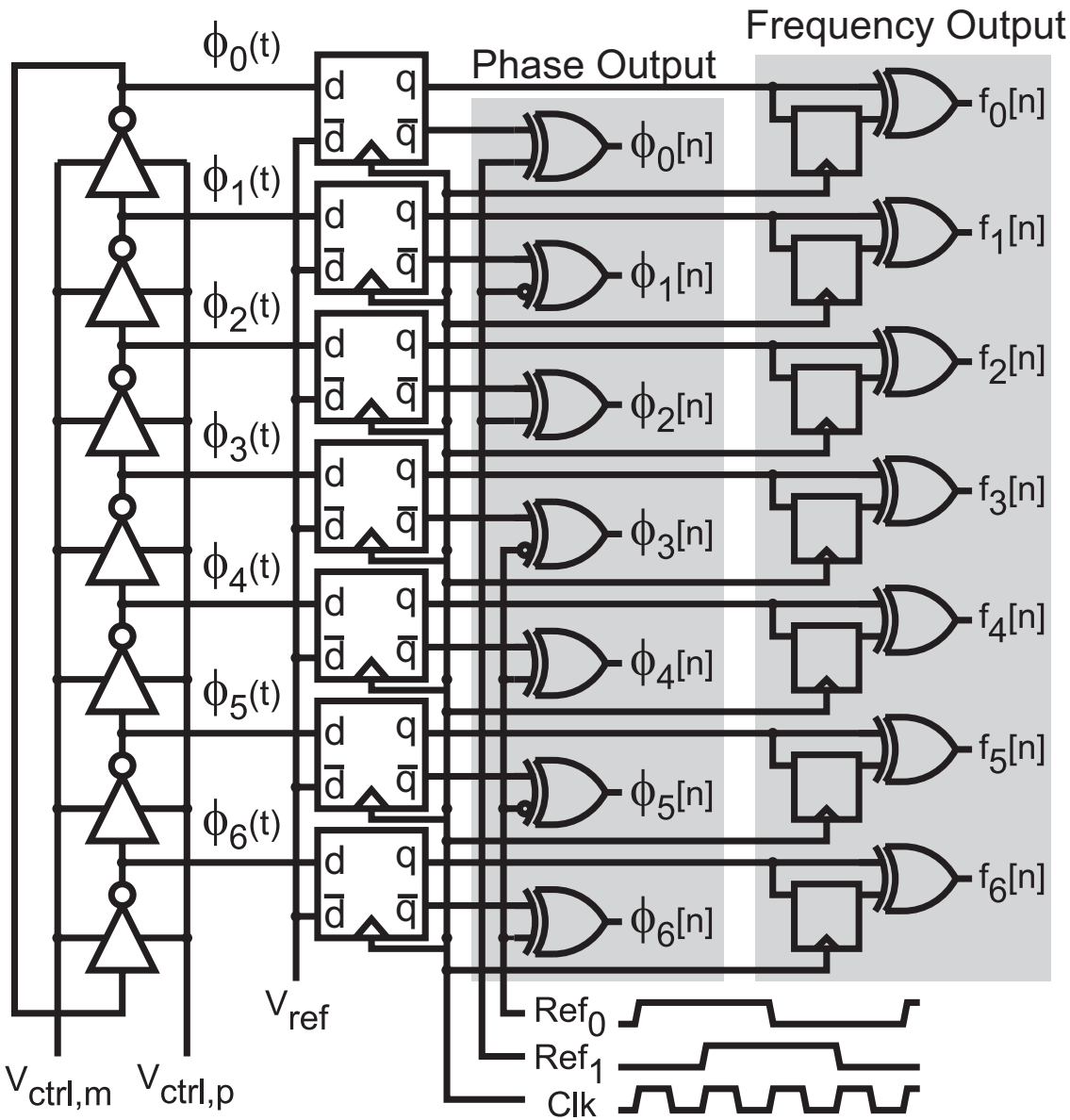
VCO Quantizer Schematic



- **Phase quantization with sense-amp flip-flop**
  - **Single phase clocking**
- **Rail-to-rail quantizer output signals (VDD to GND)**

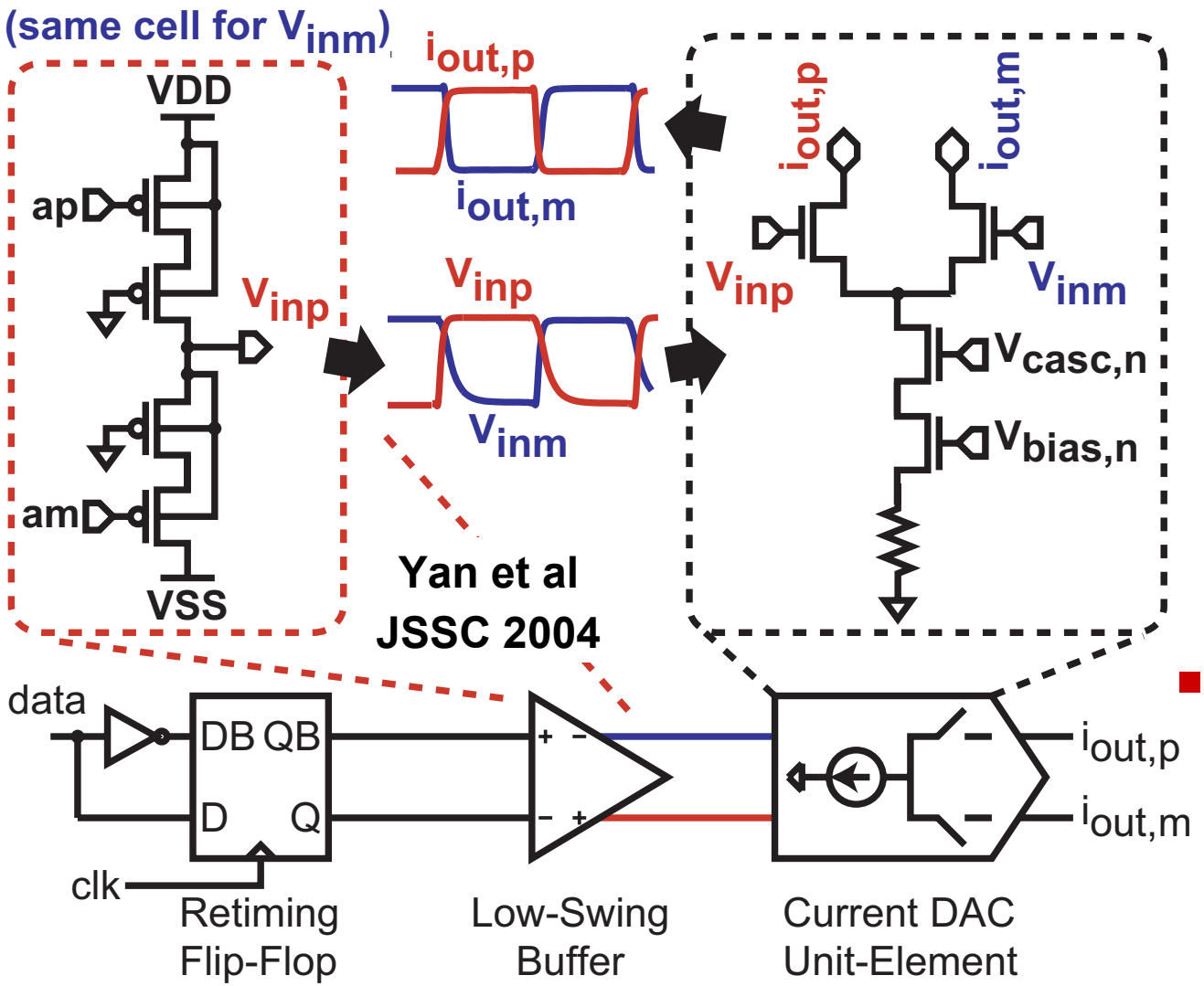
Nikolic et al, JSSC 2000

Phase Quantizer, Phase and Frequency Detector



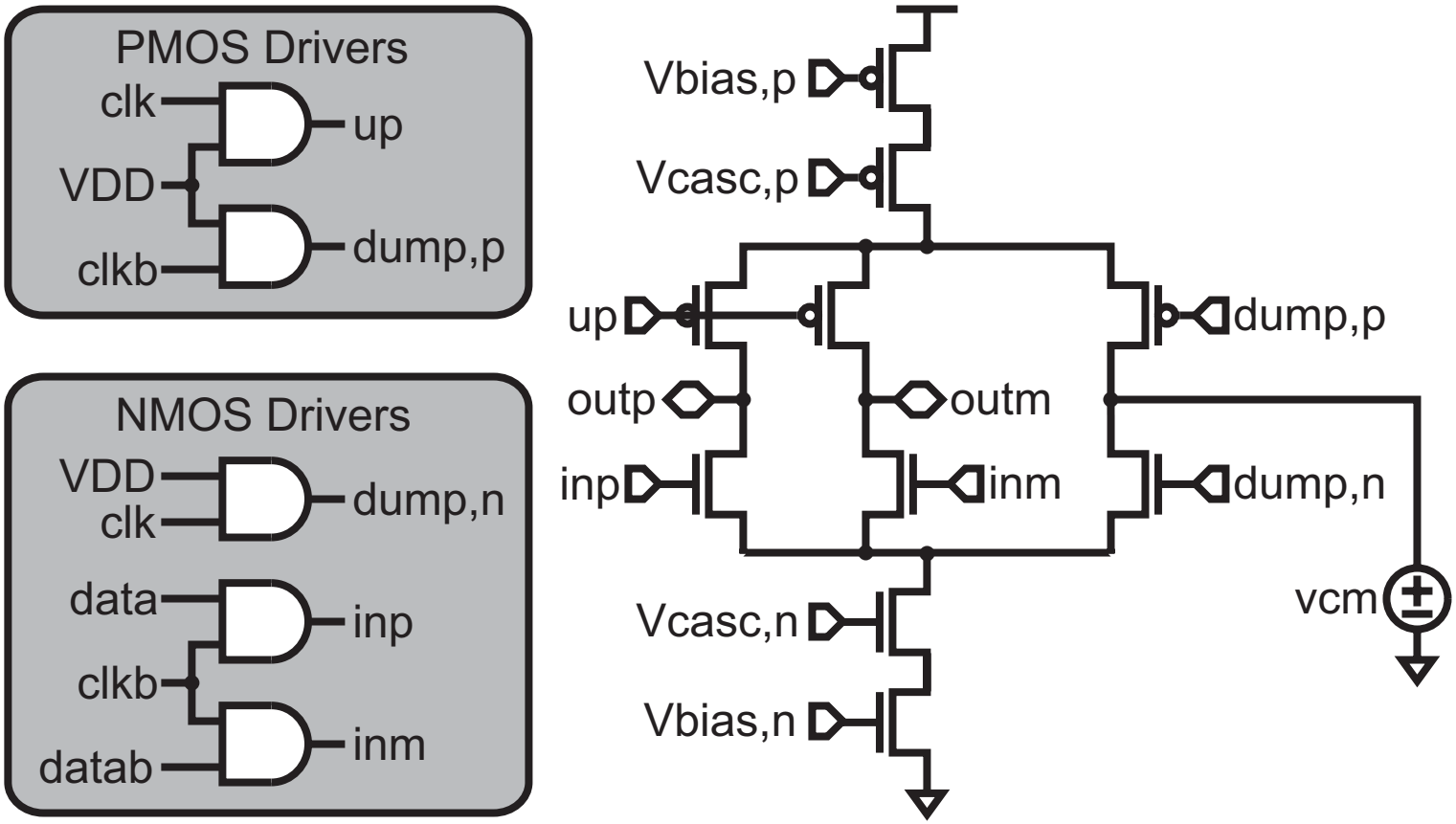
- **Highly digital implementation**
  - Phase sampled & quantized by SAFF
  - XOR phase and frequency detection with FF and XOR
- **Automatic DWA for frequency detector output code**
  - Must explicitly perform DWA on phase detector output code

Main Feedback DAC Schematic



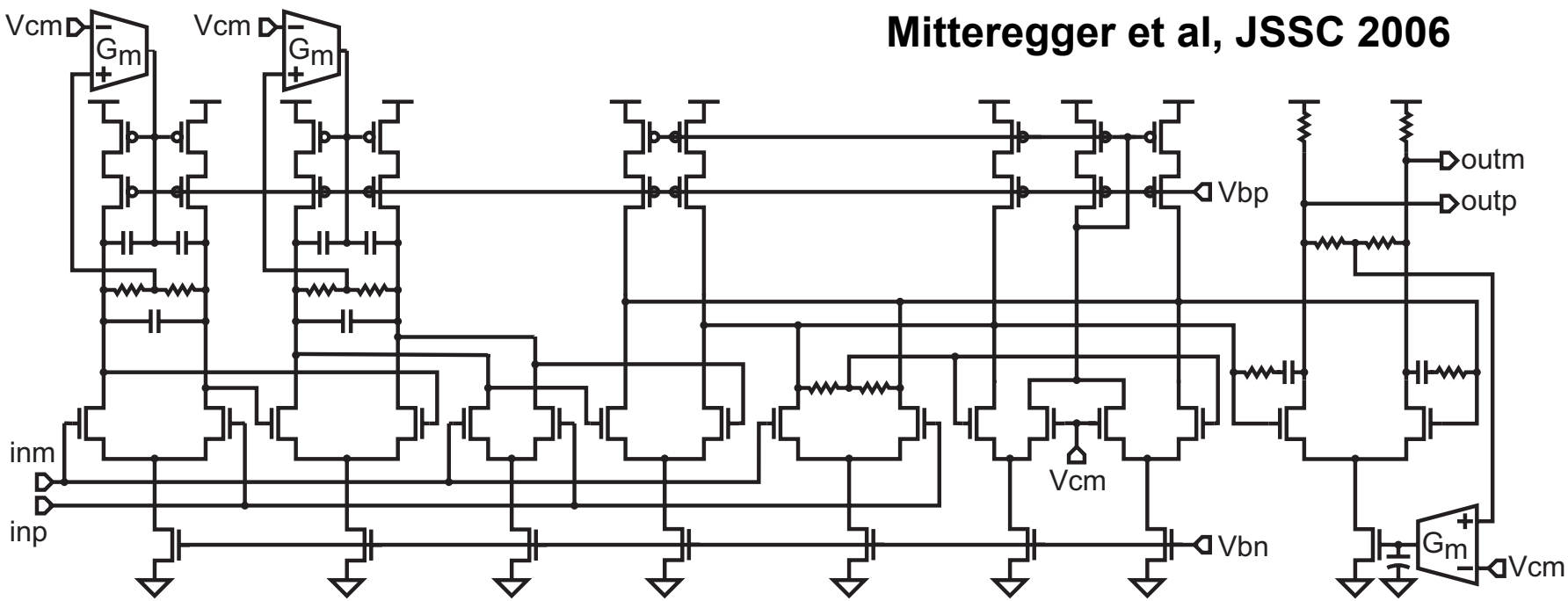
- Low-swing buffers
  - Keeps switch devices in saturation
  - Fast “on” / Slow “off” reduces glitches at DAC output
  - Uses external Vdd/Vss
- Resistor degeneration minimizes 1/f noise

Bit-Slice of Minor Loop RZ DAC



- **RZ DAC unit elements transition every sample period**
  - **Breaks code-dependency of transient mismatch (ISI)**
  - **Uses full-swing logic signals for switching**

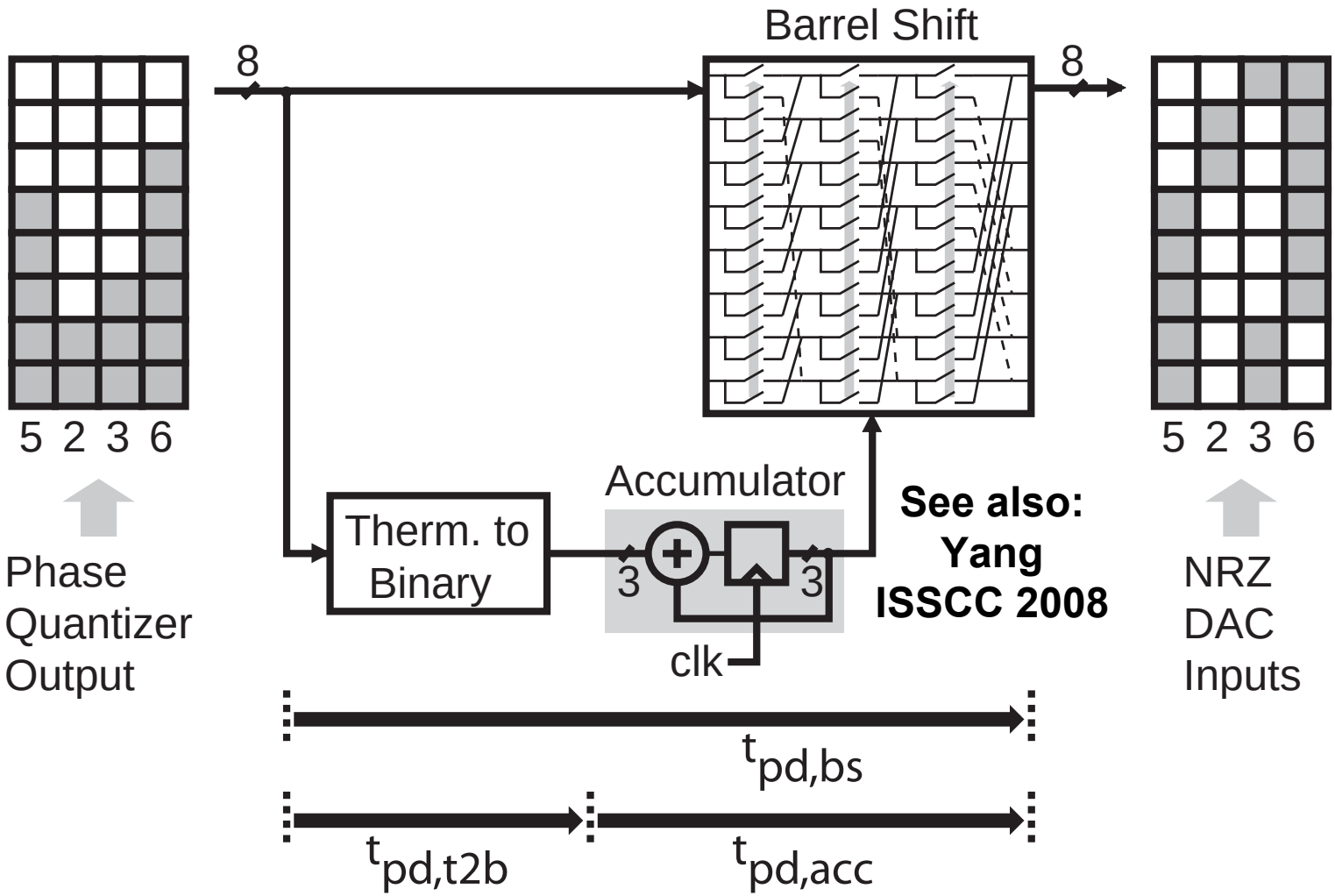
Opamp Schematic



Parameter	Value
DC Gain	63 dB
Unity-Gain Frequency	4.0 GHz
Phase Margin	55°
Input Referred Noise Power (20 MHz BW)	11 uV (rms)
Power (V_{DD} = 1.5 V)	22.5 mW

- Modified nested Miller opamp
  - 4 cascaded gain stages, 2 feedforward stages
  - Behaves as 2-stage Miller near cross-over frequencies
  - Opamp 1 power is 2X of opamps 2 and 3 (for low noise)

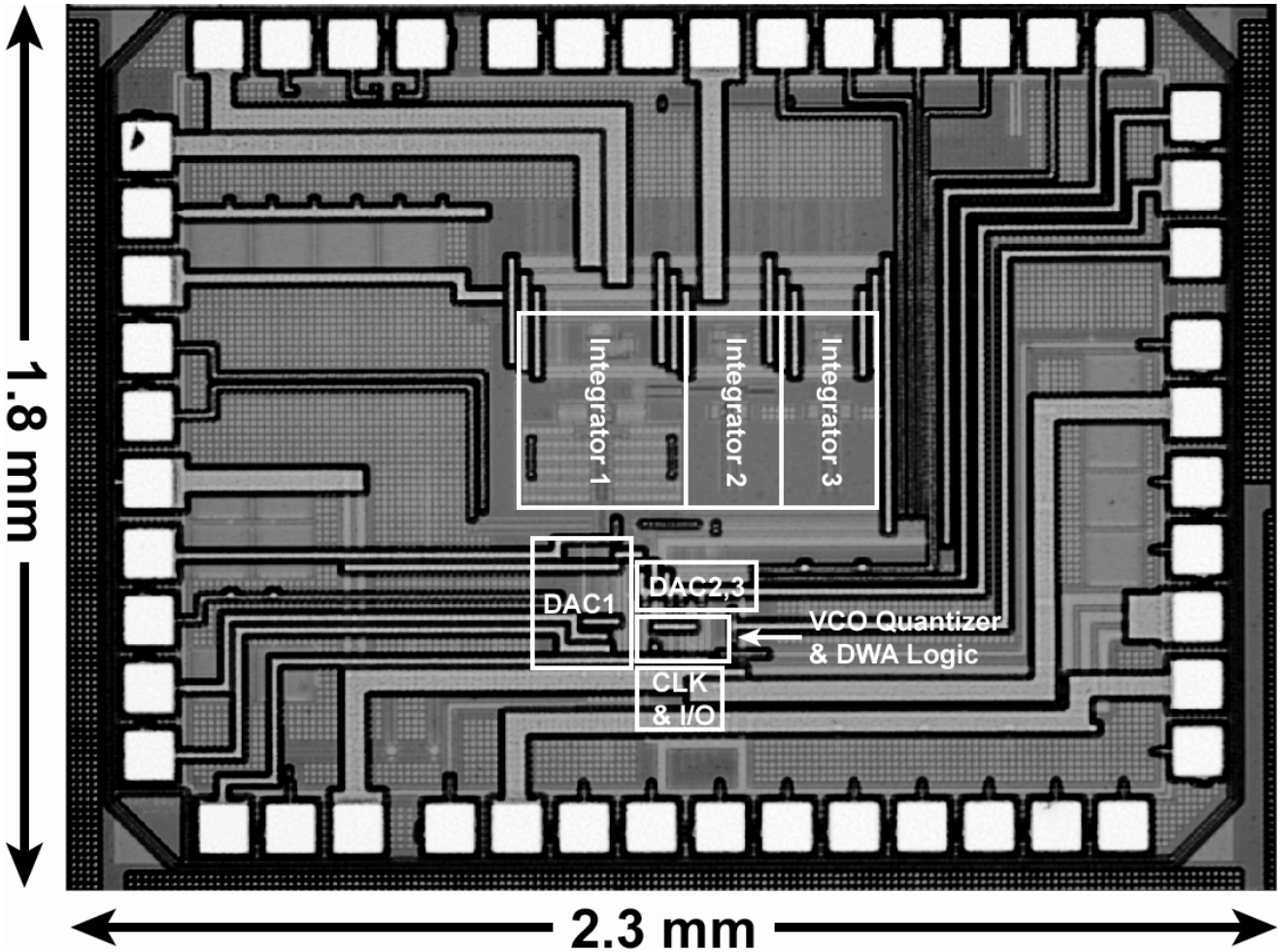
DEM Architecture (3-bit example)



- **Achieves low-delay to allow 4-bit DEM at 900 MHz**
  - **Code through barrel shift propagates in half a sample period**

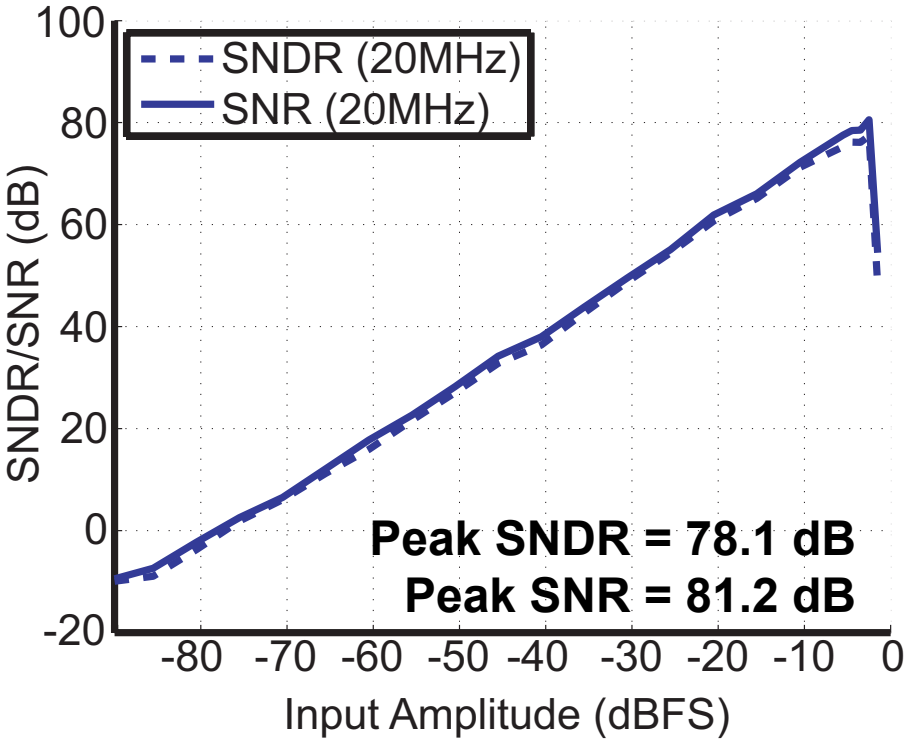
Die Photo (0.13u CMOS)

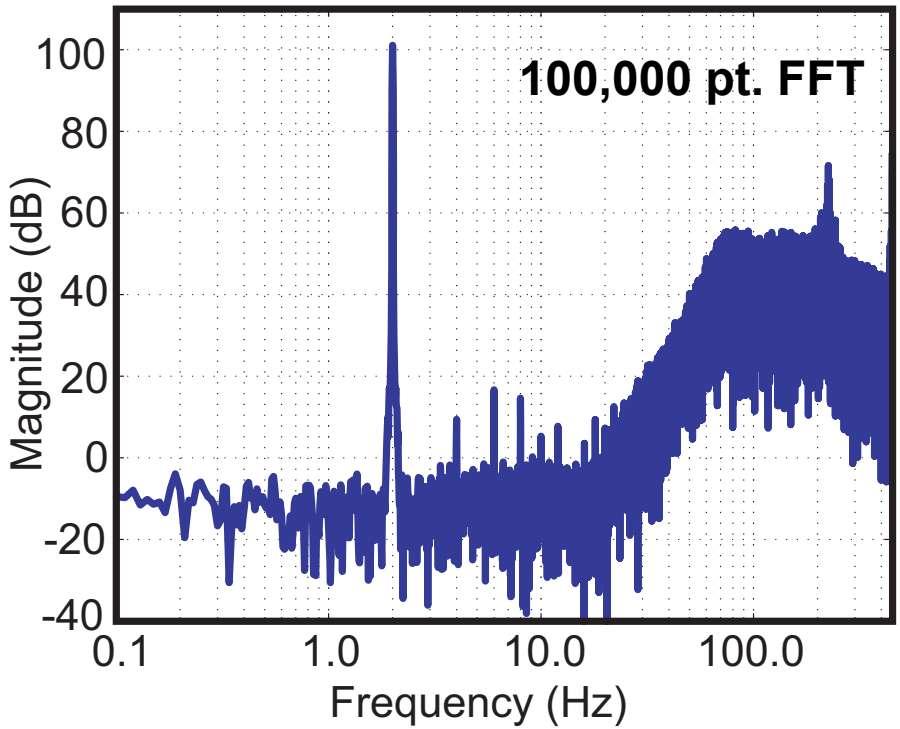
Die photo courtesy of Annie Wang (MTL)



- Active area
  - 0.45 mm^2
- Sampling Freq
  - 900 MHz
- Input BW
  - 20 MHz
- Supply Voltage
  - 1.5 V
- Analog Power
  - 69 mW
- Digital Power
  - 18 mW

Measured Results

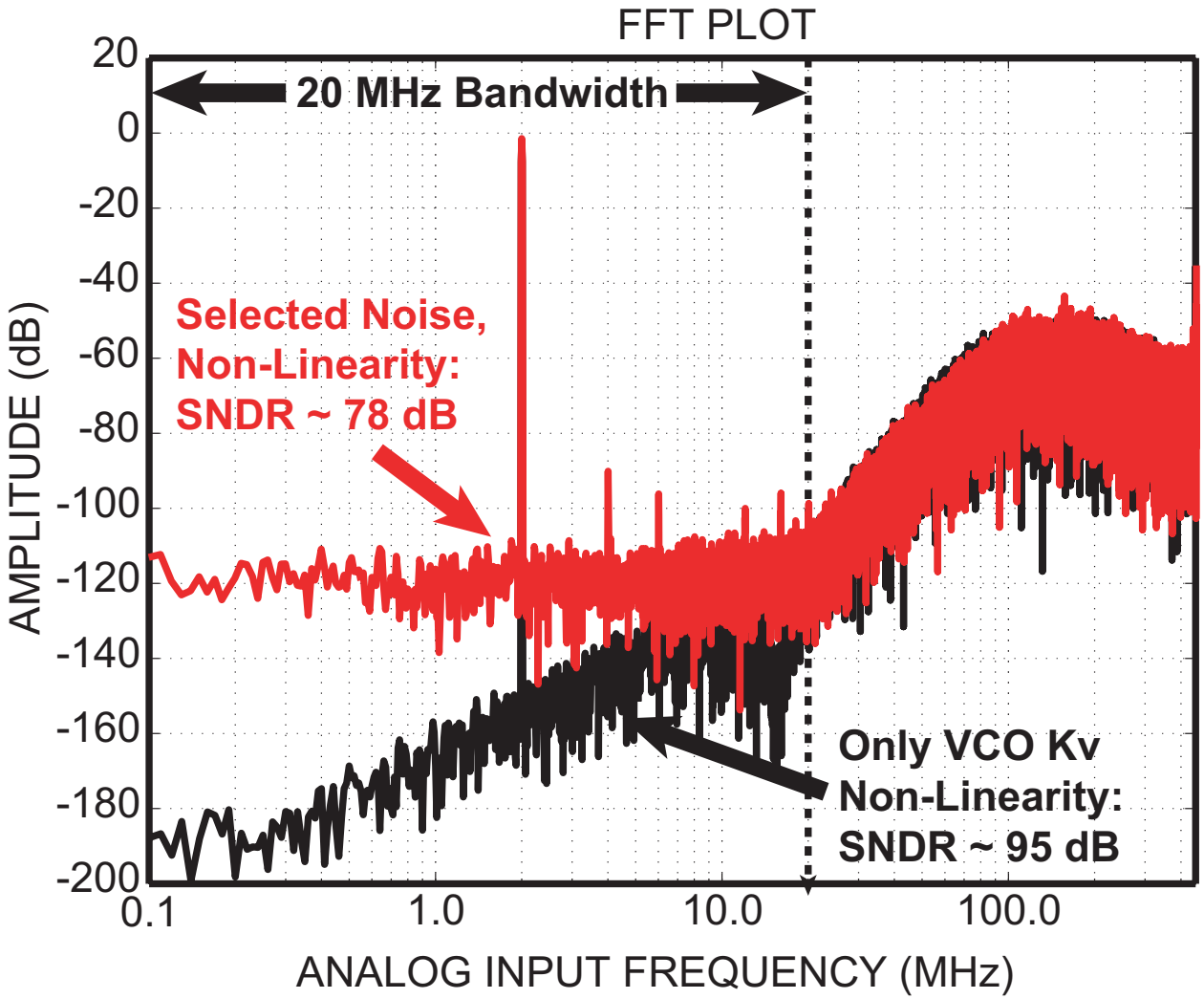




- 78 dB Peak SNDR performance in 20 MHz
  - Bottleneck: transient mismatch from main feedback DAC
- Architecture robust to VCO K_v non-linearity

Figure of Merit: 330 fJ/Conv with 78 dB SNDR

Behavioral Model Reveals Key Performance Issue



- Amplifier nonlinearity degrades SNDR to 81 dB
- DAC transient mismatch degrades SNDR to 78 dB
  - DEM does not help
  - Could be improved with dual RZ structure

Transient DAC mismatch is likely the key bottleneck

Conclusion

- **VCO-based quantization is a promising component to achieve high performance Σ–Δ ADC structures**
  - **High speed, low power, low area implementation**
  - **First order shaping of quantization noise and mismatch**
  - **Kv non-linearity was a limitation in previous approaches**

- **Demonstrated a 4th-order CT ΔΣ ADC with a VCO-based integrator and quantizer**
  - **Proposed voltage-to-phase conversion to avoid distortion from Kv non-linearity**
  - **Achieved 78 dB SNDR in 20 MHz BW with 87 mW power**
    - Key performance bottleneck: transient DAC mismatch