

***High Speed Communication Circuits and Systems***  
***Lecture 21***  
***MSK Modulation and***  
***Clock and Data Recovery Circuits***

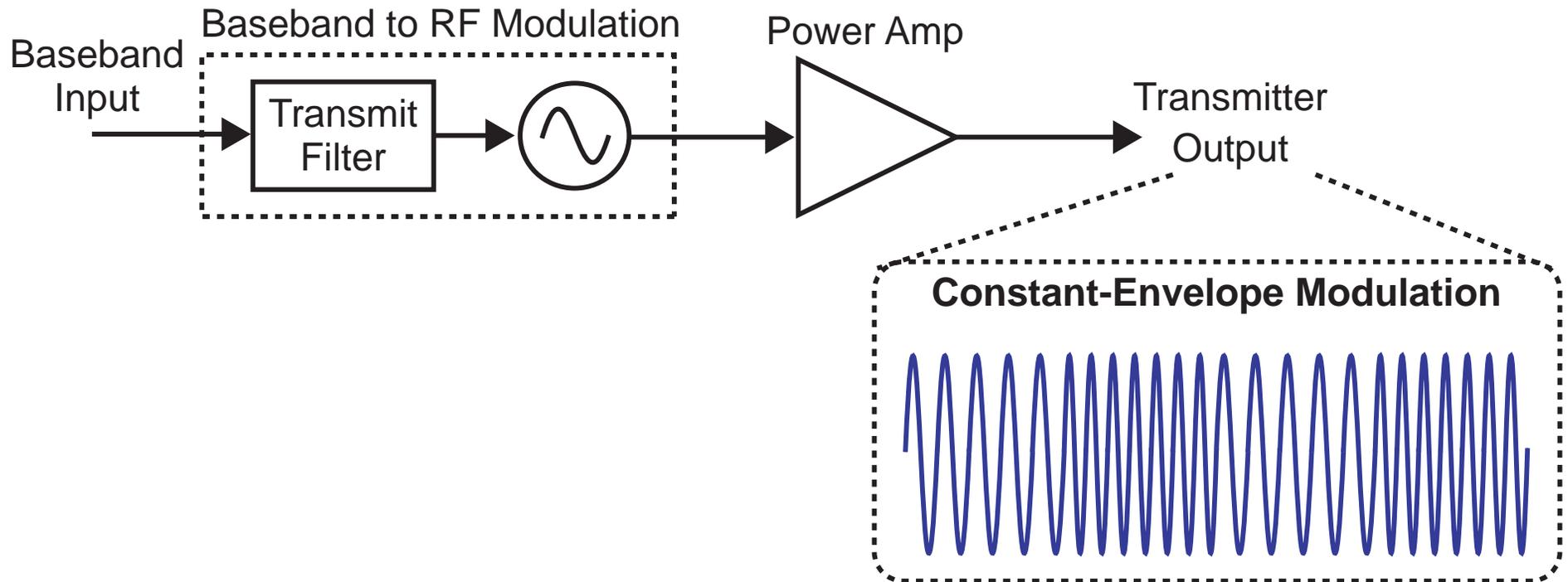
**Michael H. Perrott**

**April 23, 2004**

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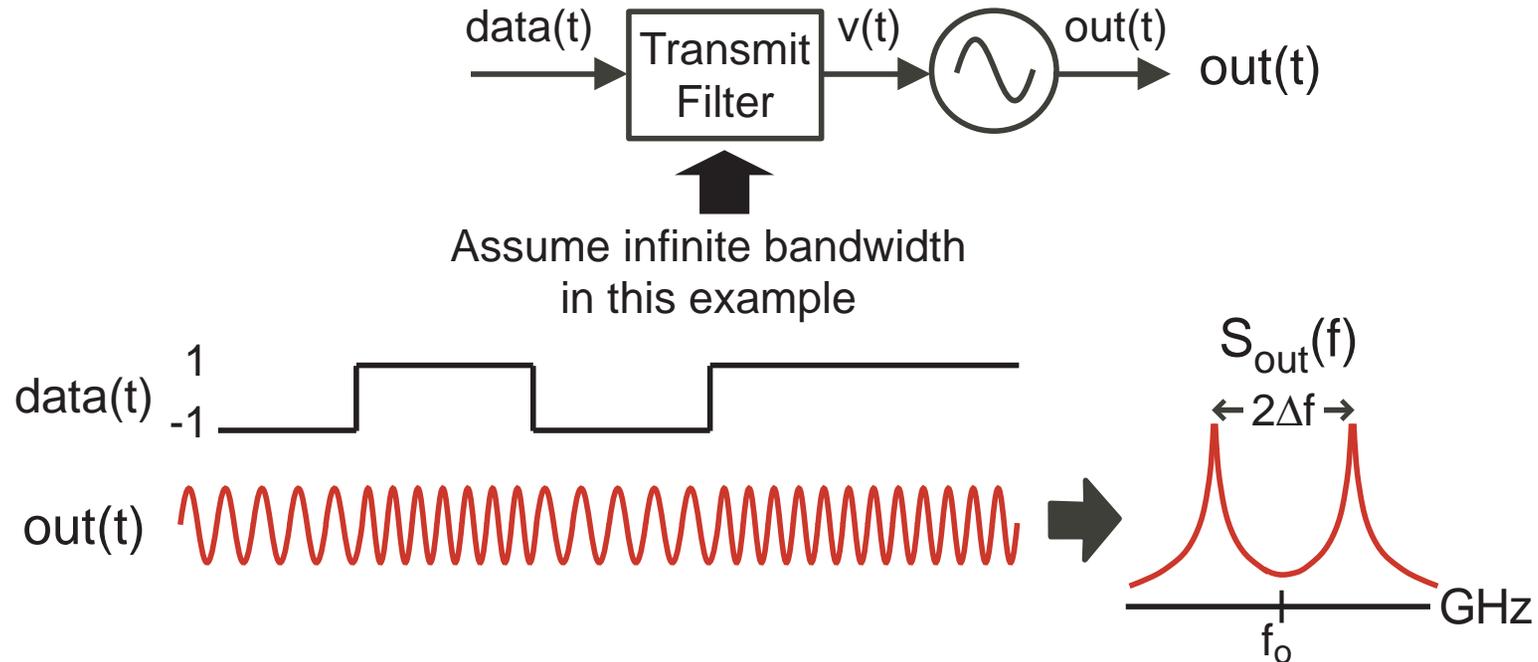
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# Recall Constant Envelope Modulation from Lecture 19



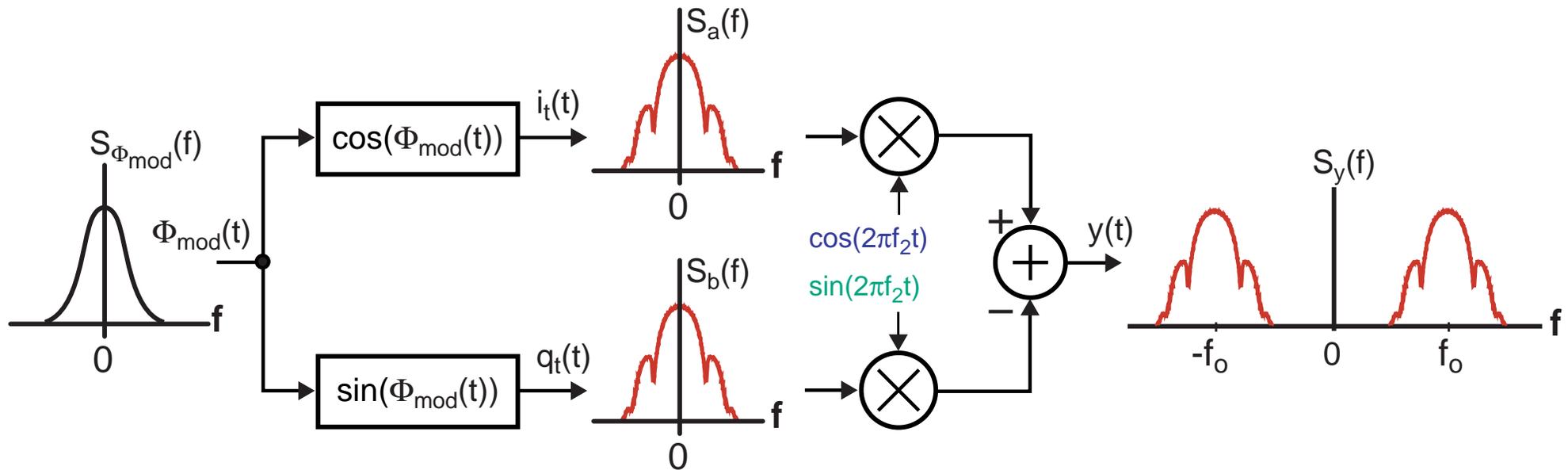
- Popular for cell phones and cordless phones due to the reduced linearity requirements on the power amp
  - Allows a more efficient power amp design
    - Transmitter power is reduced

# Frequency Shift Keying



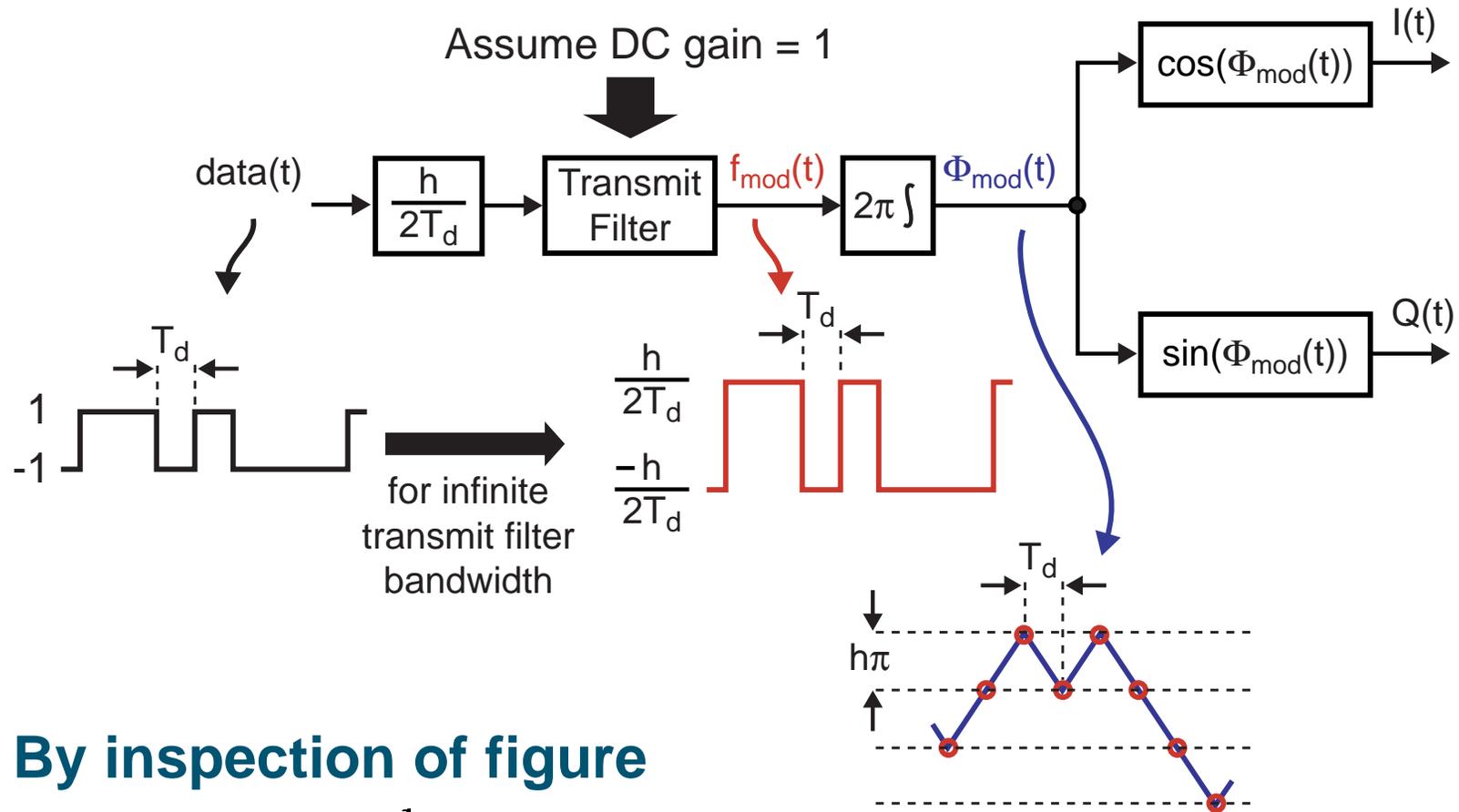
- **Sends information encoded in instantaneous frequency**
  - Can build simple transmitters and receivers
    - Pagers use this modulation method
- **Issue – want to obtain high spectral efficiency**
  - Need to choose an appropriate transmit filter
  - Need to choose an appropriate value of  $\Delta f$

# Transmit Filter Selection



- Recall from Lecture 19 that output spectrum is related in a nonlinear manner to transmit filter
  - Raised cosine filter is not necessarily the best choice
- We'll come back to this issue
  - Focus instead on choosing  $\Delta f$

# A More Detailed Model



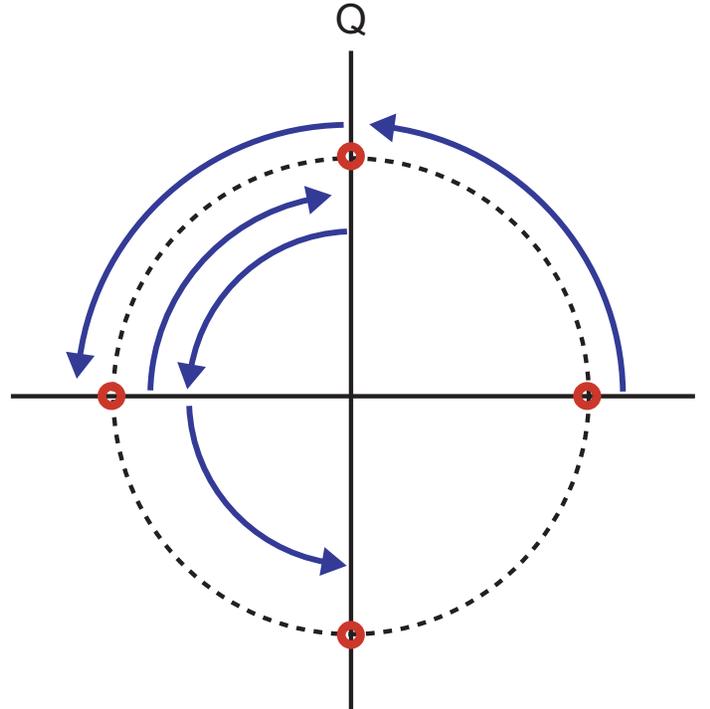
- By inspection of figure

$$\Delta f = \frac{h}{2T_d}$$

- The choice of  $\Delta f$  is now parameterized by  $h$  and  $T_d$ 
  - $h$  is called the modulation index,  $T_d$  is symbol period

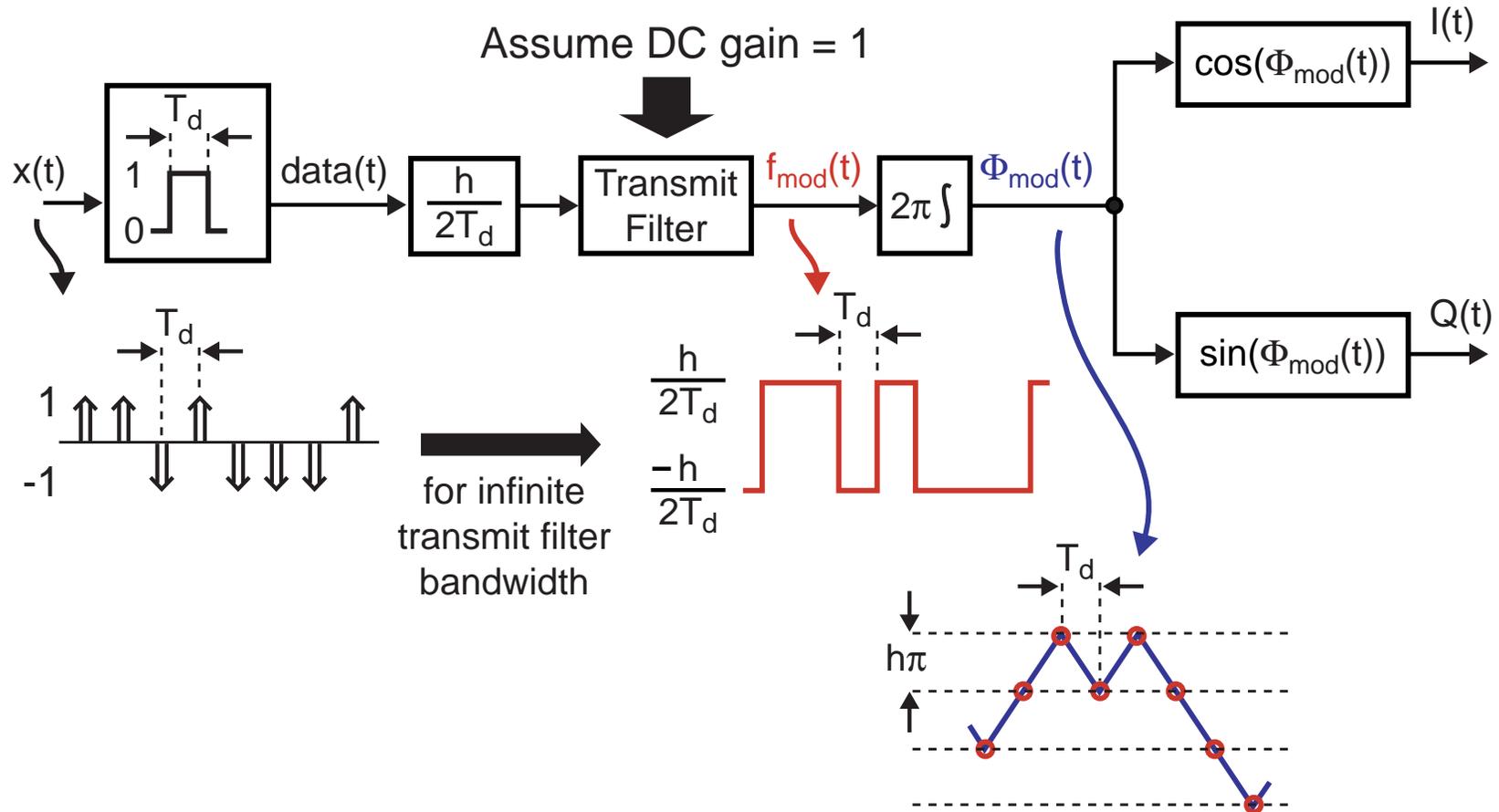
# MSK Modulation

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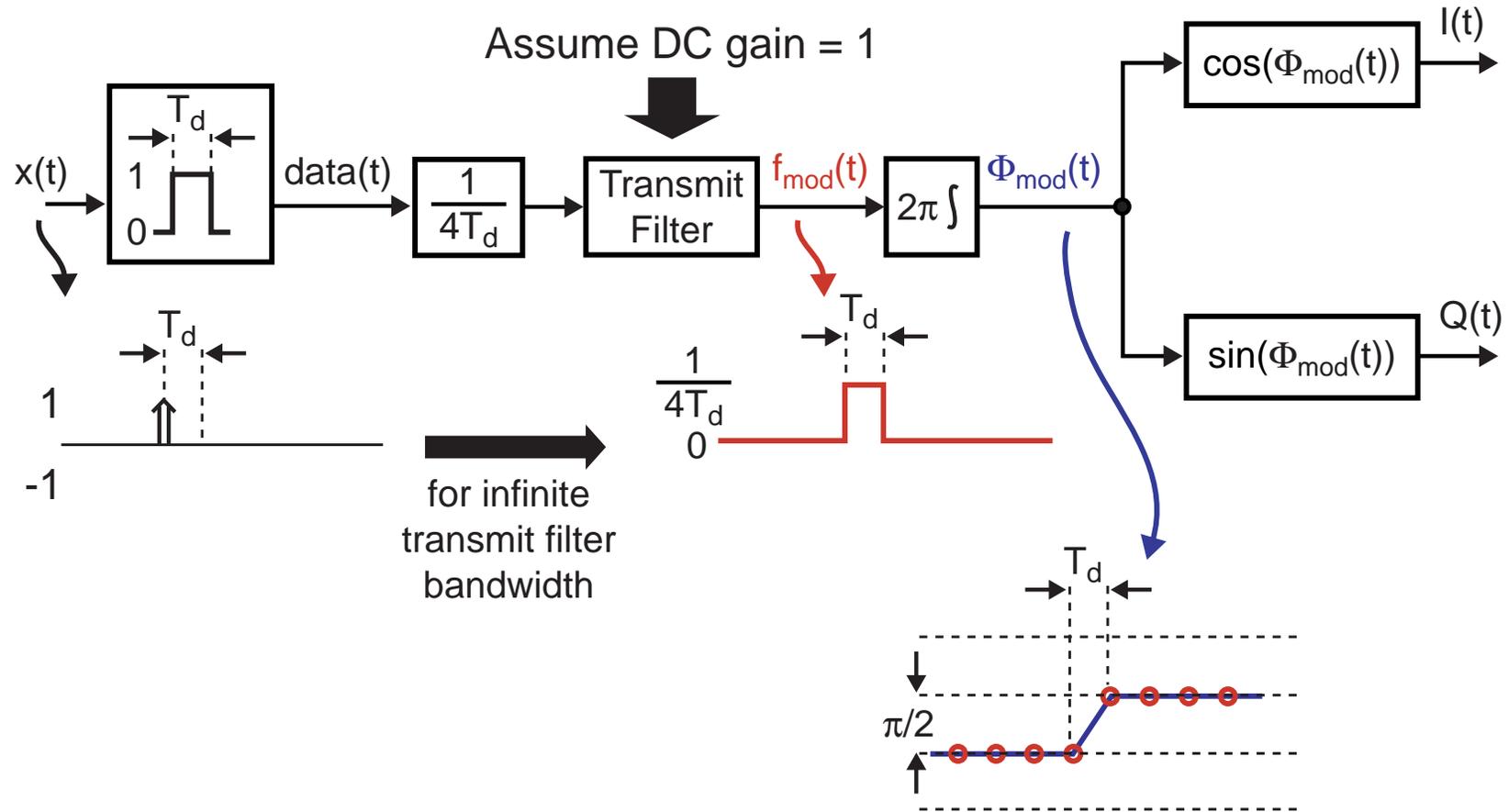
- Choose  $h$  such that the phase rotates  $\pm 90^\circ$  each symbol period
  - Based on previous slide, we need  $h = 1/2$
  - Note: 1-bit of information per symbol period
    - Bit rate = symbol rate

# A More Convenient Model for Analysis



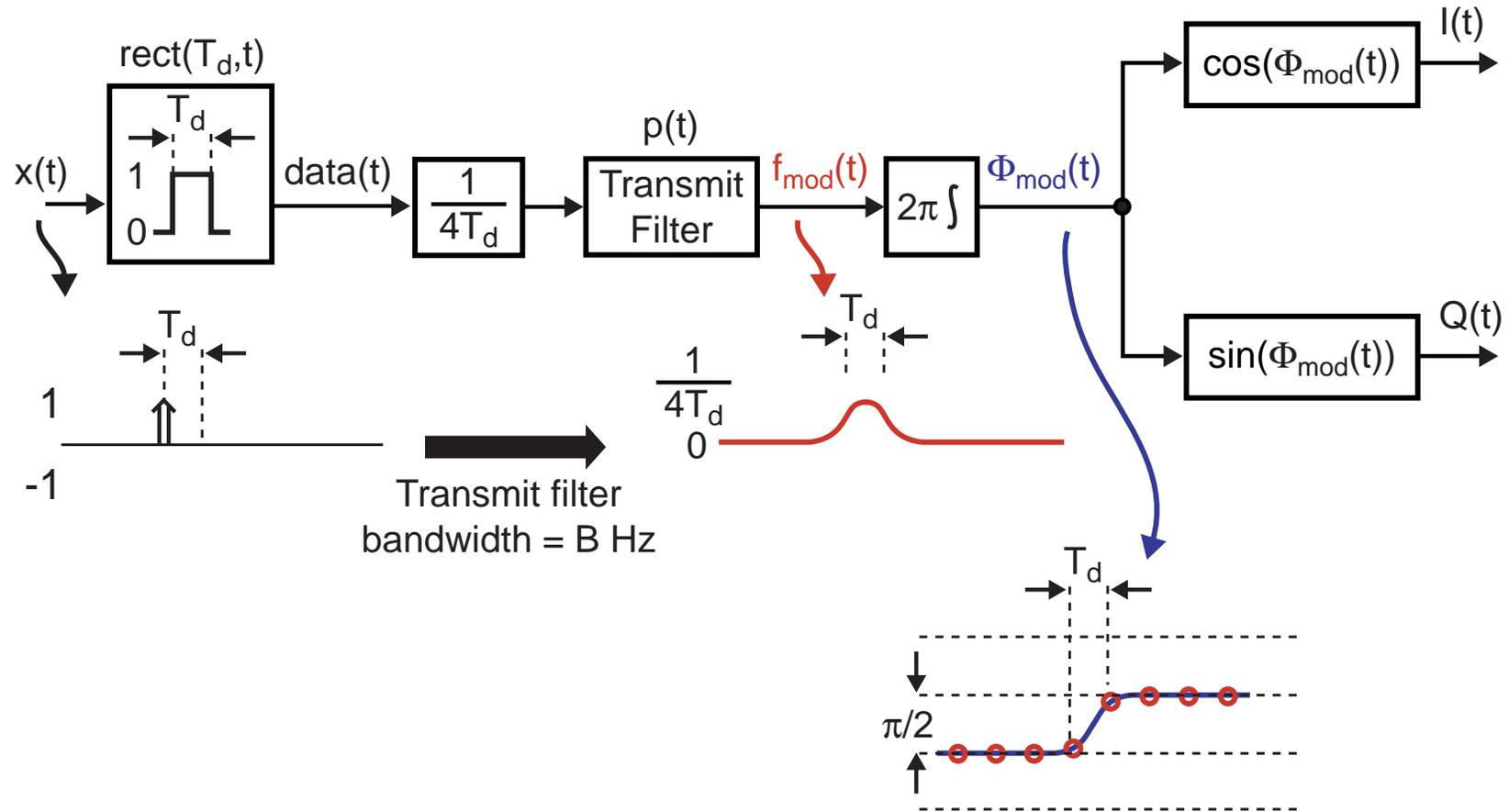
- Same as previous model, but we represent data as impulses convolved with a rectangular pulse
  - Note that  $h = 1/2$  for MSK

# Impact of Sending a Single Data Impulse



- To achieve MSK modulation, resulting phase shift must be  $\pm 90^\circ$  (i.e.,  $\pi/4$ )

# Include Influence of Transmit Filter



## ■ For MSK modulation

$$2\pi \int_{-\infty}^{\infty} \text{rect}(T_d, t) * \frac{1}{4T_d} p(t) = \frac{\pi}{2}$$

— Where \* denotes convolution

# Gaussian Minimum Shift Keying

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## ■ Definition

- Minimum shift keying in which the transmit filter is chosen to have a Gaussian shape (in time and frequency) with bandwidth = B Hz

$$p(t) = \frac{1}{\sqrt{2\pi\sigma}} e^{-\frac{1}{2}\left(\frac{t}{\sigma}\right)^2}$$

$$\text{where : } \sigma = \frac{.833T_d}{(BT_d)2\pi}$$

## ■ Key parameters

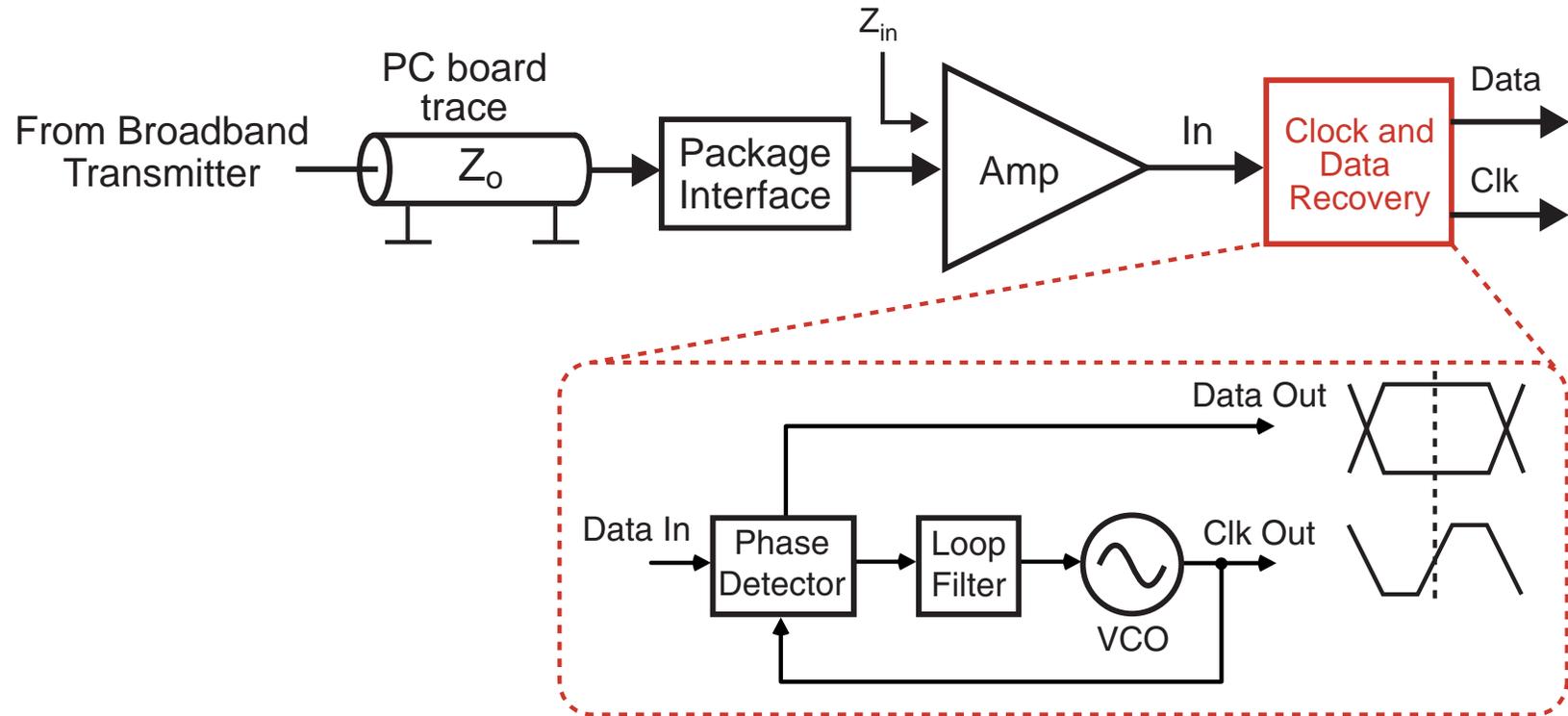
- Modulation index: as previously discussed
  - $h = 1/2$
- $BT_d$  product: ratio of transmit filter bandwidth to data rate
  - For GSM phones:  $BT_d = 0.3$

## Project 2

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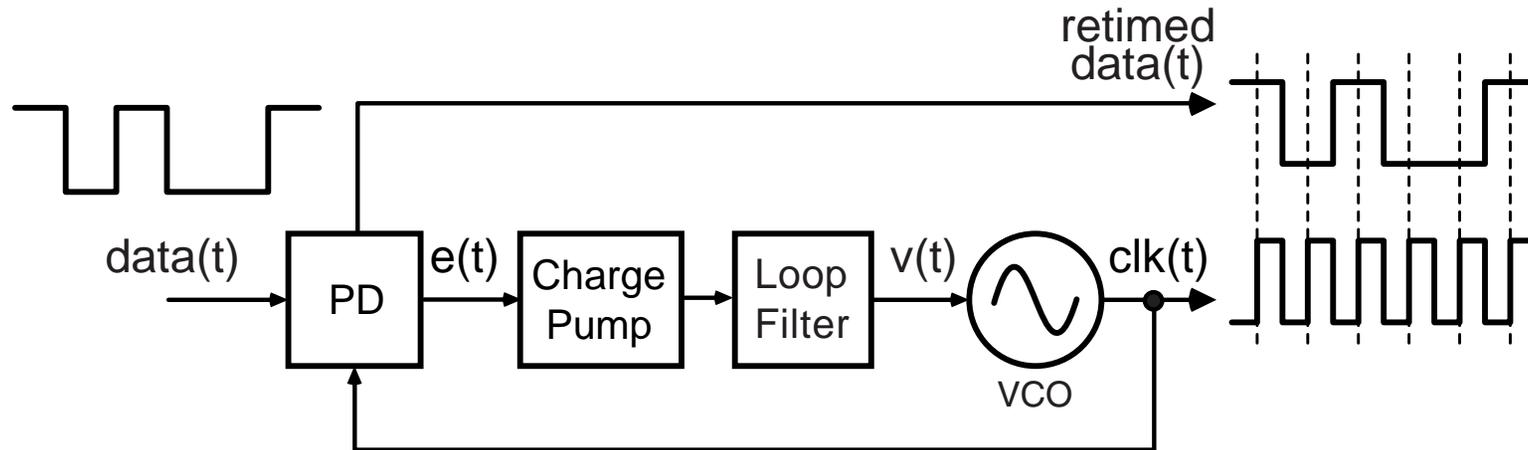
- **Simulate a GMSK transmitter and receiver**
- **What you'll learn**
  - **How GMSK works at the system level**
  - **Behavioral level simulation of a communication system**
  - **Generation of eye diagrams and spectral plots**
  - **Analysis and simulation of discrete-time version of loop filter and other signals**
- **Note: you'll also be exposed a little to GFSK modulation**
  - **Popular for cordless phones**
  - **Similar as GMSK, but frequency is the important variable rather than phase**
    - **Typical GFSK specs:  $h = 0.5 \pm 0.05$ ,  $BT_d = 0.5$**

# High Speed Data Links



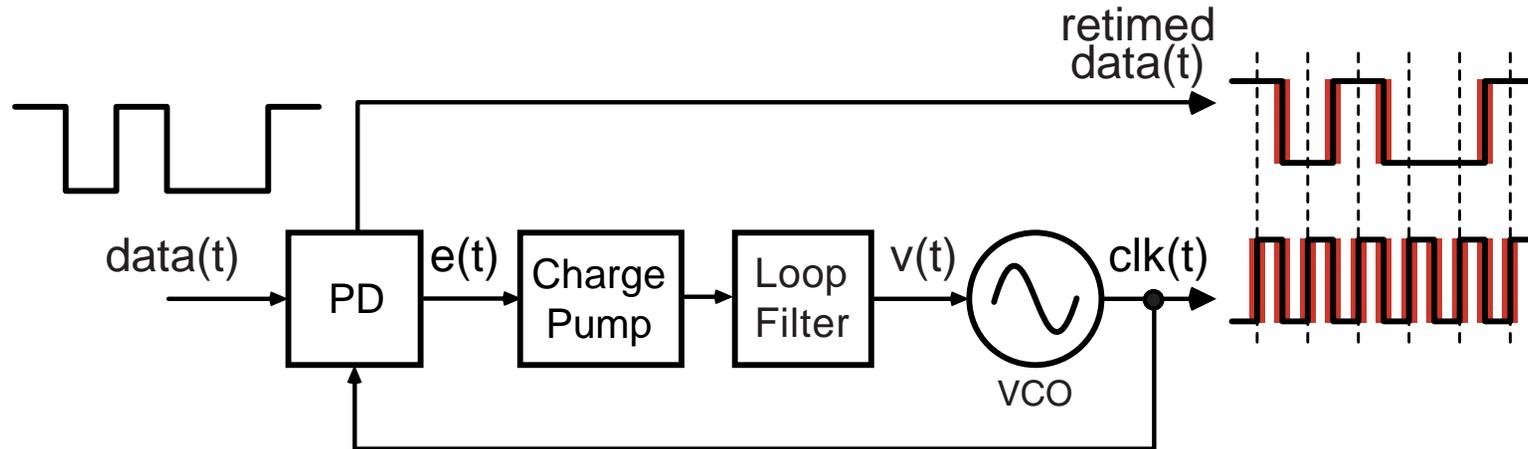
- **A challenging component is the clock and data recovery circuit (CDR)**
  - **Two primary functions**
    - Extract the clock corresponding to the input data signal
    - Resample the input data

# PLL Based Clock and Data Recovery



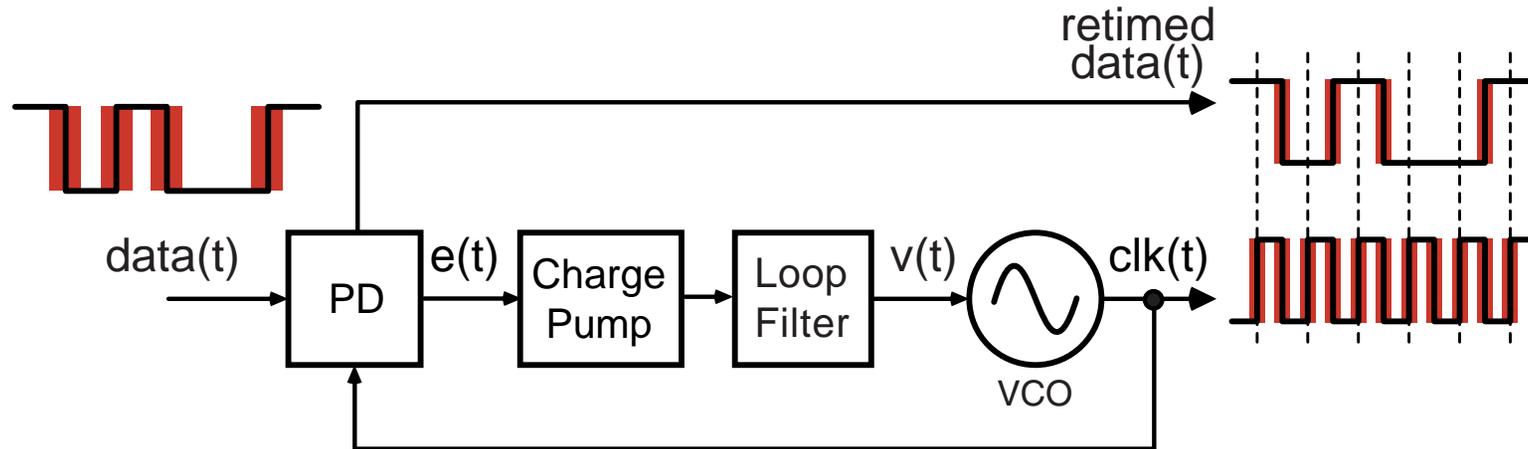
- Use a phase locked loop to tune the frequency and phase of a VCO to match that of the input data
- Performance issues
  - Jitter
  - Acquisition time
  - Bit error rate (at given input levels)
- Let's focus on specifications for OC-48
  - i.e., 2.5 Gbit/s SONET

# Jitter Generation



- **Definition**
  - The amount of jitter at the output of the CDR when no jitter (i.e., negligible jitter) is present on the data input
- **SONET requires**
  - $< 10$  mUI rms jitter
  - $< 100$  mUI peak-to-peak jitter
- **Note:** UI is unit interval, and is defined as the period of the  $clk$  signal (i.e., 400 ps for 2.5 Gbit/s data rates)

# Jitter Tolerance



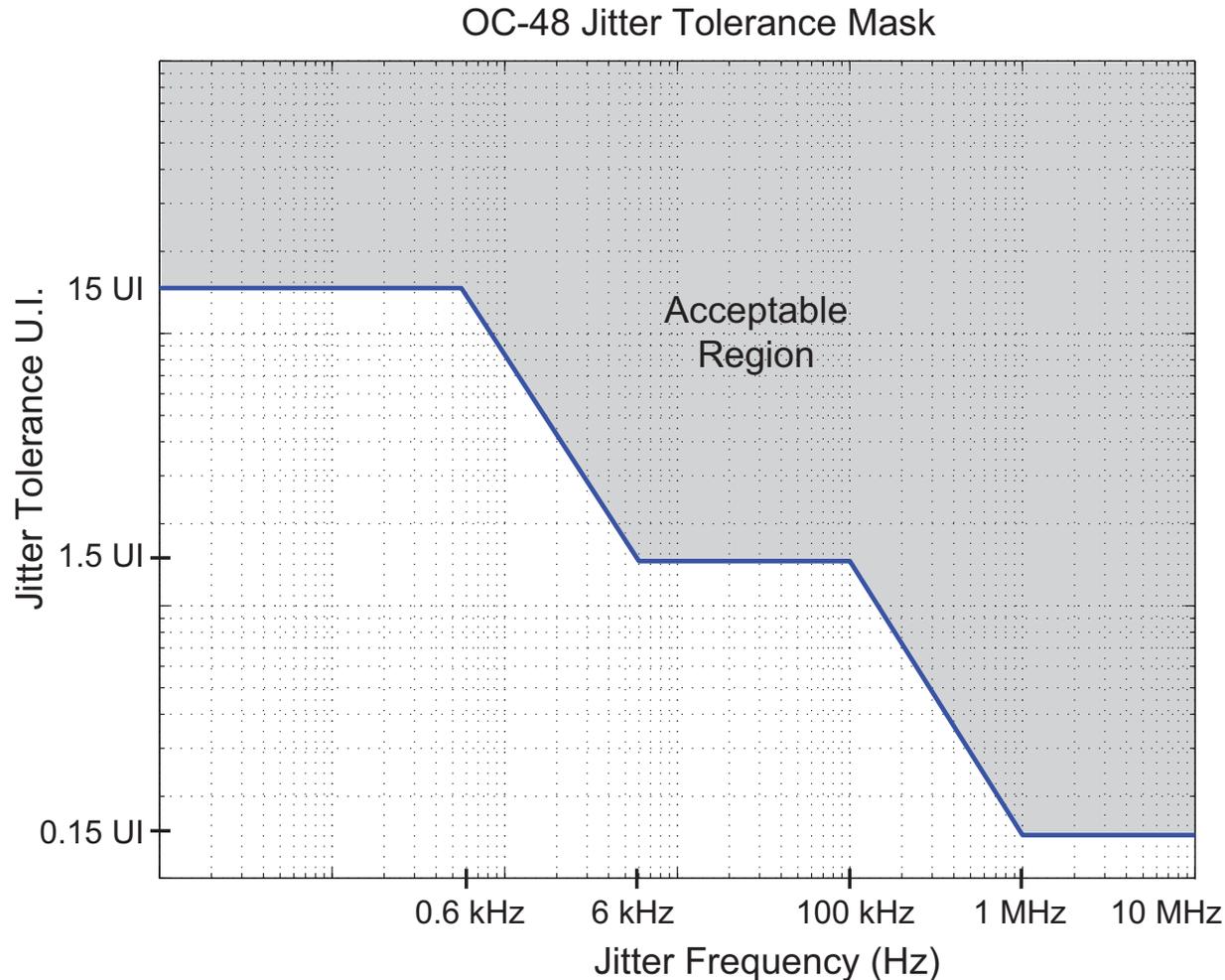
## ■ Definition

- The maximum amount of jitter allowed on the input while still achieving low bit error rates ( $< 1e-12$ )

## ■ SONET specifies jitter tolerance according to the frequency of the jitter

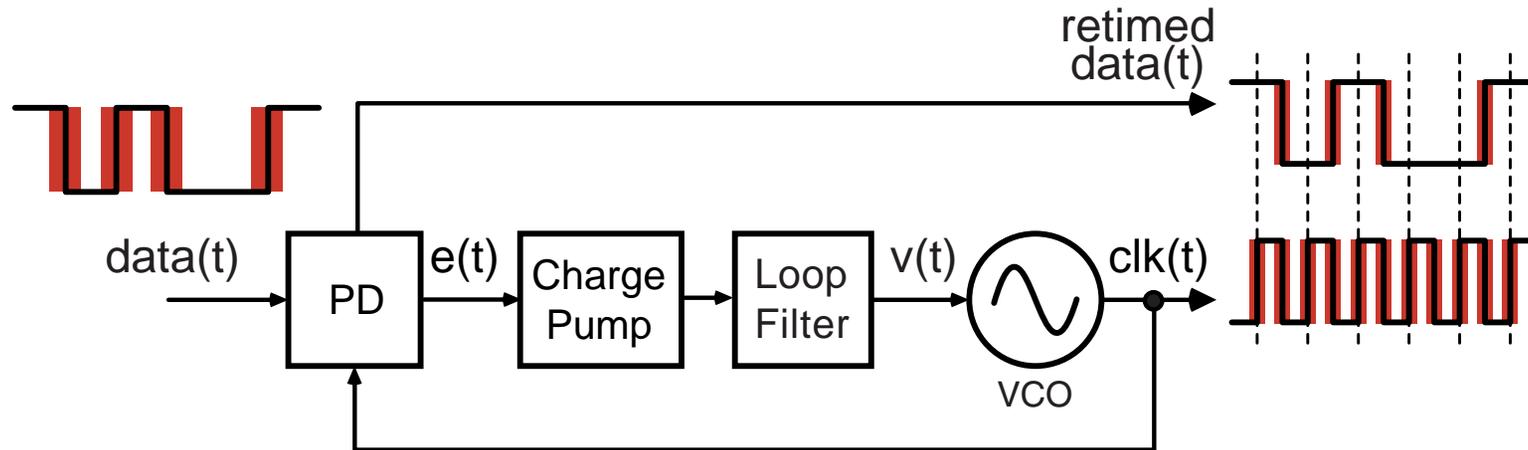
- Low frequency jitter can be large since it is tracked by PLL
- High frequency jitter (above the PLL bandwidth) cannot be as high (PLL can't track it out)
  - Limited by setup and hold times of PD retiming register

# Example Jitter Tolerance Mask



- **CDR tested for tolerance compliance by adding sine wave jitter at various frequencies (with amplitude greater than mask) to the data input and observing bit error rate**

# Jitter Transfer



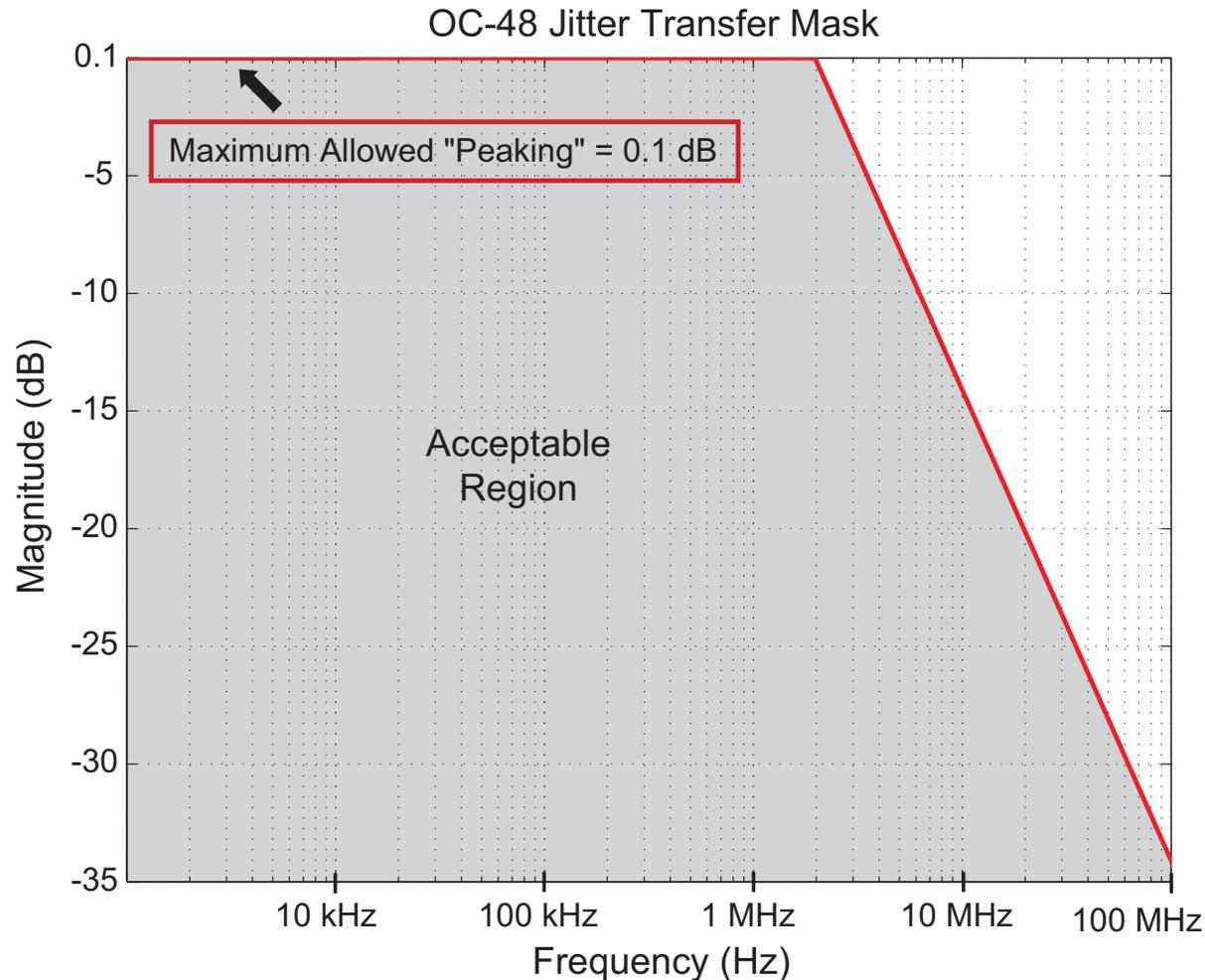
## ■ Definition

- The amount of jitter attenuation that the CDR provides from input to output

## ■ SONET specifies jitter transfer by placing limits on its transfer function behavior from input to output

- Peaking behavior: low frequency portion of CDR transfer function must be less than 0.1 dB
- Attenuation behavior: high frequency portion of CDR transfer function must not exceed a mask limit

# Example Jitter Transfer Mask



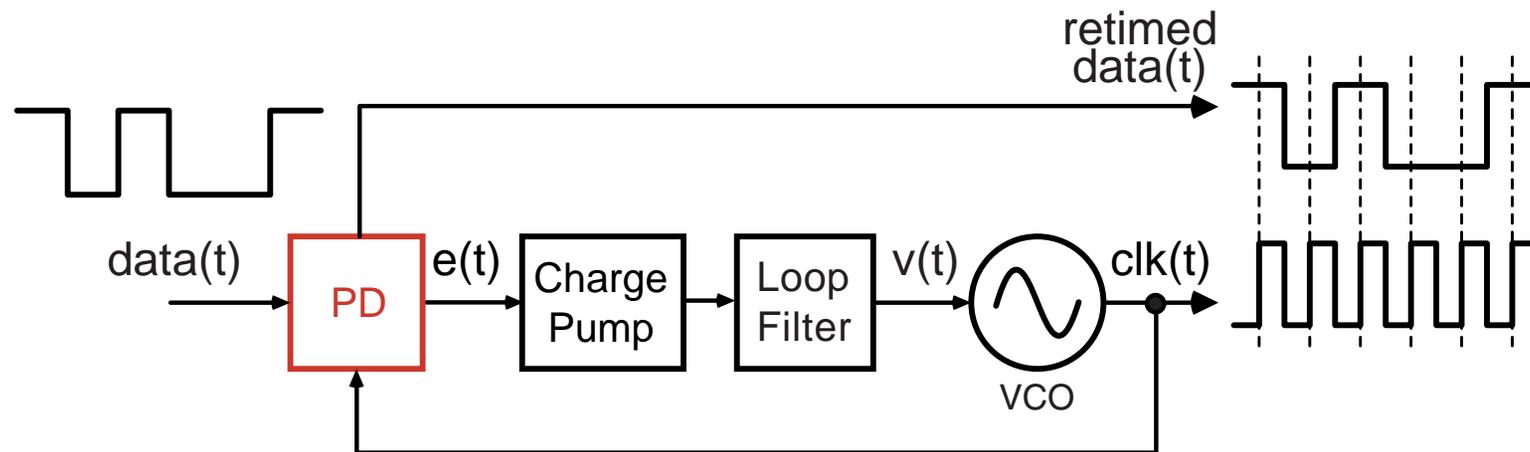
- CDR tested for compliance by adding sine wave jitter at various frequencies and observing the resulting jitter at the CDR output

# Summary of CDR Performance Specifications

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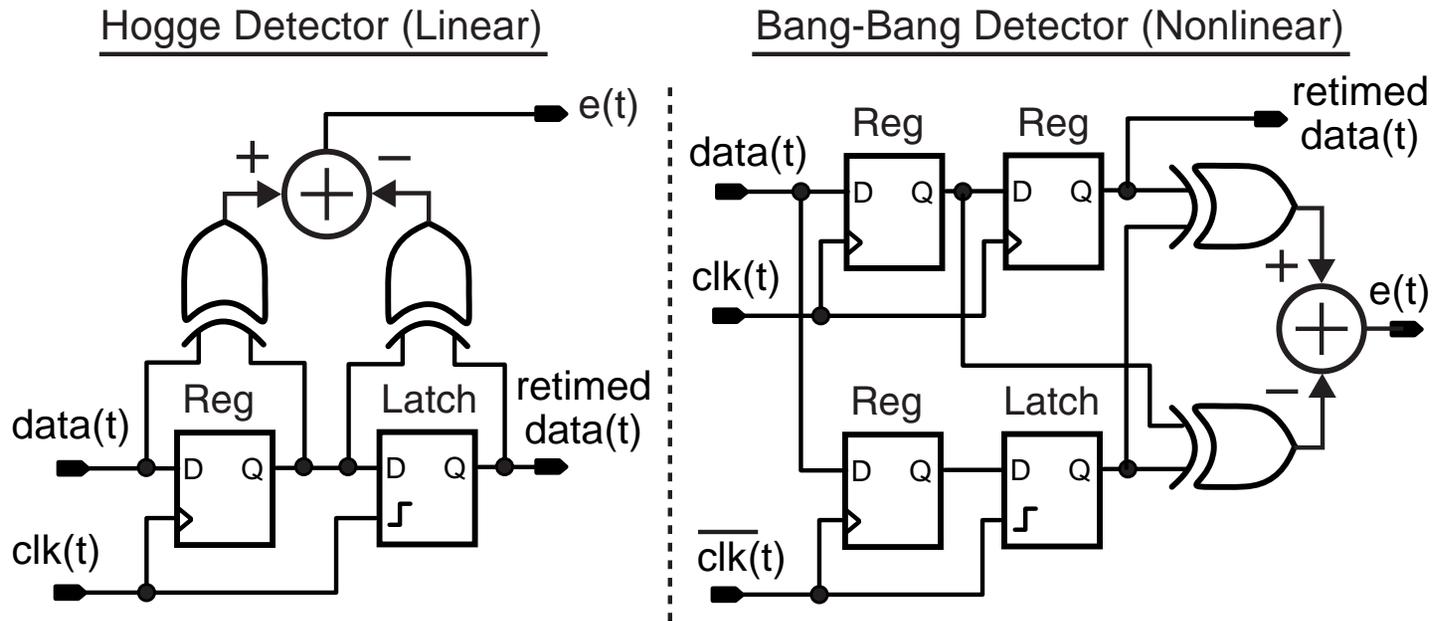
- **Jitter**
  - Jitter generation
  - Jitter tolerance
  - Jitter transfer (and peaking)
- **Acquisition time**
  - Must be less than 10 ms for many SONET systems
- **Bit error rates**
  - Must be less than  $1e-12$  for many SONET systems

# Phase Detectors in Clock and Data Recovery Circuits



- **Key issue**
  - Must accommodate “missing” transition edges in input data sequence
- **Two styles of detection**
  - Linear – PLL can analyzed in a similar manner as frequency synthesizers
  - Nonlinear – PLL operates as a bang-bang control system (hard to rigorously analyze in many cases)

# Popular CDR Phase Detectors



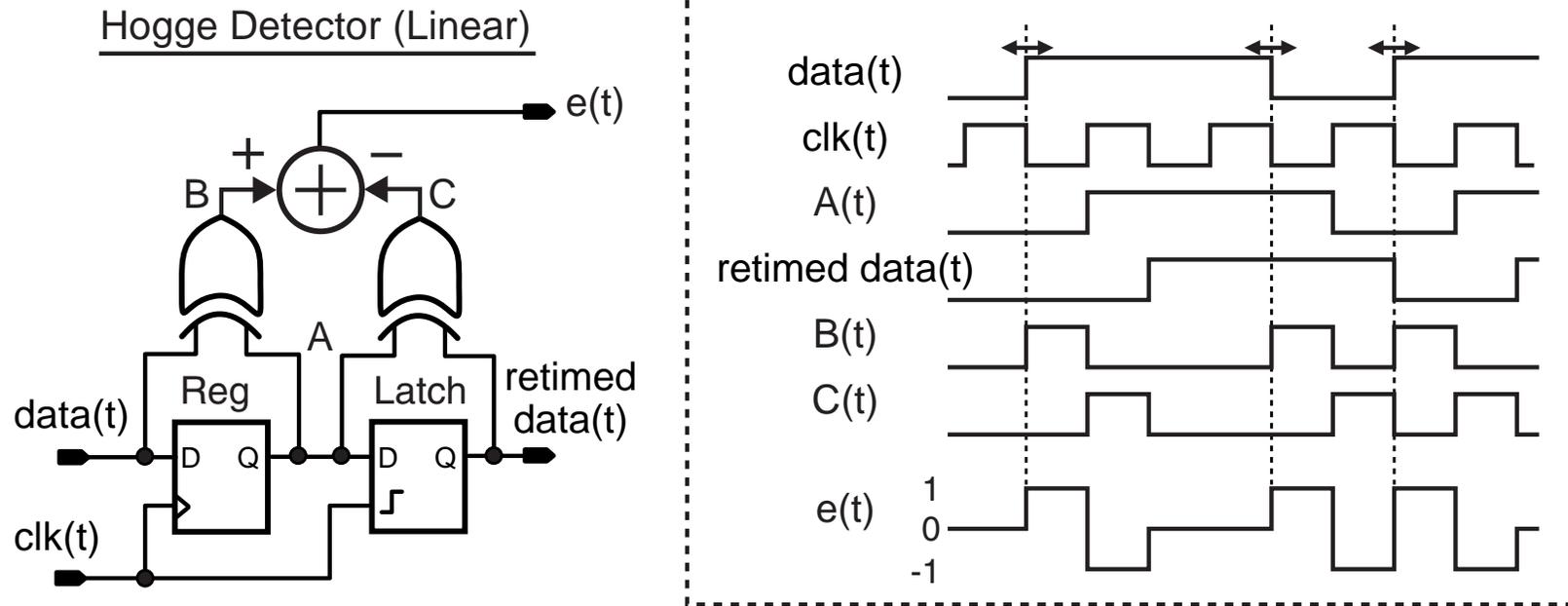
- **Linear**

- Hogge detector produces an error signal that is proportional to the instantaneous phase error

- **Nonlinear**

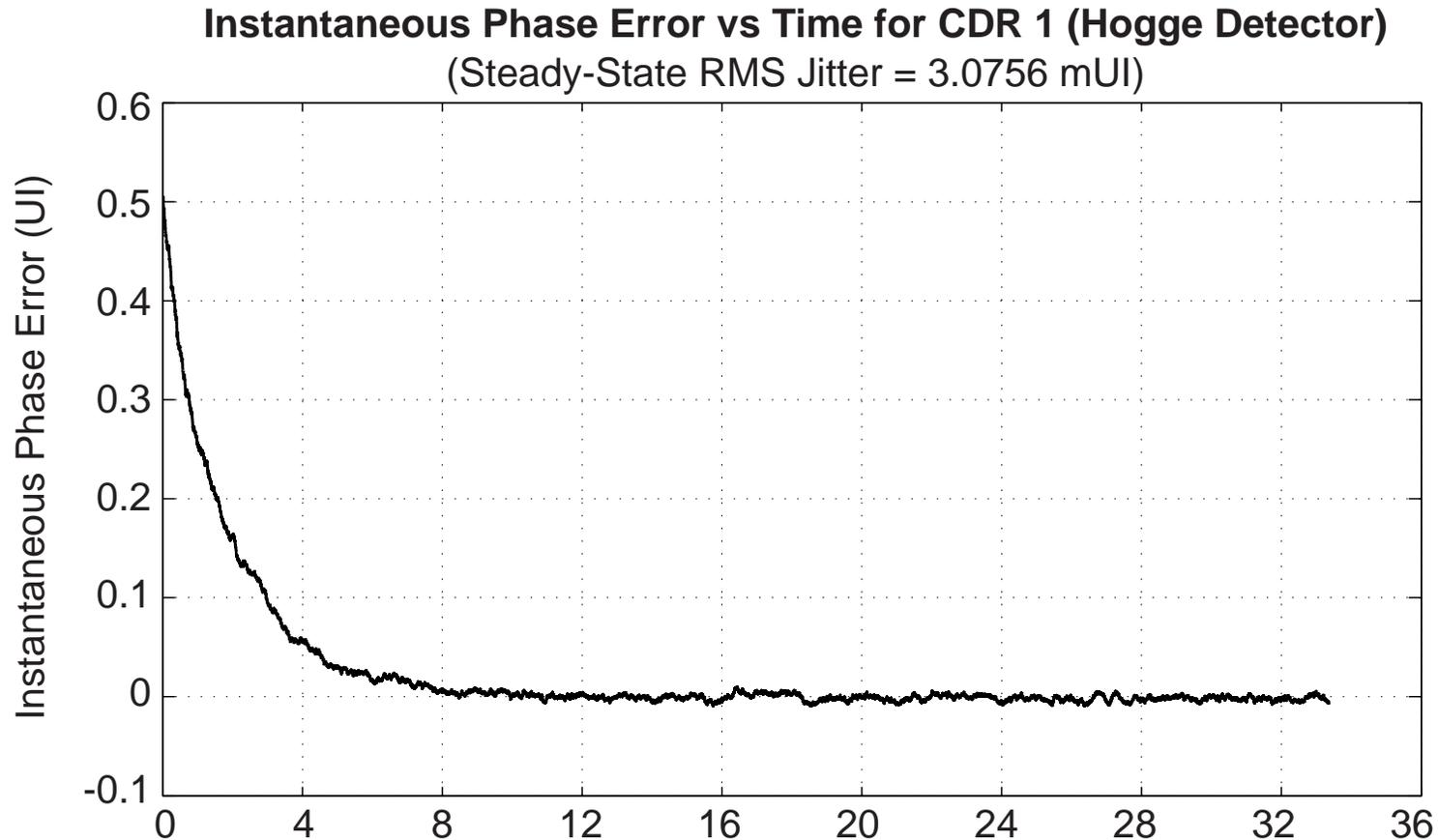
- Alexander (Bang-bang) detector produces an error signal that corresponds to the sign of the instantaneous phase error

# A Closer Look at the Hogge Detector



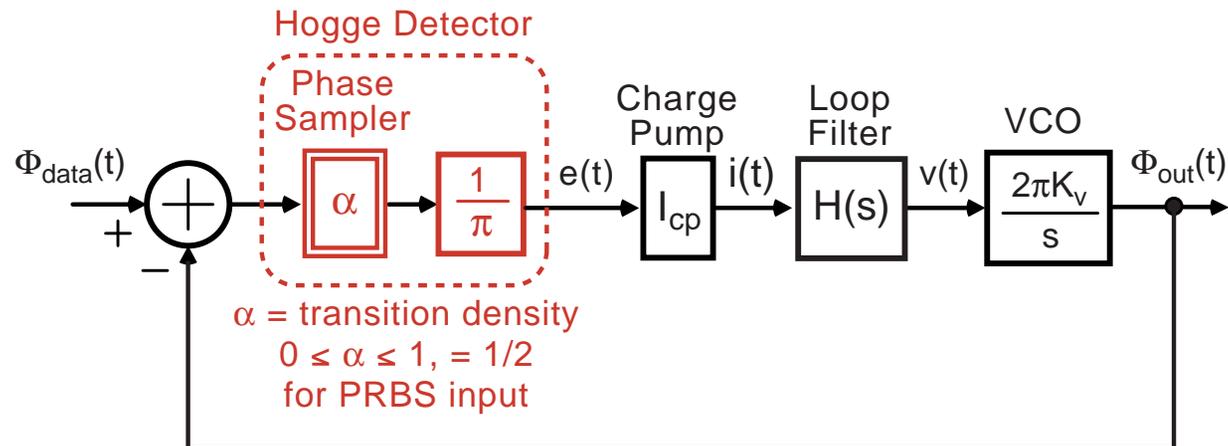
- **Error output,  $e(t)$ , consists of two pulses with opposite polarity**
  - Positive polarity pulse has an area that is proportional to the phase error between the data and clk
  - Negative polarity pulse has a fixed area corresponding to half of the clk period
  - Overall area is zero when data edge is aligned to falling clk edge

# Example CDR Settling Characteristic with Hogge PD



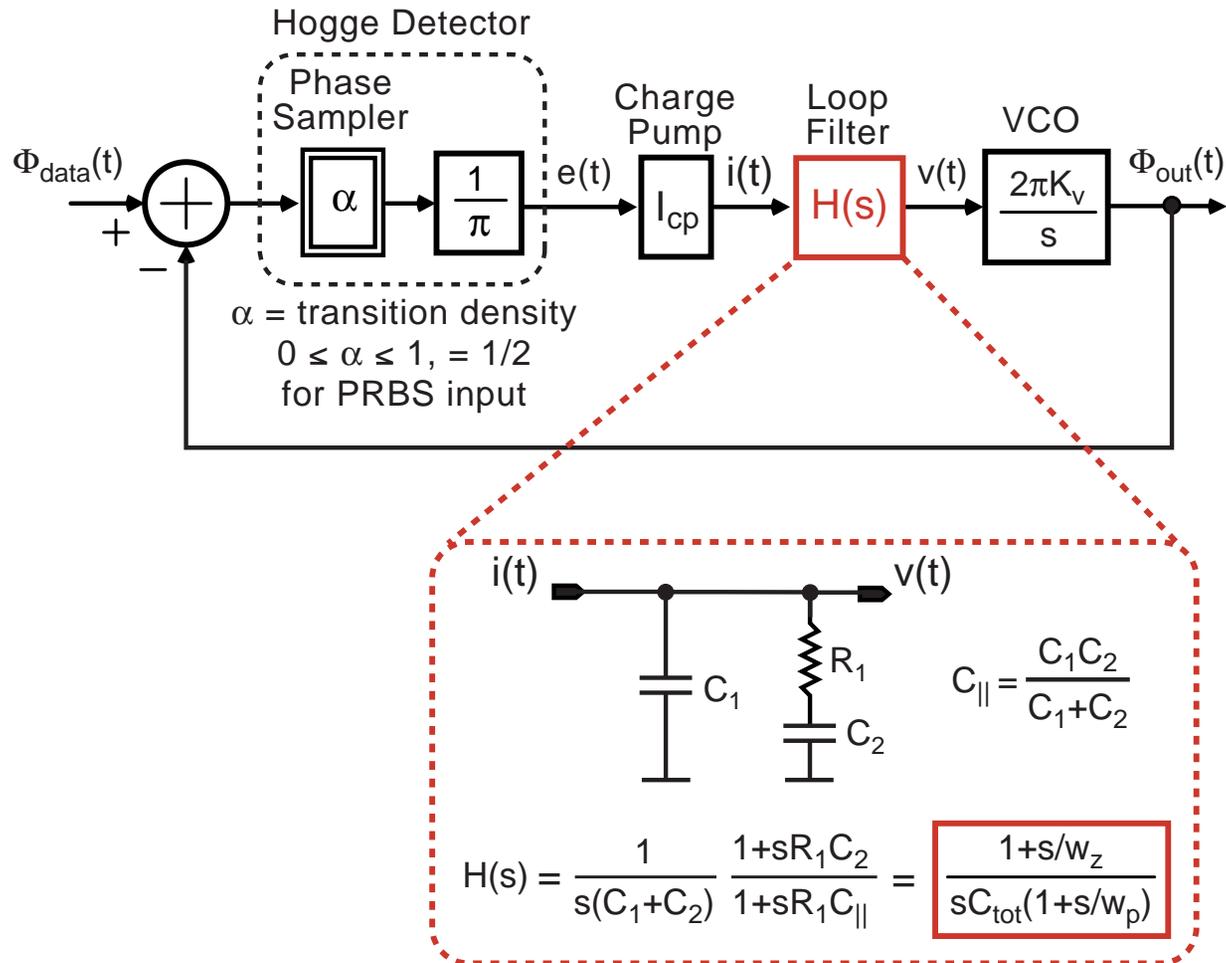
- CDR tracks out phase error with an exponential transition response
- Jitter occurring at steady state is due to VCO and non-idealities of phase detector

# Modeling of CDR with Hogge Detector



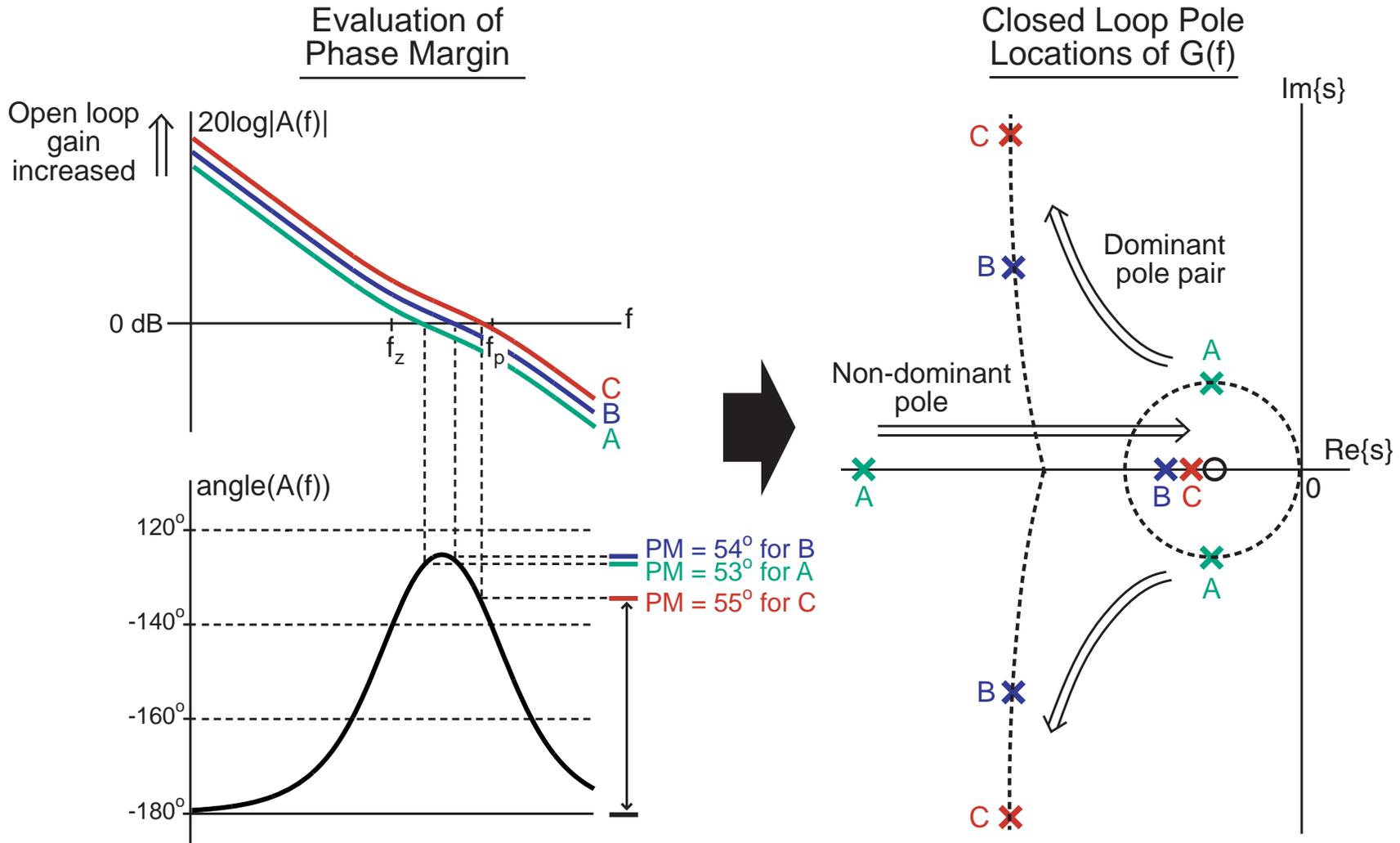
- **Similar to frequency synthesizer model except**
  - No divider
  - Phase detector gain depends on the transition density of the input data
- **The issue of transition density**
  - Phase error information of the input data signal is only seen when it transitions
    - VCO can wander in the absence of transitions
  - Open loop gain (and therefore the closed loop bandwidth) is decreased at low transition densities

# A Common Loop Filter Implementation



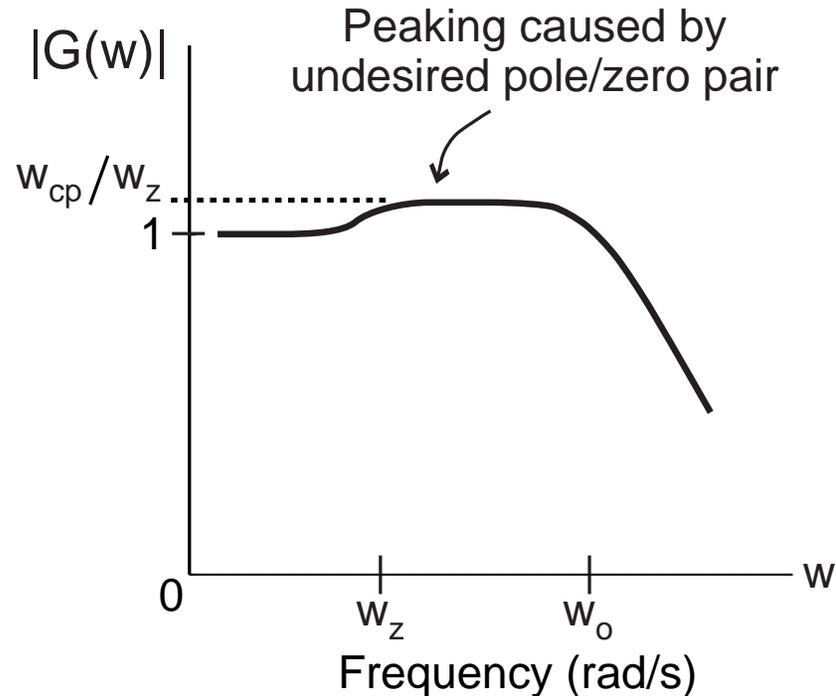
- Use a lead/lag filter to implement a type II loop
  - Integrator in  $H(s)$  forces the steady-state phase error to zero (important to minimize jitter)

# Open Loop Response and Closed Loop Pole/Zeros



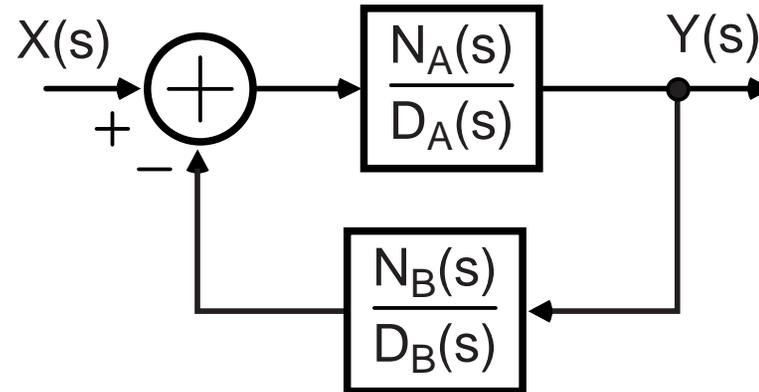
- **Key issue: an undesired pole/zero pair occurs due to stabilizing zero in the lead/lag filter**

# Corresponding Closed Loop Frequency Response



- Undesired pole/zero pair causes peaking in the closed loop frequency response
- SONET demands that peaking must be less than 0.1 dB
  - For classical lead/lag filter approach, this must be achieved by having a very low-valued zero
    - Requires a large loop filter capacitor

## An Interesting Observation



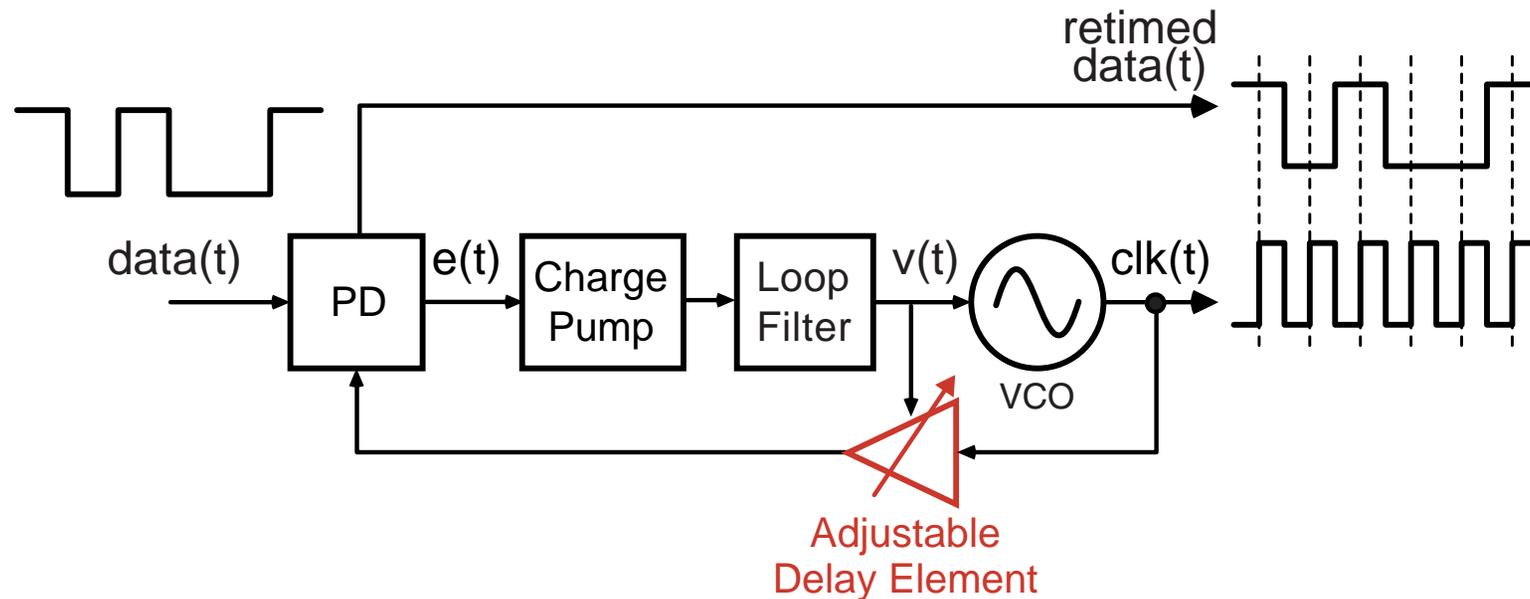
### ■ Calculation of closed loop transfer function

$$\begin{aligned}\frac{Y(s)}{X(s)} &= \frac{N_A(s)/D_A(s)}{1 + N_B(s)/D_B(s) \cdot N_A(s)/D_A(s)} \\ &= \frac{N_A(s)D_B(s)}{D_A(s)D_B(s) + N_B(s)N_A(s)}\end{aligned}$$

### ■ Key observation

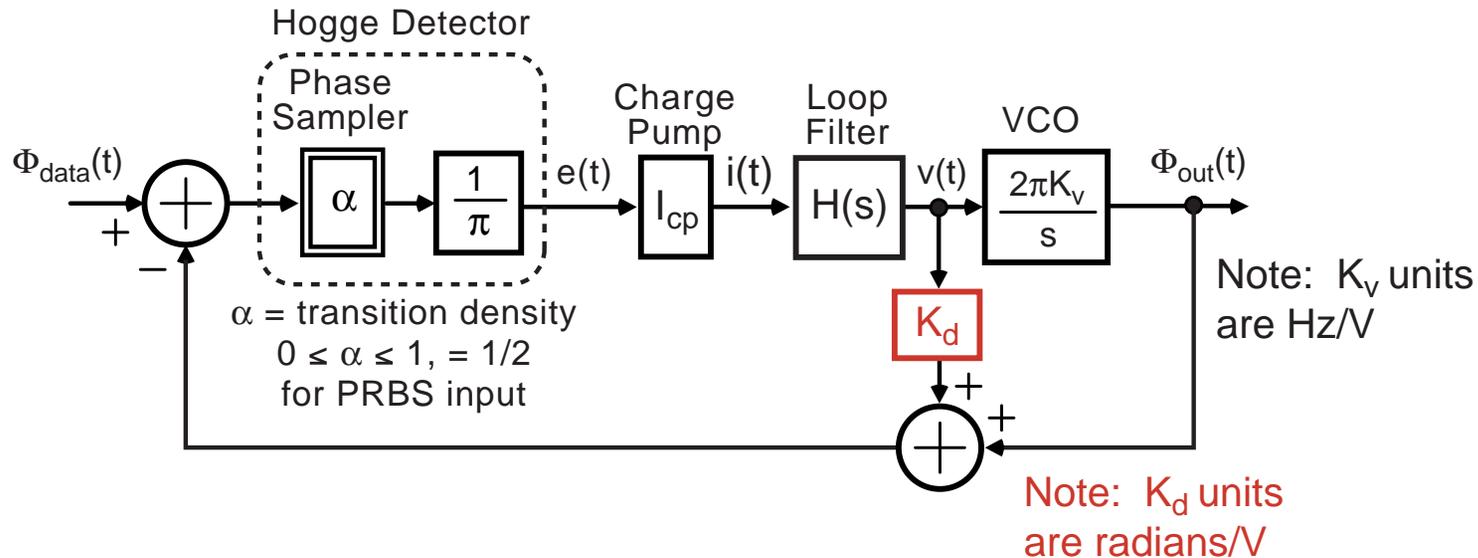
- Zeros in feedback loop do not appear as zeros in the overall closed loop transfer function!

# Method of Achieving Zero Peaking



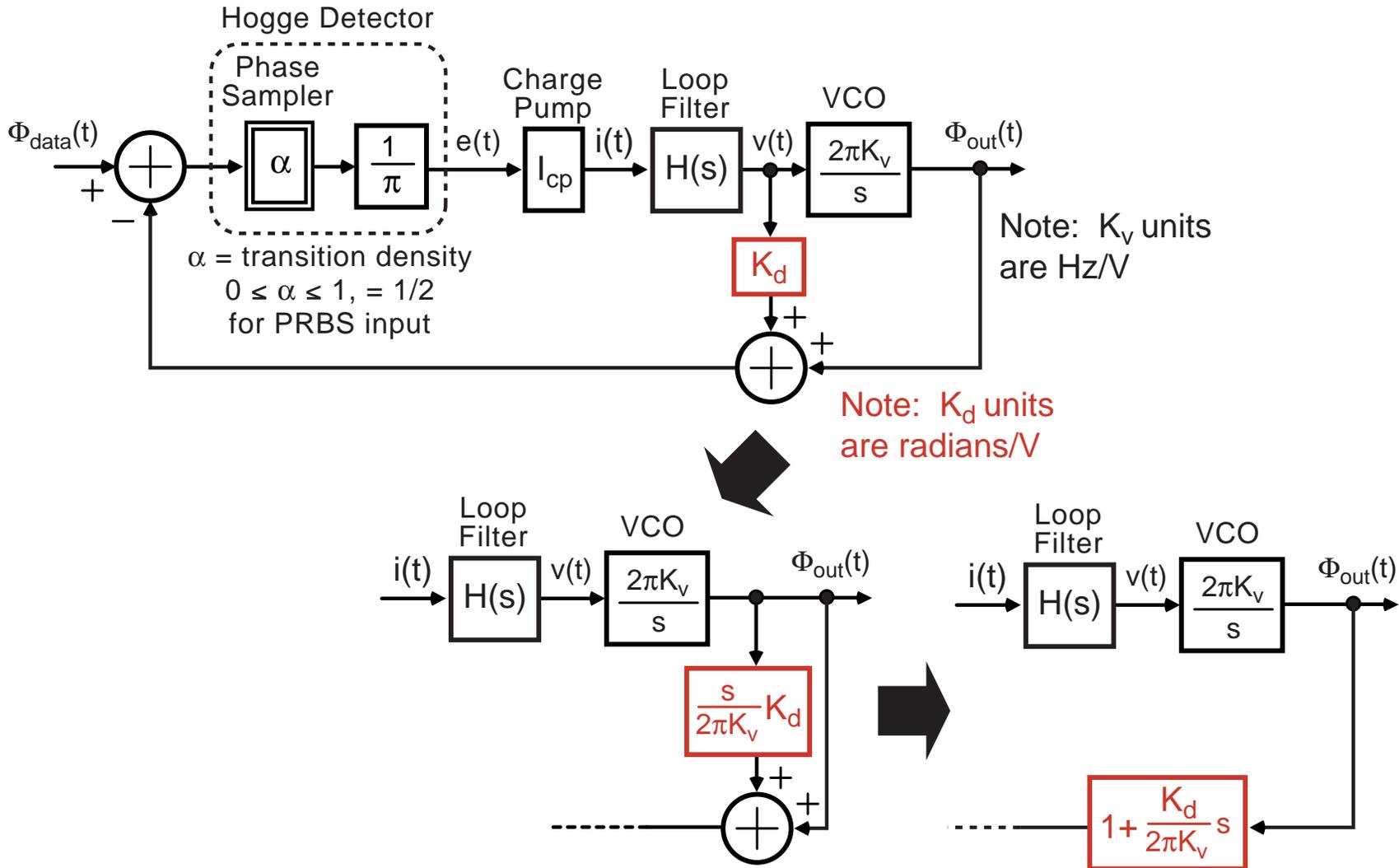
- We can implement a stabilizing zero in the PLL feedback path by using a variable delay element
  - Loop filter can now be implemented as a simple integrator
- Issue: delay must support a large range
- See T.H. Lee and J.F. Bulzacchelli, “A 155-MHz Clock Recovery Delay- and Phase-Locked Loop”, JSSC, Dec 1992

# Model of CDR with Delay Element



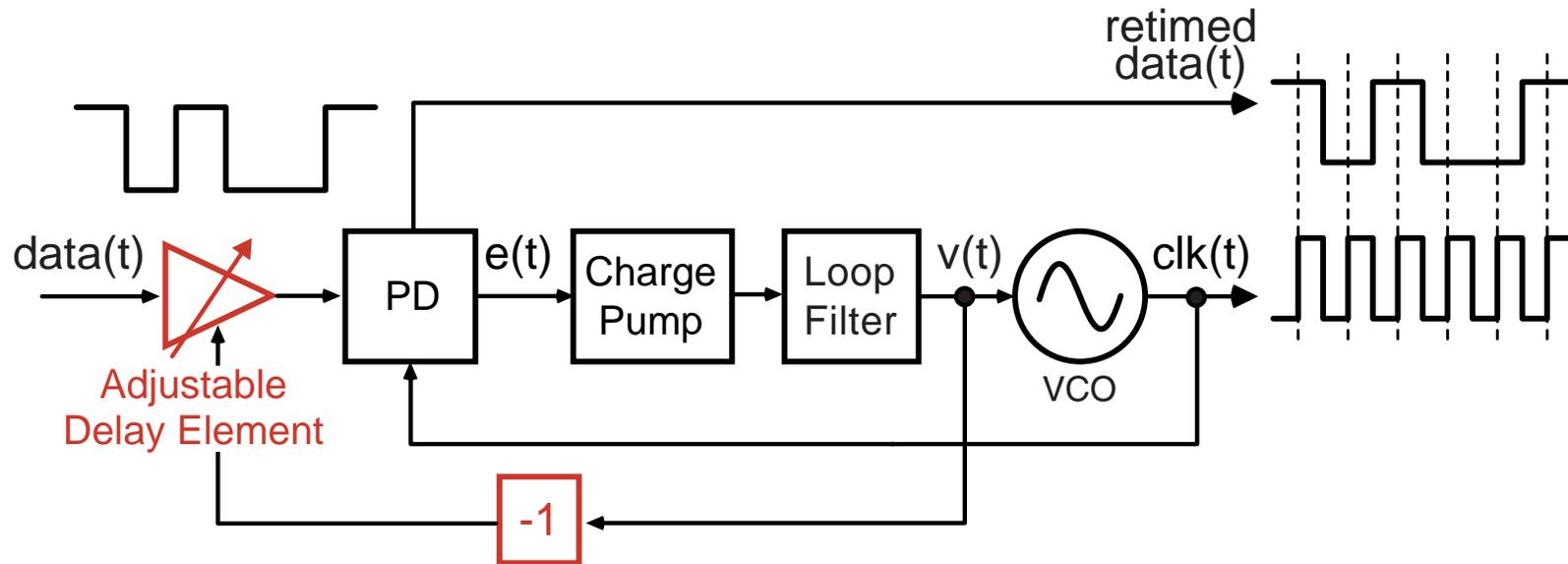
- Delay “gain”,  $K_d$ , is set by delay implementation
- Note that  $H(s)$  can be implemented as a simple capacitor
  - $H(s) = 1/(sC)$

# Derivation of Zero Produced by Delay Element



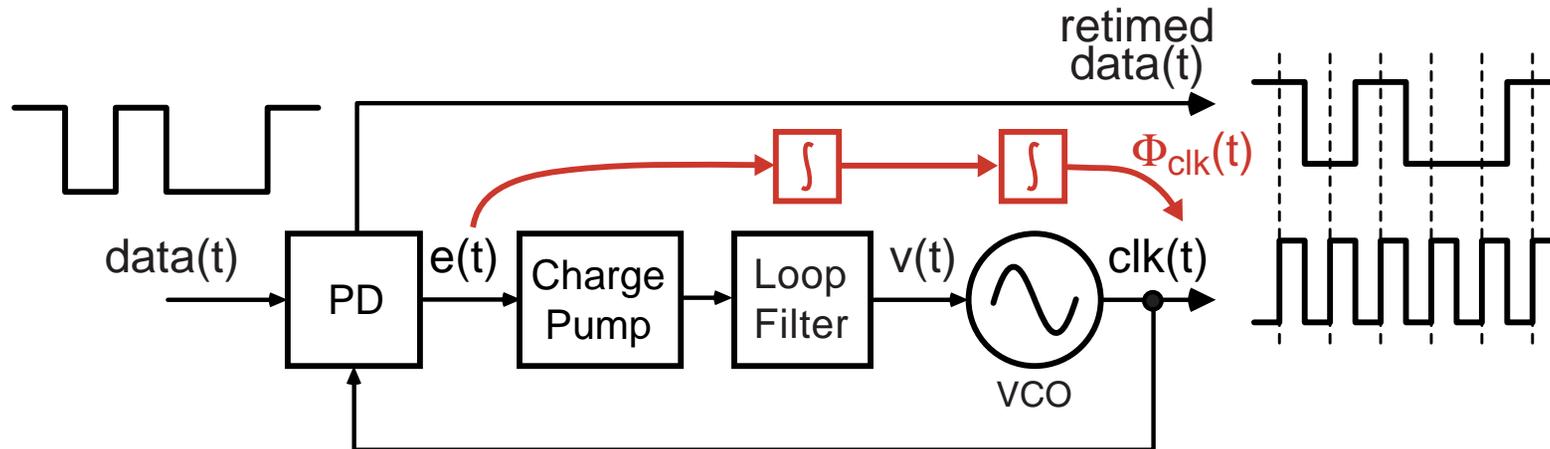
- Zero set by ratio of delay gain to VCO gain

# Alternate Implementation



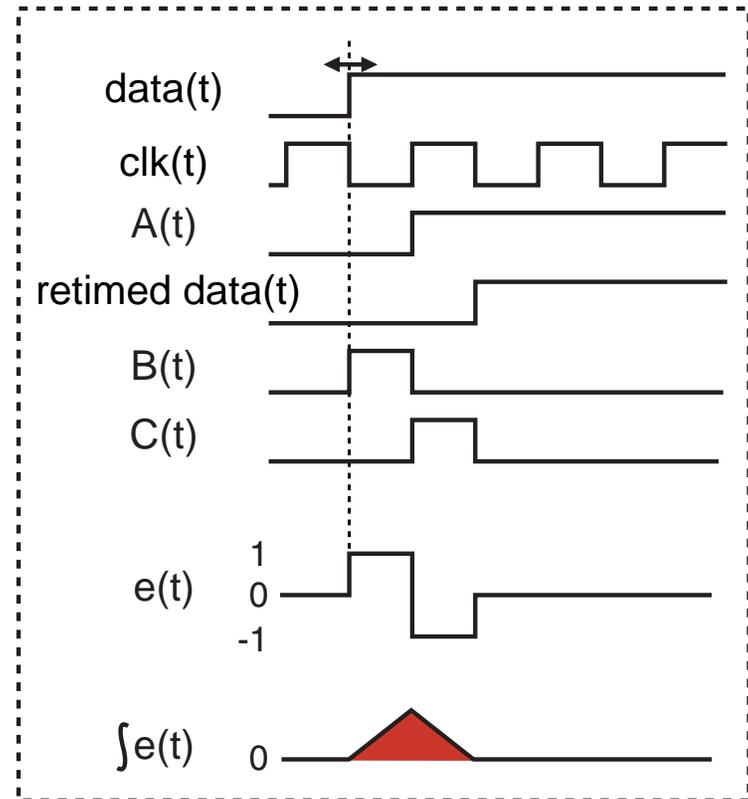
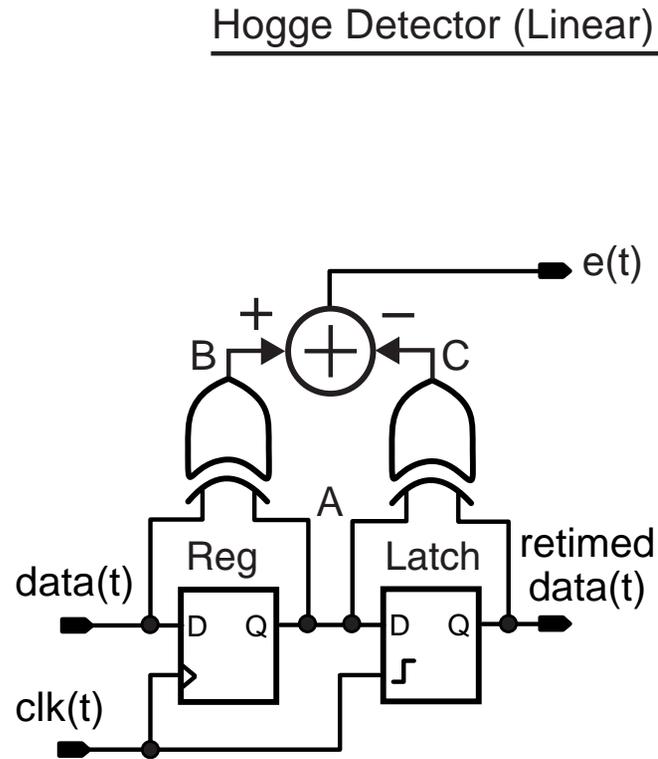
- **Can delay data rather than clk**
  - Same analysis as before

# The Issue of Data Dependent Jitter



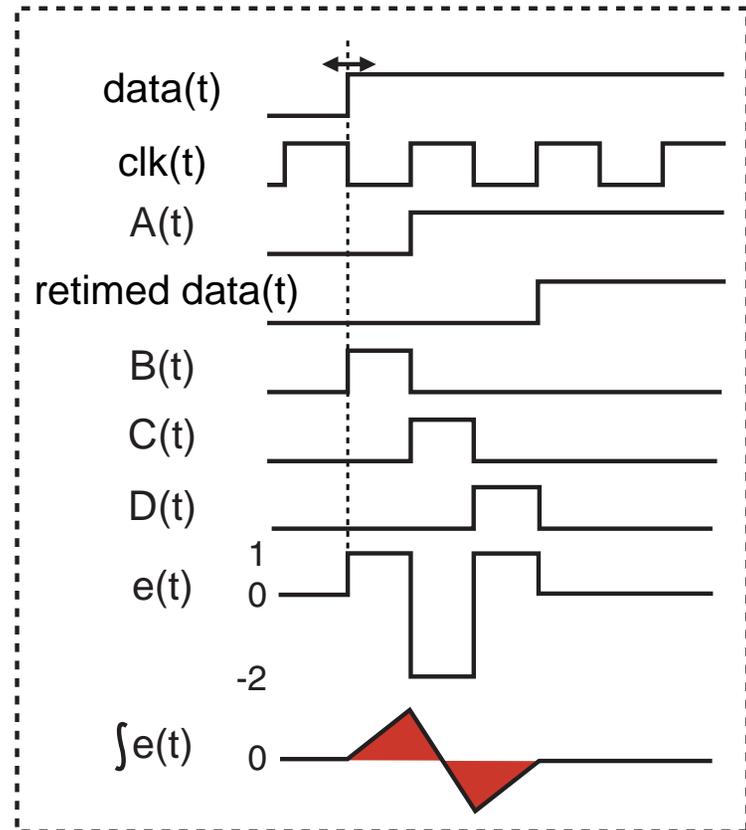
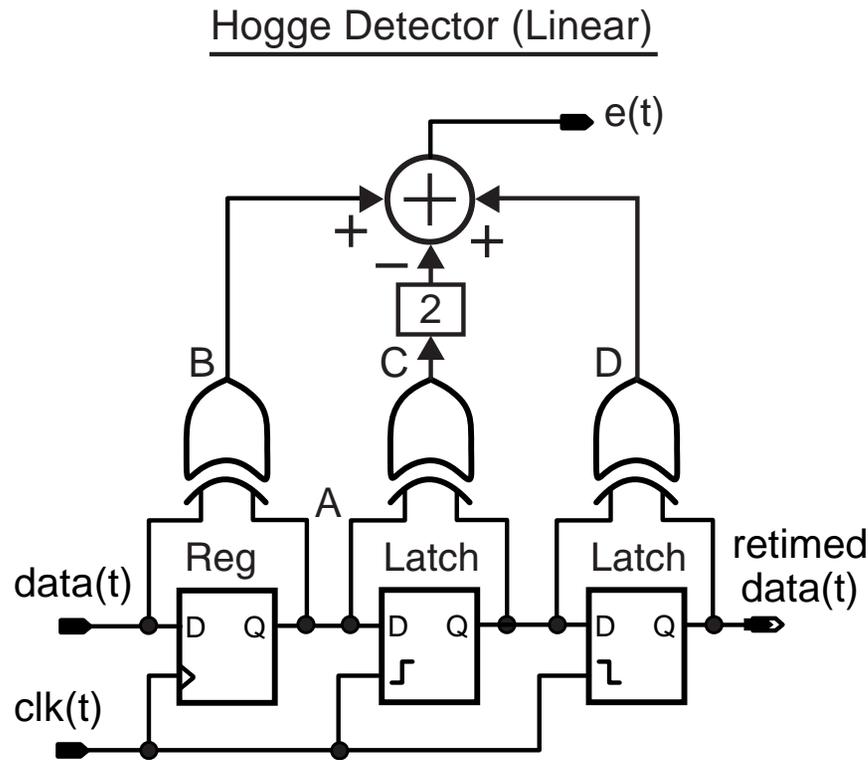
- **For classical or Bulzacchelli CDR**
  - Type II PLL dynamics are employed so that steady state phase detector error is zero
- **Issue: phase detector output influences VCO phase through a double integrator operation**
  - The classical Hogge detector ends up creating data dependent jitter at the VCO output

# Culprit Behind Data Dependent Jitter for Hogge PD



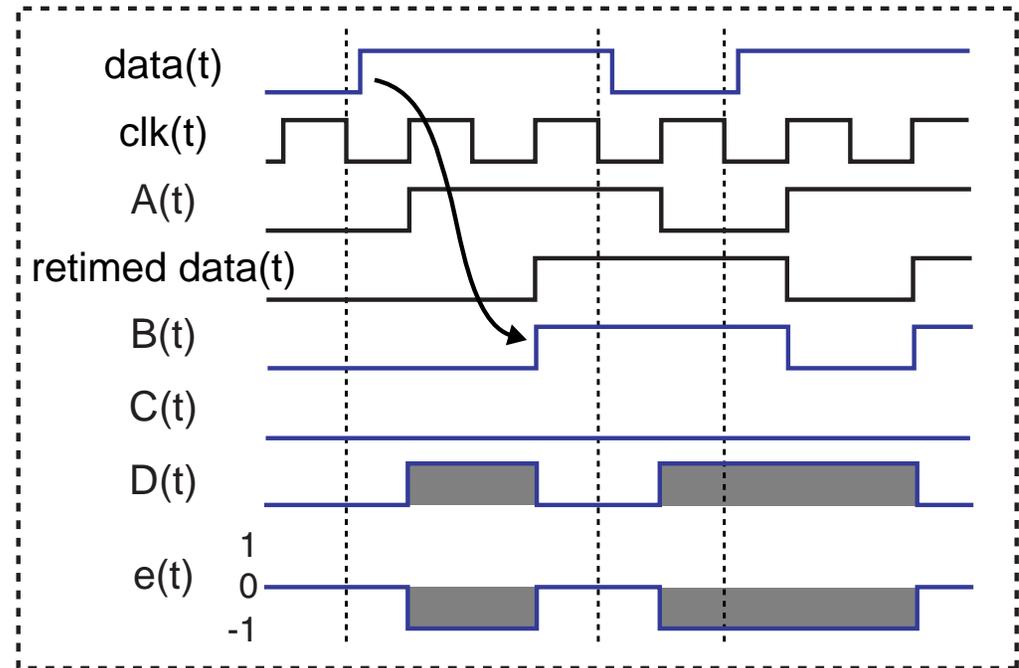
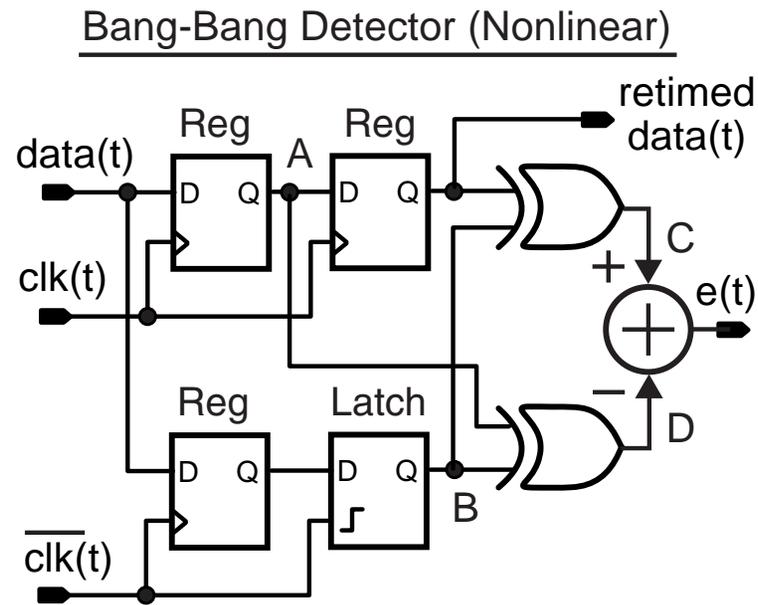
- **The double integral of the  $e(t)$  pulse sequence is nonzero (i.e., has DC content)**
  - Since the data transition activity is random, a low frequency noise source is created
    - Low frequency noise not attenuated by PLL dynamics

# One Possible Fix



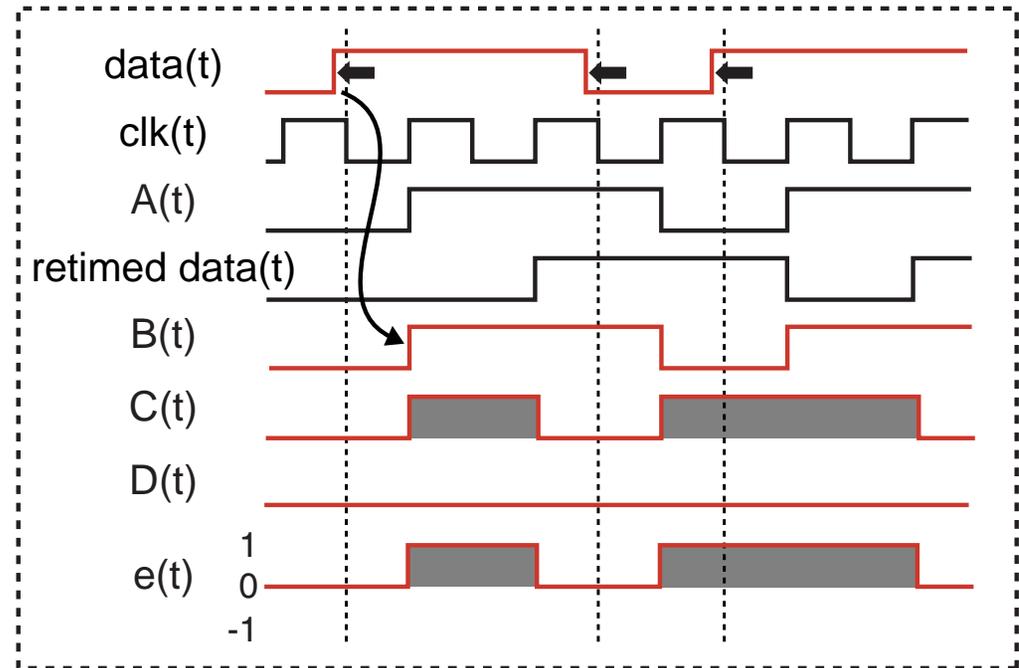
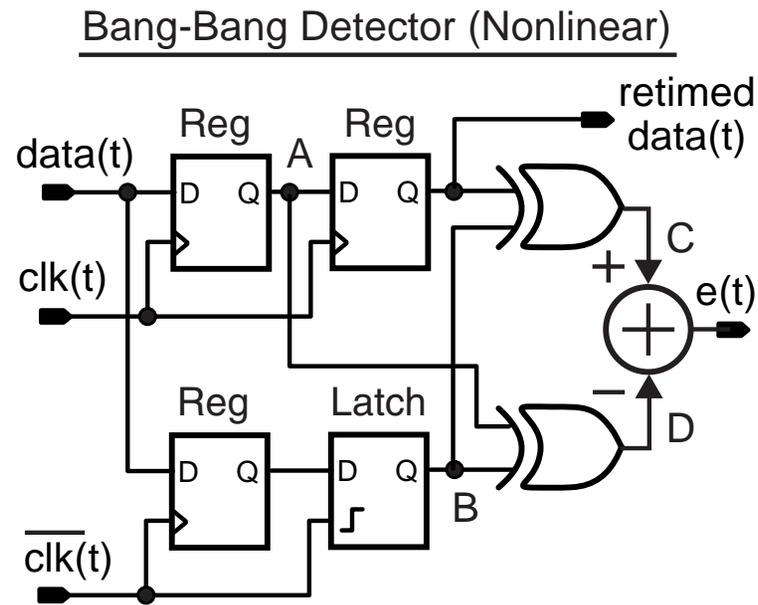
- **Modify Hogge so that the double integral of the e(t) pulse sequence is zero**
  - Low frequency noise is now removed
- **See L. Devito et. al., “A 52 MHz and 155 MHz Clock-recovery PLL”, ISSCC, Feb, 1991**

# A Closer Look at the Bang-Bang Detector



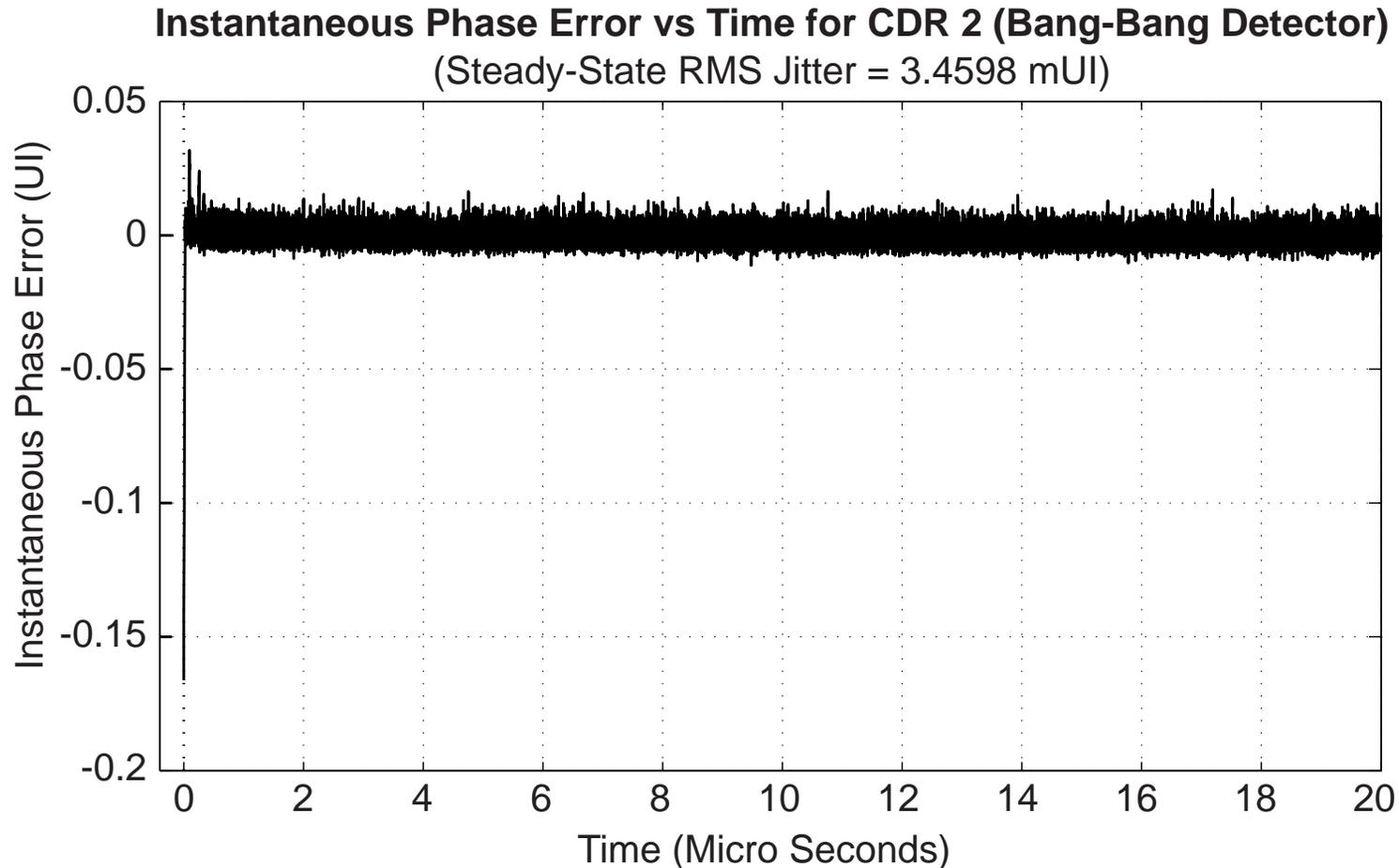
- Error output consists of pulses of fixed area that are either positive or negative depending on phase error
- Pulses occur at data edges
  - Data edges detected when sampled data sequence is different than its previous value
- Above example illustrates the impact of having the data edge *lagging* the clock edge

# A Closer Look at the Bang-Bang Detector (continued)



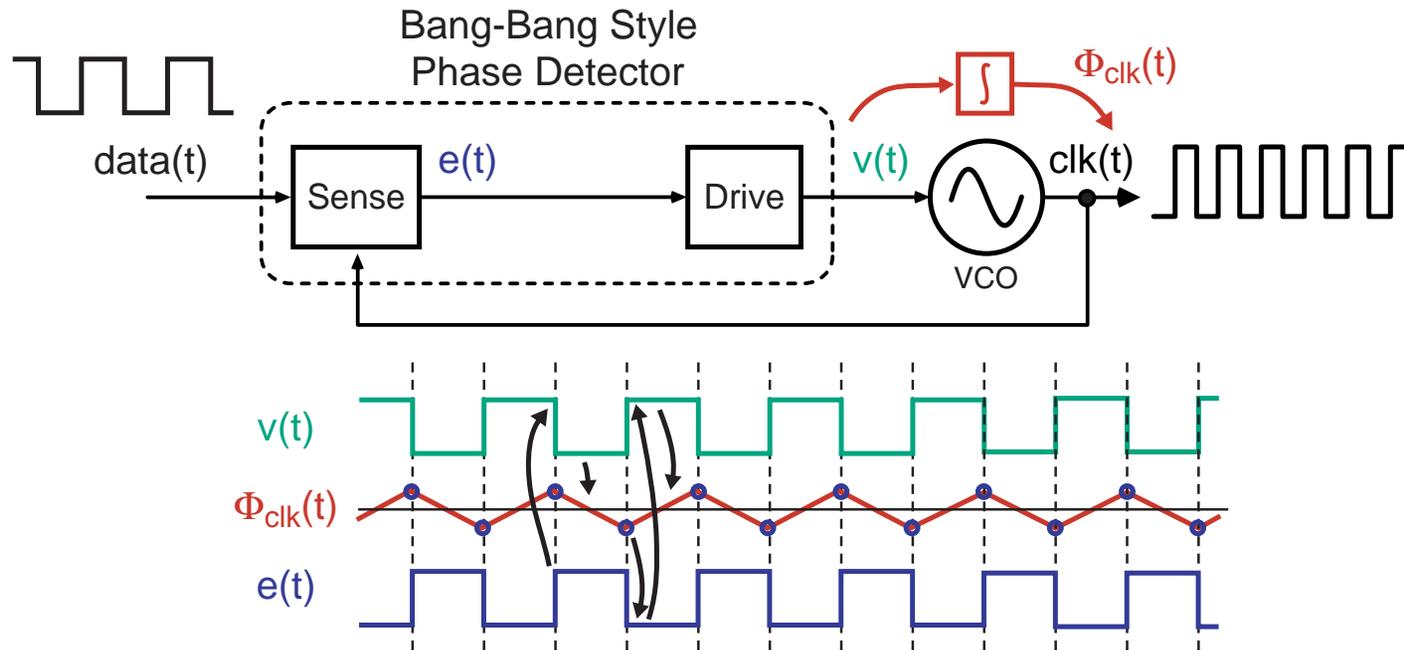
- Above example illustrates the impact of having the data edge *leading* the clk edge
  - Error pulses have opposite sign from lagging edge case

# Example CDR Settling Characteristic with Bang-Bang PD



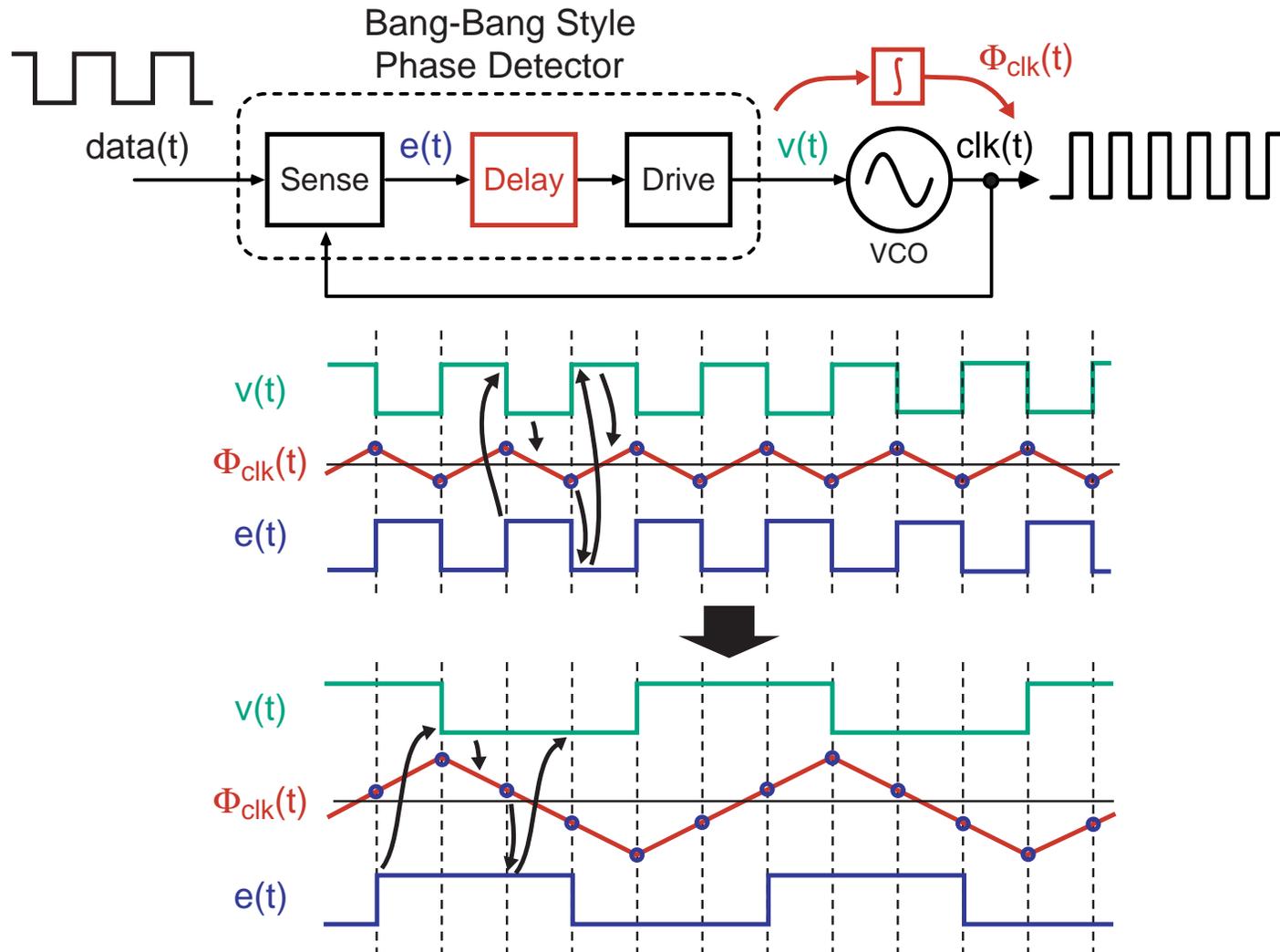
- **Bang-bang CDR response is slew rate limited**
  - Much faster than linear CDR, in general
- **Steady-state jitter often dominated by bang-bang behavior (jitter set by error step size and limit cycles)**

# The Issue of Limit Cycles



- **Bang-bang loops exhibit limit cycles during steady-state operation**
  - Above diagram shows resulting waveforms when data transitions on every cycle
  - Signal patterns more complicated for data that randomly transitions
- **For lowest jitter: want to minimize period of limit cycles**

# The Impact of Delays in a Bang-Bang Loop



- Delays increase the period of limit cycles, thereby increasing jitter

# ***Practical Implementation Issues for Bang-Bang Loops***

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- **Minimize limit cycle periods**
  - Use phase detector with minimal delay to error output
  - Implement a high bandwidth feedforward path in loop filter
    - One possibility is to realize feedforward path in VCO
      - See B. Lai and R.C Walker, “A Monolithic 622 Mb/s Clock Extraction Data Retiming Circuit”, ISSCC, Feb 1991
- **Avoid dead zones in phase detector**
  - Cause VCO phase to wander within the dead zone, thereby increasing jitter
- **Use simulation to examine system behavior**
  - Nonlinear dynamics can be non-intuitive
  - For first order analysis, see R.C. Walter et. al., “A Two-Chip 1.5-GBd Serial Link Interface”, JSSC, Dec 1992