Analysis and Design of Analog Integrated Circuits
Lecture 7

Differential Amplifiers

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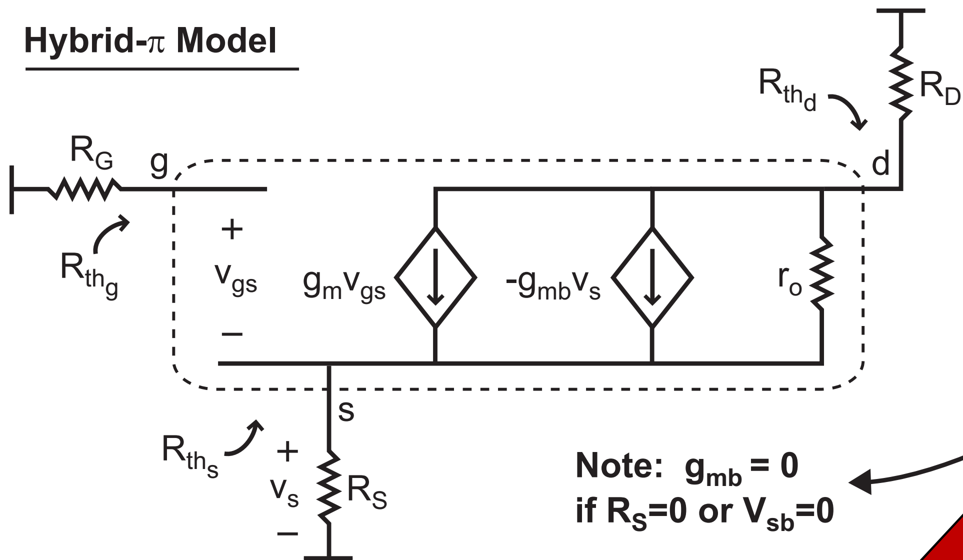
Review Proposed Thevenin CMOS Transistor Model

Hybrid-π Model

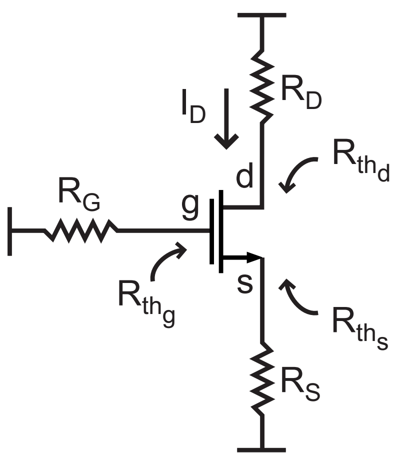


Note: $g_{mb} = 0$ if R_S=0 or V_{sb}=0

Key Small-Signal Parameters

Parameter	Strong Inversion	Weak Inversion
g_m	$\sqrt{2\mu_n C_{ox}(W/L) I_D}$	$\frac{qI_D}{nkT}$
g_{mb}	$\frac{\gamma g_m}{2\sqrt{2\lvert\Phi_F\rvert + V_{SB}}}$	$\frac{(n-1)qI_D}{nkT}$
r_o	$\frac{1}{\lambda I_D}$	$\frac{1}{\lambda I_D}$

Thevenin Resistances



Exact

$R_{th_d} = r_o(1+(g_m+g_{mb})R_S)+R_S$

R_{th_g} = infinite

$R_{th_s} = (1+R_D/r_o)\left(r_o \,\Big\|\, \frac{1}{g_m+g_{mb}}\right)$

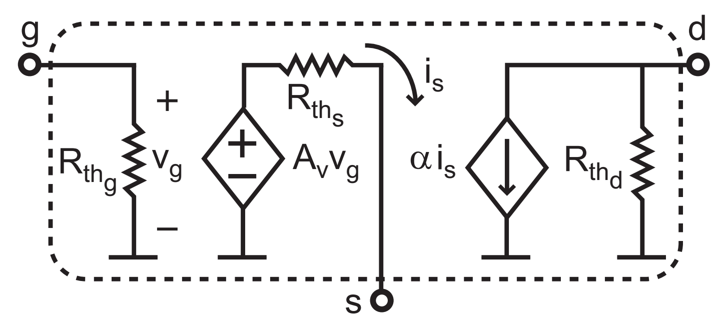
Approximation
($g_{mb} << g_m$, $g_m r_o >> 1$)

$R_{th_d} = r_o(1+g_m R_S)$

R_{th_g} = infinite

$R_{th_s} = \frac{1+R_D/r_o}{g_m} \approx \frac{1}{g_m}$ **($R_D << r_o$)**

Proposed Small Signal Transistor Model



Exact

$A_v = g_m r_o \,\Big\|\, \frac{g_m}{g_m+g_{mb}}$

$\alpha = 1+R_D/R_{th_d}$

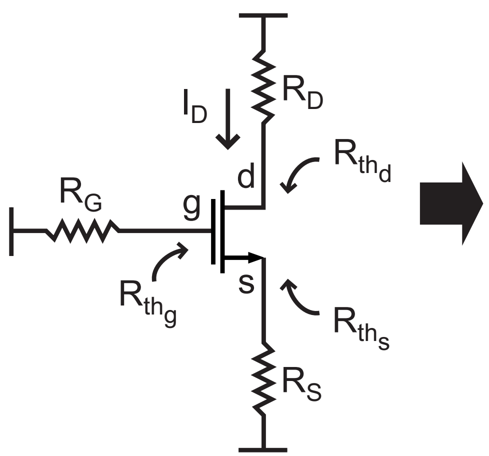
Approximation

$A_v = 1$ **($g_{mb}<<g_m$, $g_m r_o>>1$)**

$\alpha = 1$ **($R_D<<R_{th_d}$)**

Key Observations

Thevenin Resistances



Exact

$R_{th_d} = r_o(1+(g_m+g_{mb})R_S)+R_S$

R_{th_g} = infinite

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Approximation ($g_{mb} << g_m$, $g_m r_o >> 1$)

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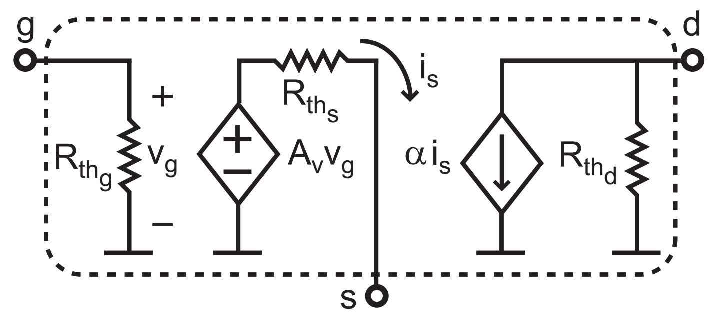
R_{th_g} = infinite

$R_{th_s} = \frac{1+R_D/r_o}{g_m} \approx \frac{1}{g_m}$ **($R_D << r_o$)**

Proposed Small Signal Transistor Model



Exact

$A_v = g_m r_o \,\Big|\Big|\, \frac{g_m}{g_m+g_{mb}}$

$\alpha = 1+R_D/R_{th_d}$

Approximation

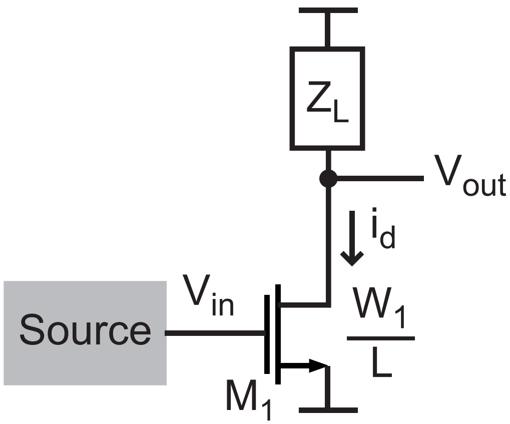
$A_v = 1$ **($g_{mb} << g_m$, $g_m r_o >> 1$)**

$\alpha = 1$ **($R_D << R_{th_d}$)**

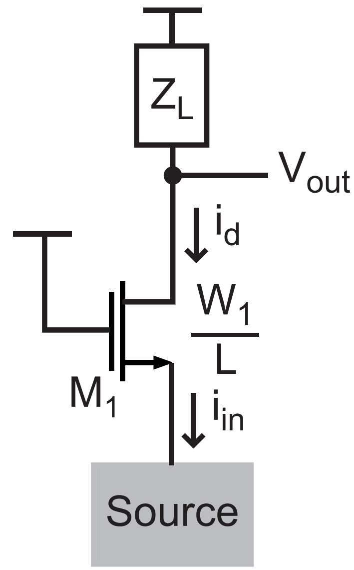
- **For calculations focusing on signal flow from gate or source to the drain**
  - **Observe that current through R_d equals i_s**
    - True since $\alpha * R_{thd}/(R_d + R_{thd}) = 1$
    - You can avoid doing calculations involving α or R_{thd}
- **For calculations focusing on signal flow from the drain**
  - **Drain simply looks like impedance R_{thd}**

Basic Single-Stage Amplifiers and Current Mirrors

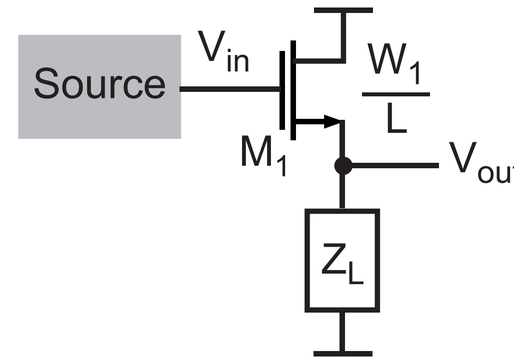
Common Source



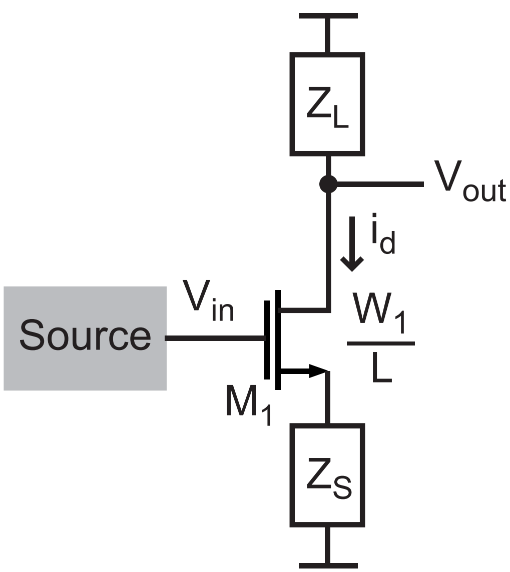
Common Gate



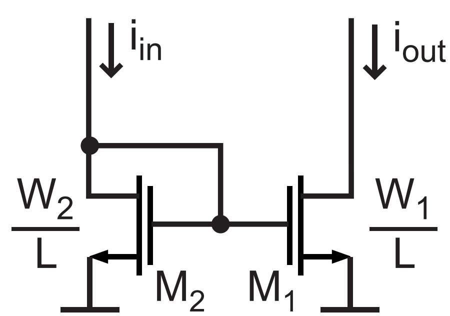
Source Follower



Common Source with Source Degeneration

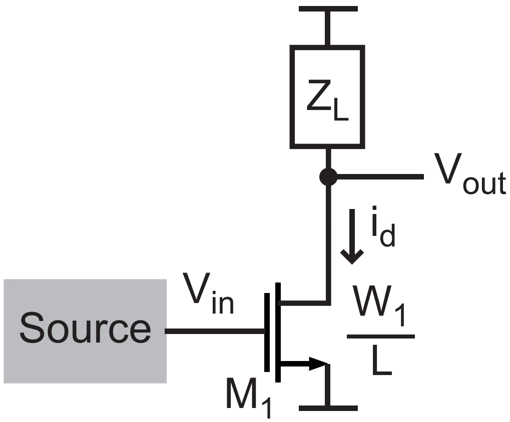


Current Mirror

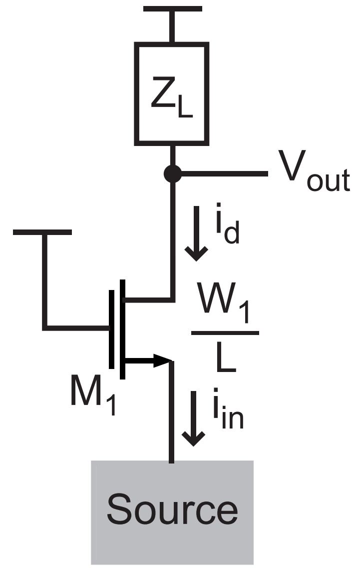


Today We Will Look At Differential Amplifiers

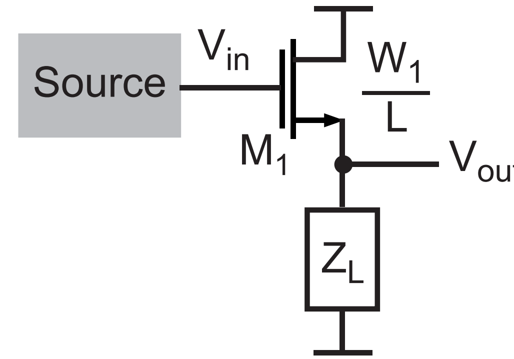
Common Source



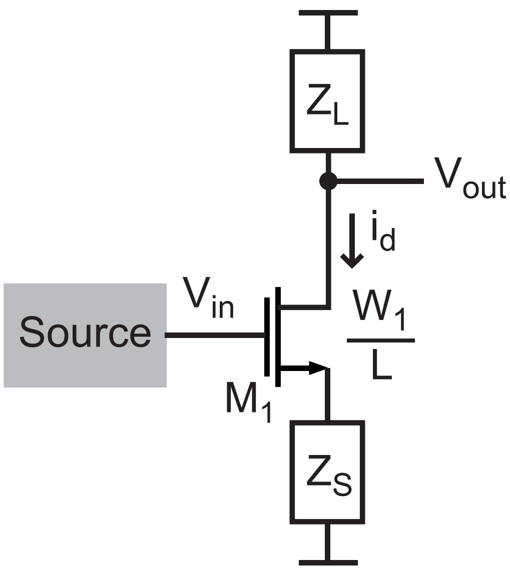
Common Gate



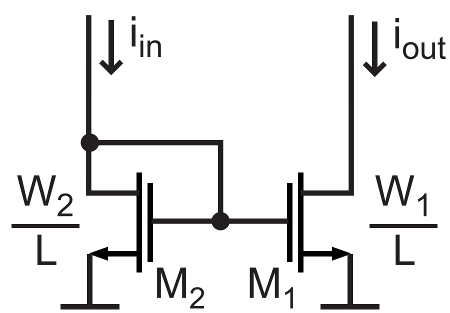
Source Follower



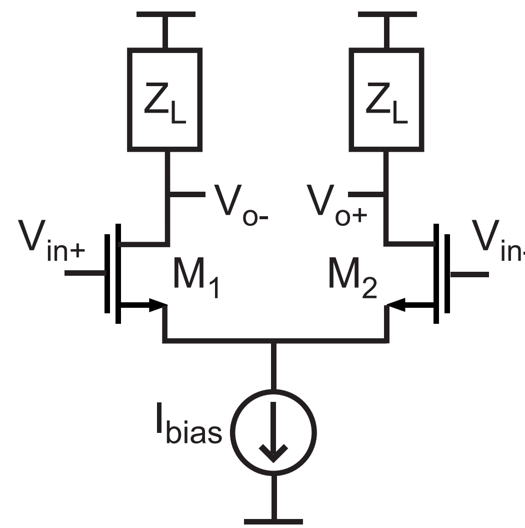
Common Source with Source Degeneration



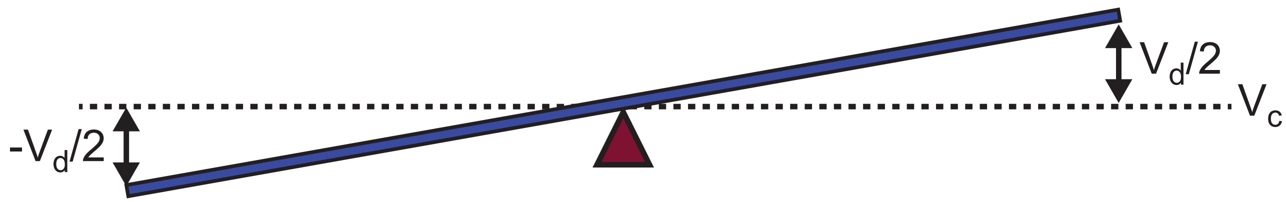
Current Mirror



Differential Amplifier



Differential and Common Mode Signals



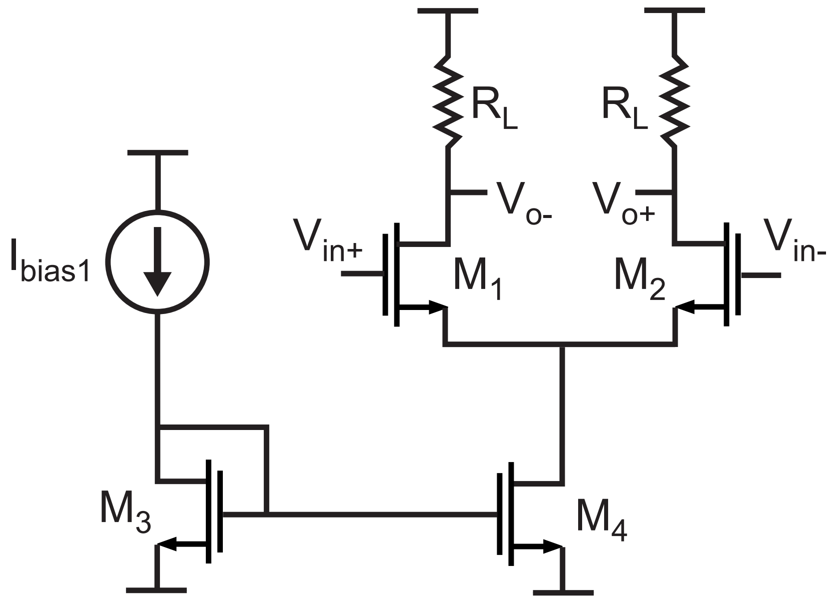
- **Consider positive and negative input terminal signals V_i^+ and V_i^-**
- **Define differential signal as:** $V_{id} = V_{in}^+ - V_{in}^-$
- **Define common mode signal as:** $V_{ic} = (V_{in}^+ + V_{in}^-)/2$
- **We can create arbitrary V_i^+ and V_i^- signals from differential and common mode components:**

$$V_{in}^+ = V_{ic} + \frac{1}{2}V_{id} \qquad V_{in}^- = V_{ic} - \frac{1}{2}V_{id}$$

- **This also applies to differential output signals:**

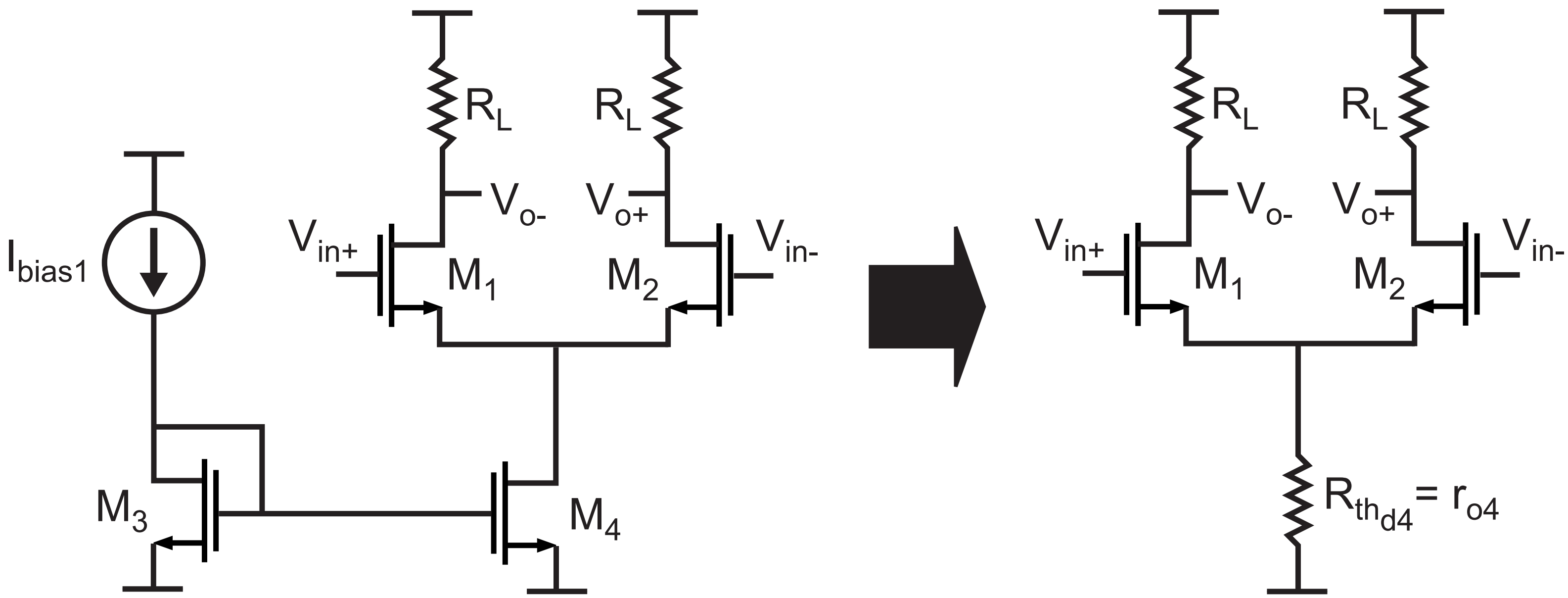
$$V_o^+ = V_{oc} + \frac{1}{2}V_{od} \qquad V_o^- = V_{oc} - \frac{1}{2}V_{od}$$

Differential Amplifier



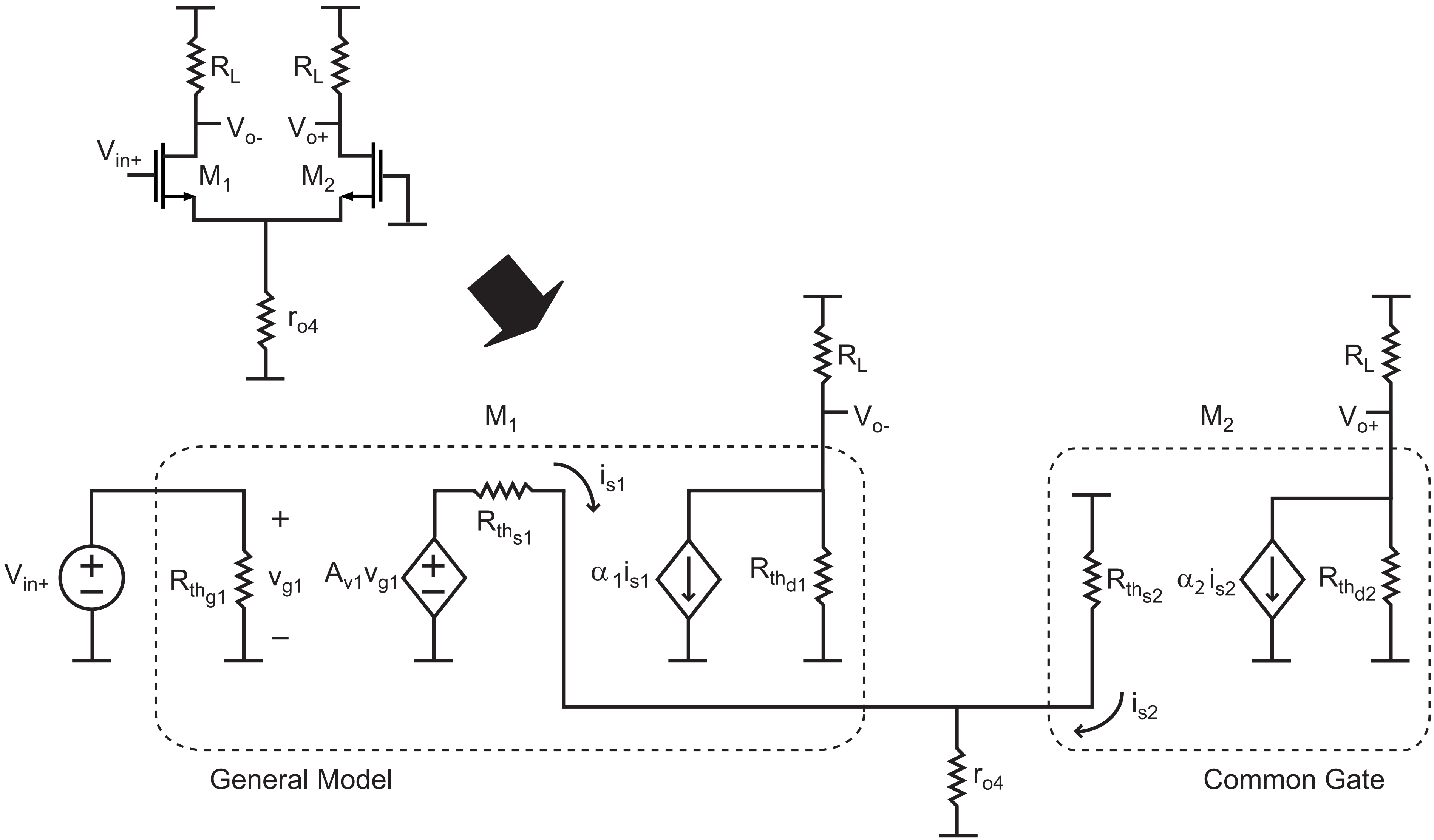
- **Useful for amplifying signals in the presence of noise**
  - **Common-mode noise is rejected**
- **Useful for high speed digital circuits**
  - **Low voltage swing allows faster gate/buffer performance**

First Steps in Small Signal Modeling



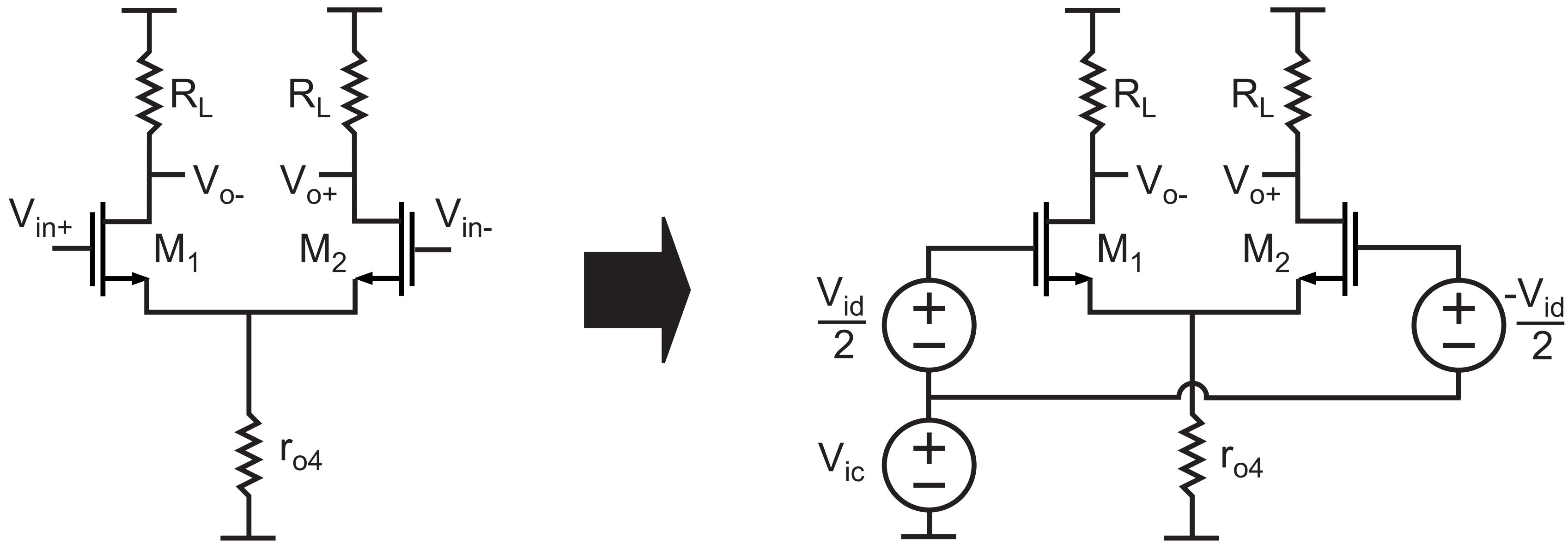
- **Small signal analysis assumes linearity**
  - **Impact of M_4 on amplifier is to simply present its drain impedance to the diff pair transistors (M_1 and M_2)**
  - **Impact of V_{in+} and V_{in-} can be evaluated separately and then added (i.e., superposition)**
    - By symmetry, we need only determine impact of V_{in+}
      - Calculation of V_{in-} impact directly follows

Calculate Impact of V_{in+} using Thevenin Models



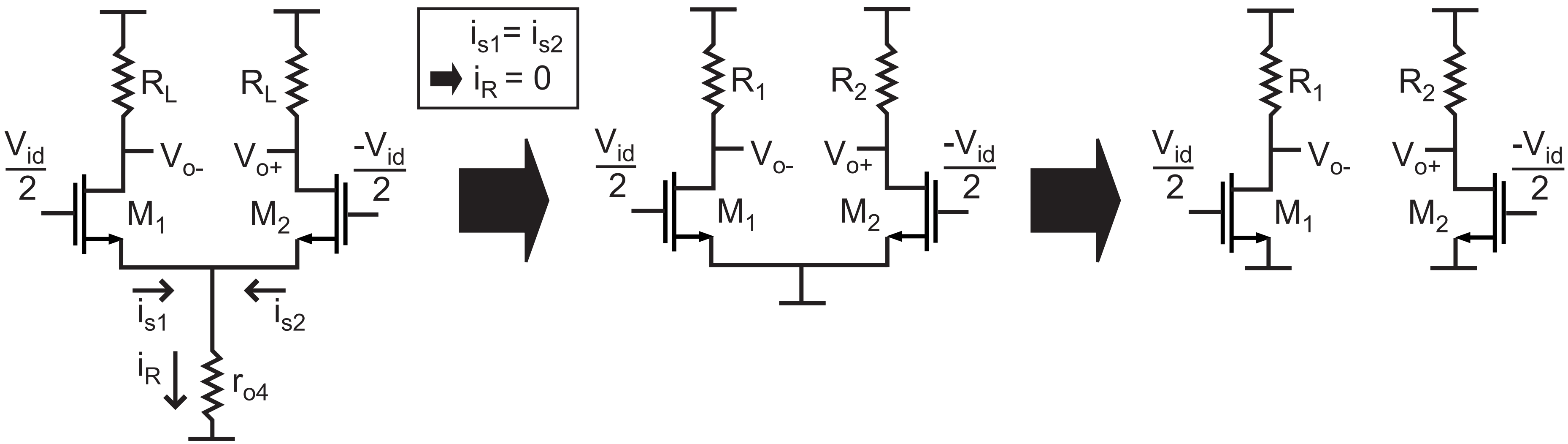
- **Analysis follows fairly easily, but there is a simpler way!**

Method 2 of Differential Amplifier Analysis



- **Partition input signals into common-mode and differential components**
- **By superposition, we can add the results to determine the overall impact of the input signals**

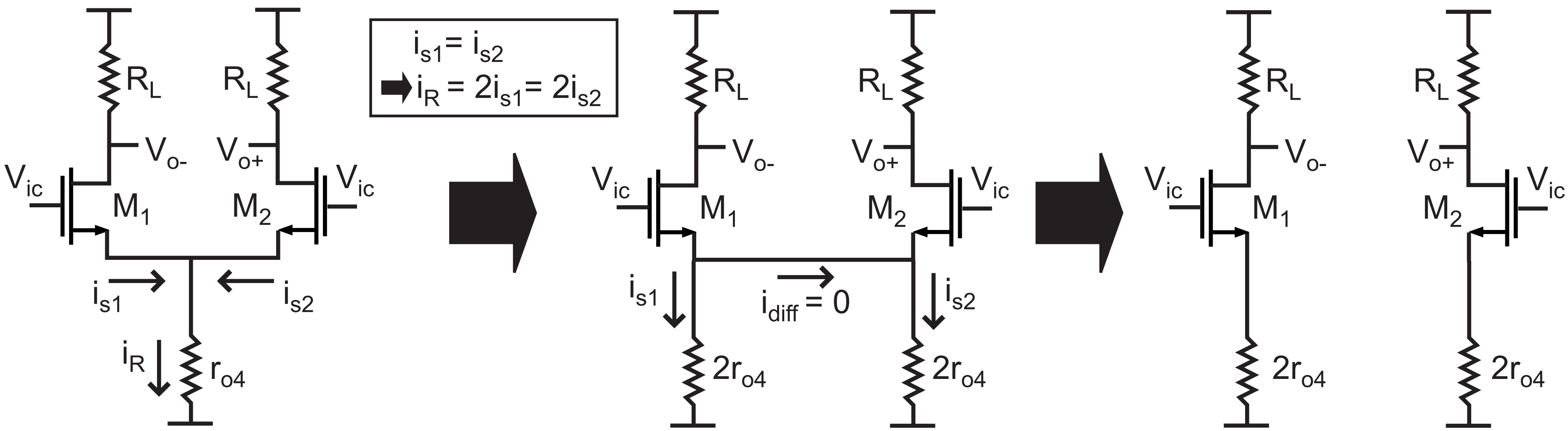
Differential Analysis



- **Key observations**
  - **Inputs are equal in magnitude but opposite in sign to each other**
  - **By linearity and symmetry, i_{s1} must equal $-i_{s2}$**
    - This implies i_R is zero, so that voltage drop across r_{o4} is zero
      - The sources of M_1 and M_2 are therefore at incremental ground and decoupled from each other!
- **Analysis can now be done on identical "half-circuits"**

What is the *differential* DC gain?

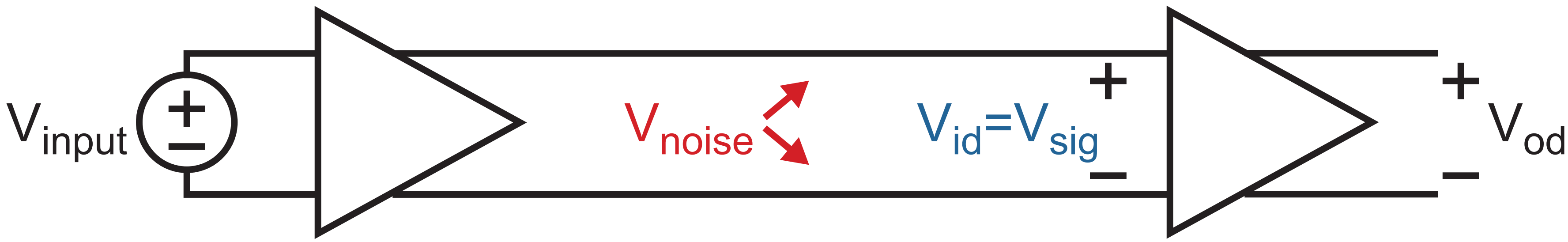
Common Mode Analysis



- **Key observations**
  - **Inputs are equal to each other**
  - **By linearity and symmetry, i_{s1} must equal i_{s2}**
    - This implies $i_R = 2i_{s1} = 2i_{s2}$
  - **We can view r_{o4} as two parallel resistors that have equal current running through them**
- **Analysis can also be done on two identical half-circuits**

What is the *common mode* DC gain?

Useful Metric for Differential Amplifiers: CMRR



- **Common Mode Rejection Ratio (CMRR)**
  - **Define: a_{vd}: differential gain, a_{vc}: common mode gain**

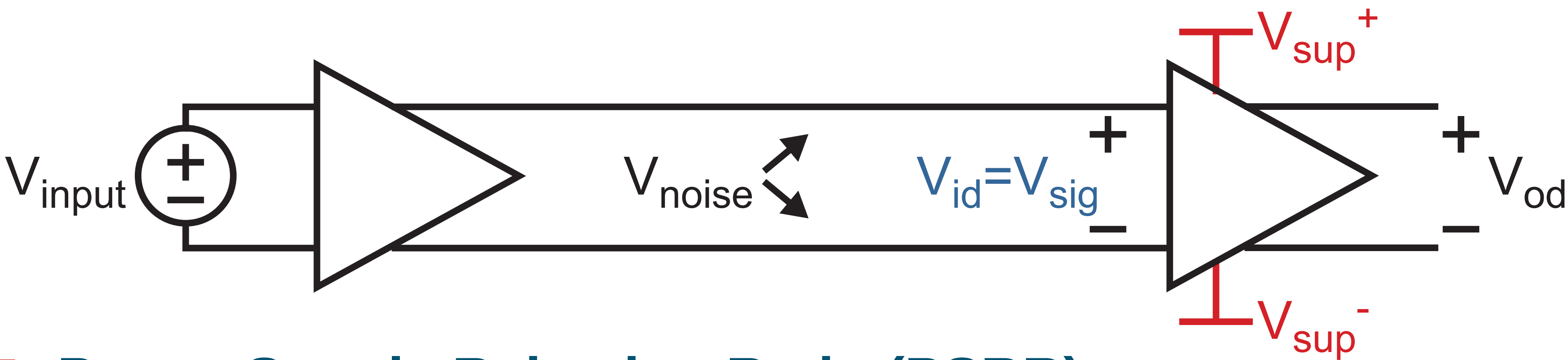
$$\mathrm{CMRR} = \left(\frac{a_{vd}}{a_{vc}}\right)$$

  - **CMRR corresponds to ratio of differential to common mode gain and is related to received signal-to-noise ratio**

$$V_{od} = a_{vd}V_{sig} + a_{vc}V_{noise}$$

$$\Rightarrow \frac{Signal}{Noise} = \left(\frac{a_{vd}}{a_{vc}}\right)\left(\frac{V_{sig}}{V_{noise}}\right) = \mathrm{CMRR}\left(\frac{V_{sig}}{V_{noise}}\right)$$

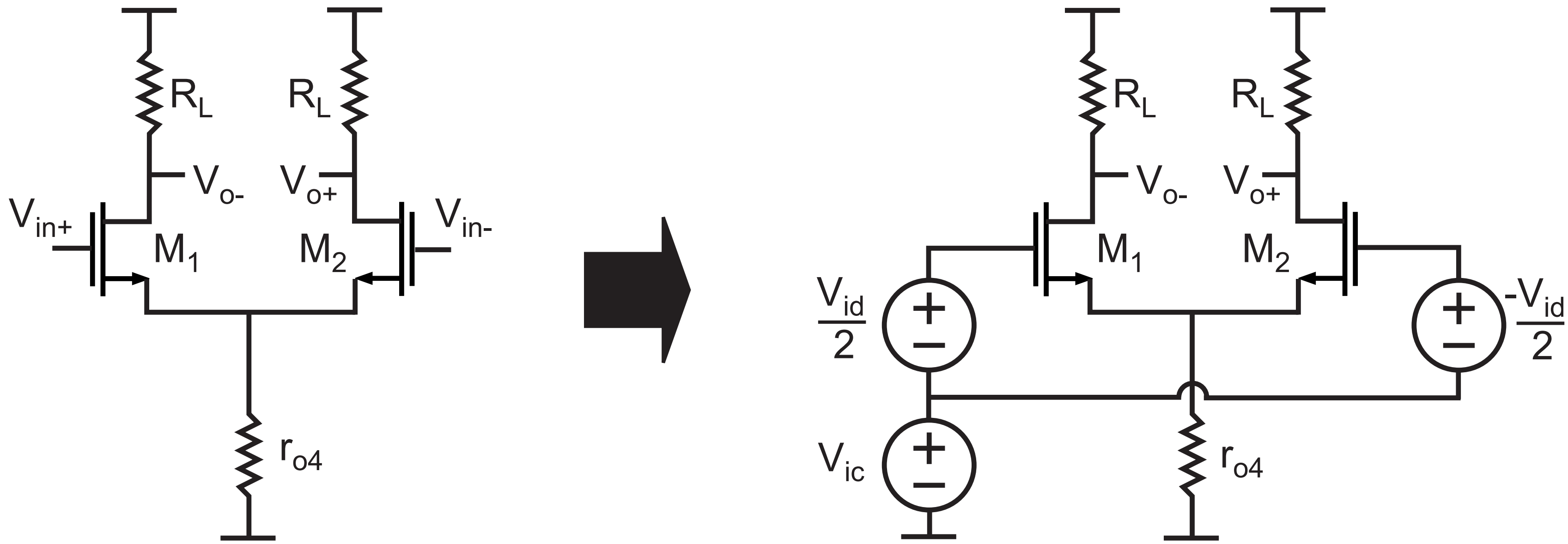
Another Useful Metric for Differential Amplifiers: PSRR



- **Power Supply Rejection Ratio (PSRR)**
  - **a_{vd}: differential gain**
  - **a_{vp+}: positive power supply gain**
  - **a_{vp-}: negative power supply gain**

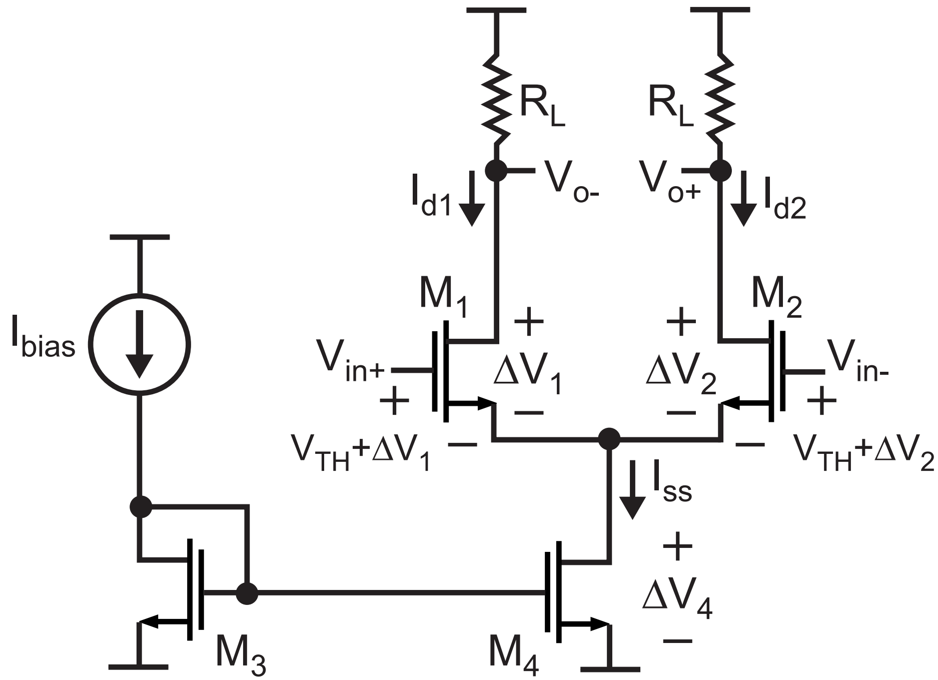
$$\mathrm{PSRR}^{+} = \left(\frac{a_{vd}}{a_{vp+}}\right) \qquad \mathrm{PSRR}^{-} = \left(\frac{a_{vd}}{a_{vp-}}\right)$$

Example: Calculate CMRR and PSRR



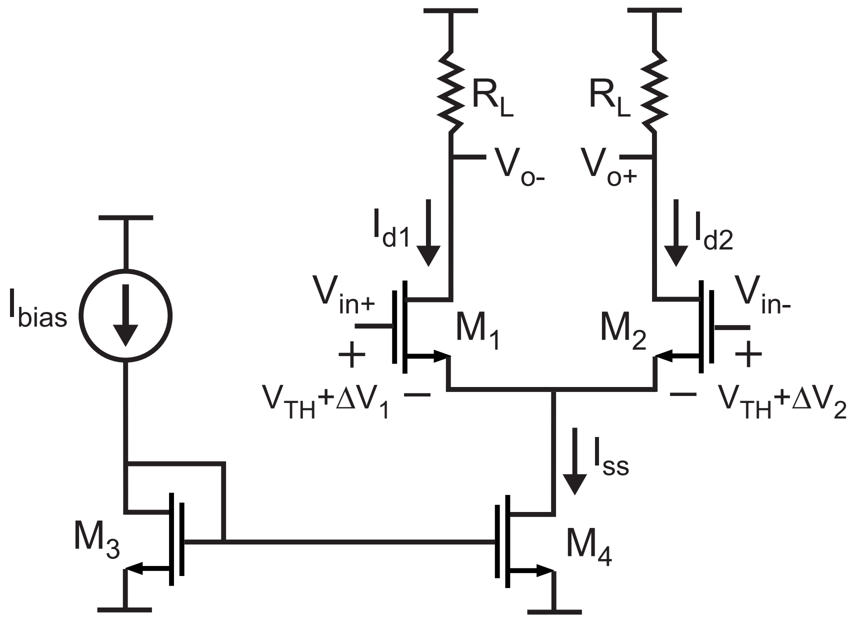
- **First determine a_{vd}, a_{vc}, a_{vp+}, and a_{vp-}**
- **Then calculate CMRR and PSRR**
  - **Note that CMRR and PSRR are often expressed in dB**
    - Example: CMRR = $20\log(a_{vd}/a_{vc})$

Common Mode Voltage Range of Differential Amplifier



- **While keeping all devices in saturation:**
  - **What is the maximum common mode output range?**
    - Assume $V_{id} = 0$
  - **What is the maximum common mode input range?**
    - Assume $V_{od} = 0$

Large Signal Behavior of Differential Mode Operation



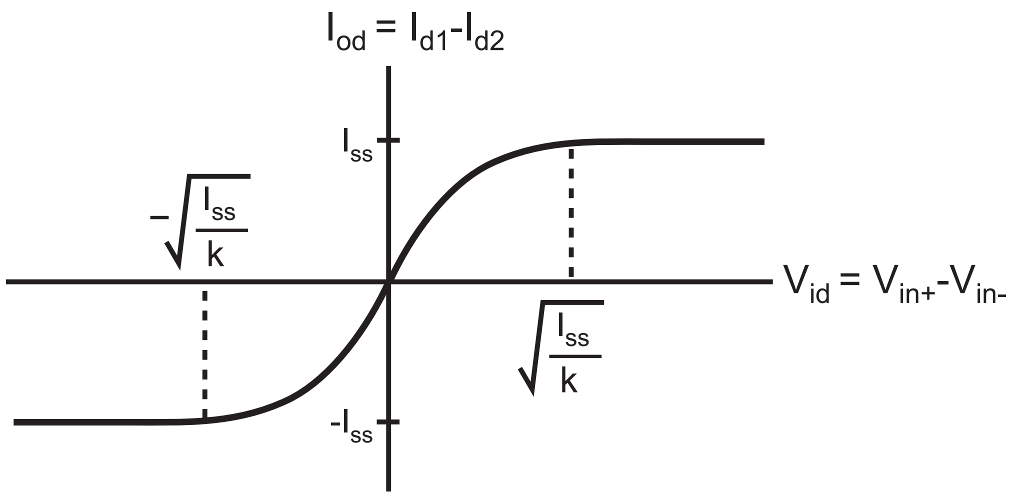
$$V_{id} = V_{in+} - V_{in-} = (V_{TH}+\Delta V_1) - (V_{TH}+\Delta V_2) = \Delta V_1 - \Delta V_2$$

$$V_{id} = \sqrt{\frac{I_{d1}}{k}} - \sqrt{\frac{I_{d2}}{k}} \qquad \text{where } k = \frac{\mu_n C_{ox} W}{2L}$$

$$V_{id} = \sqrt{\frac{I_{ss}+I_{od}/2}{k}} - \sqrt{\frac{I_{ss}-I_{od}/2}{k}} \qquad \text{where } I_{od} = I_{d1} - I_{d2}$$

square and solve for I_{od}

$$I_{od} = KV_{id}\sqrt{\frac{2I_{ss}}{k} - V_{id}^2} \qquad \text{for } V_{id} \le \sqrt{\frac{I_{ss}}{k}}$$



- **Note: above analysis assumes strong inversion**