Analysis and Design of Analog Integrated Circuits
Lecture 20

Advanced Opamp Topologies (Part II)

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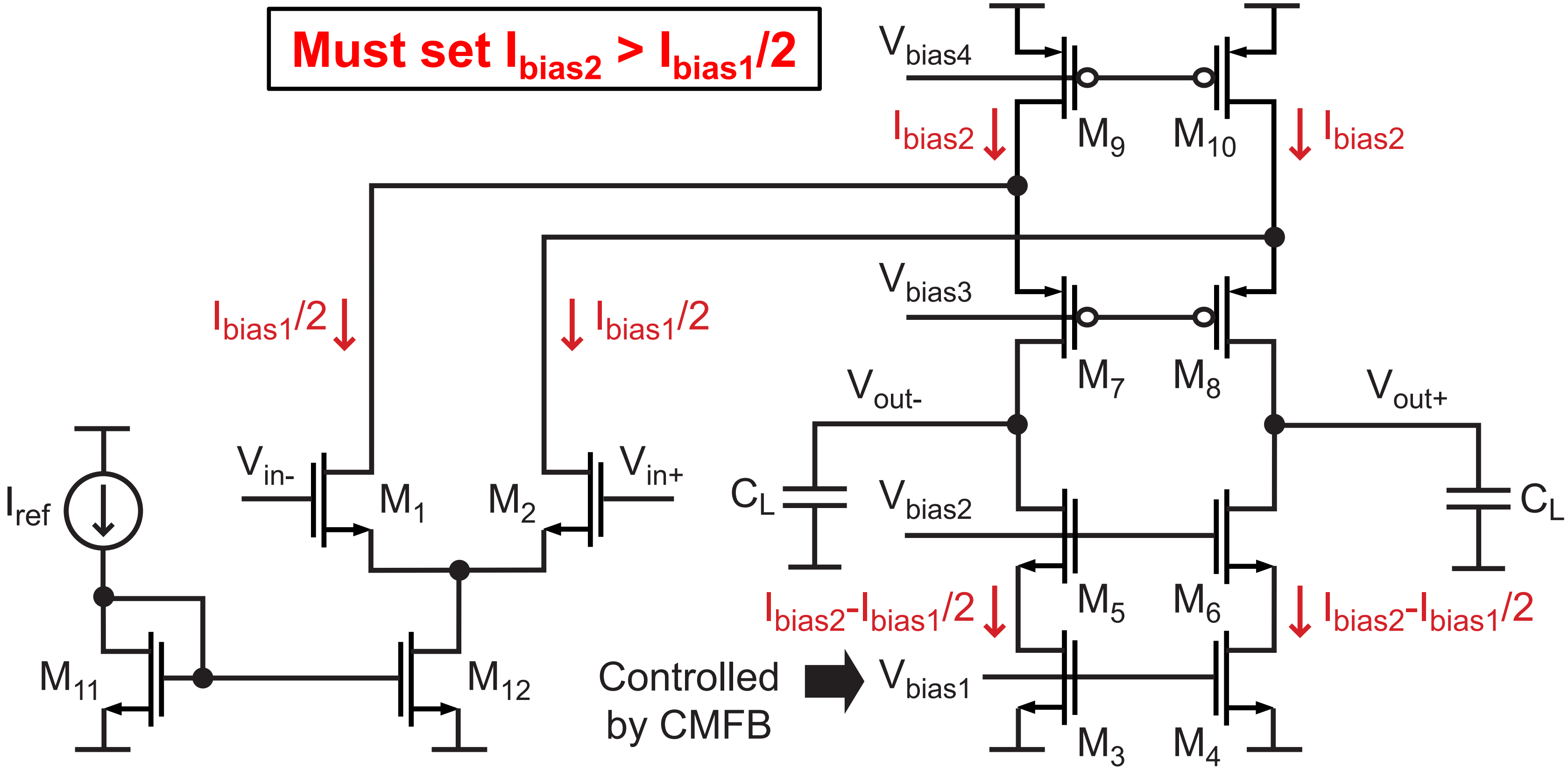
April 15, 2012

Outline of Lecture

- **Gain boosting technique**
- **Nested Miller technique**
- **Replica bias technique**
- **Improved slew rate opamp example**

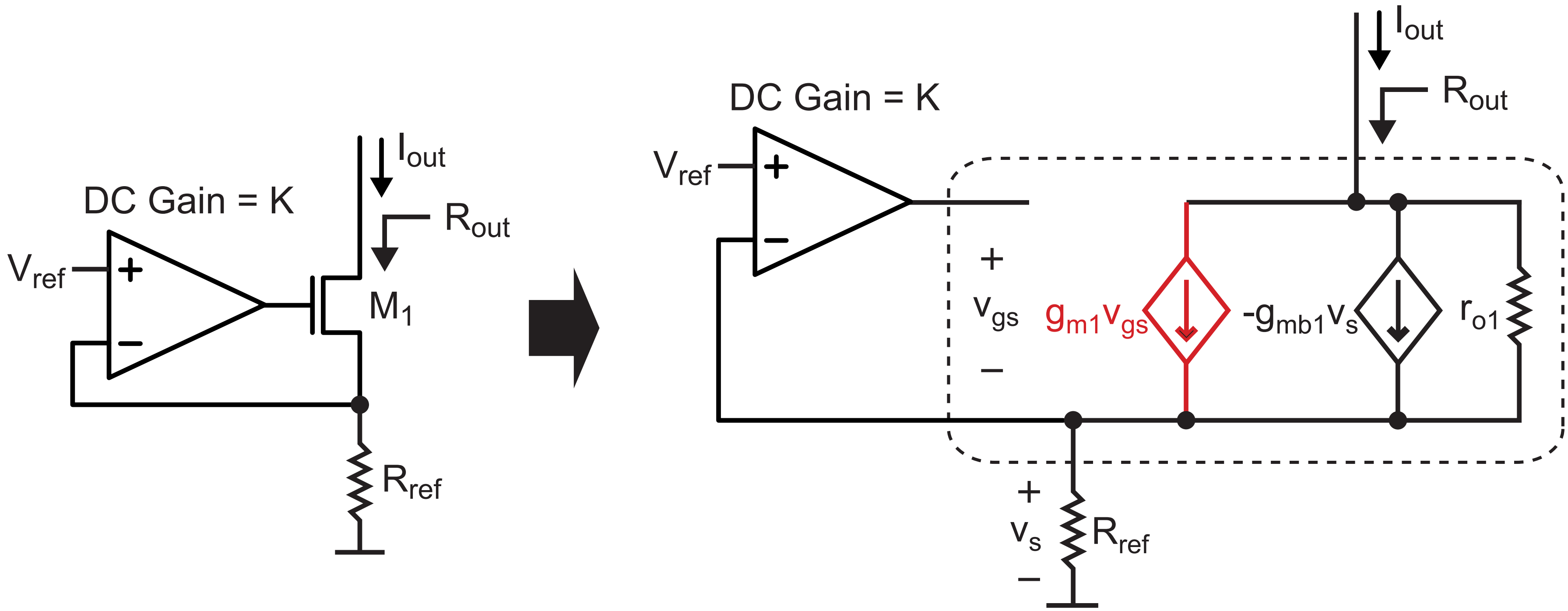
Recall the Folded Cascode Opamp



- **Modified version of telescopic opamp**
  - **Significantly improved input/output swing**
  - **High BW (better than two stage, worse than telescopic)**
  - **Single stage of gain (lower than telescopic)**

Can we further boost the DC gain?

Gain Boosting of Current Sources

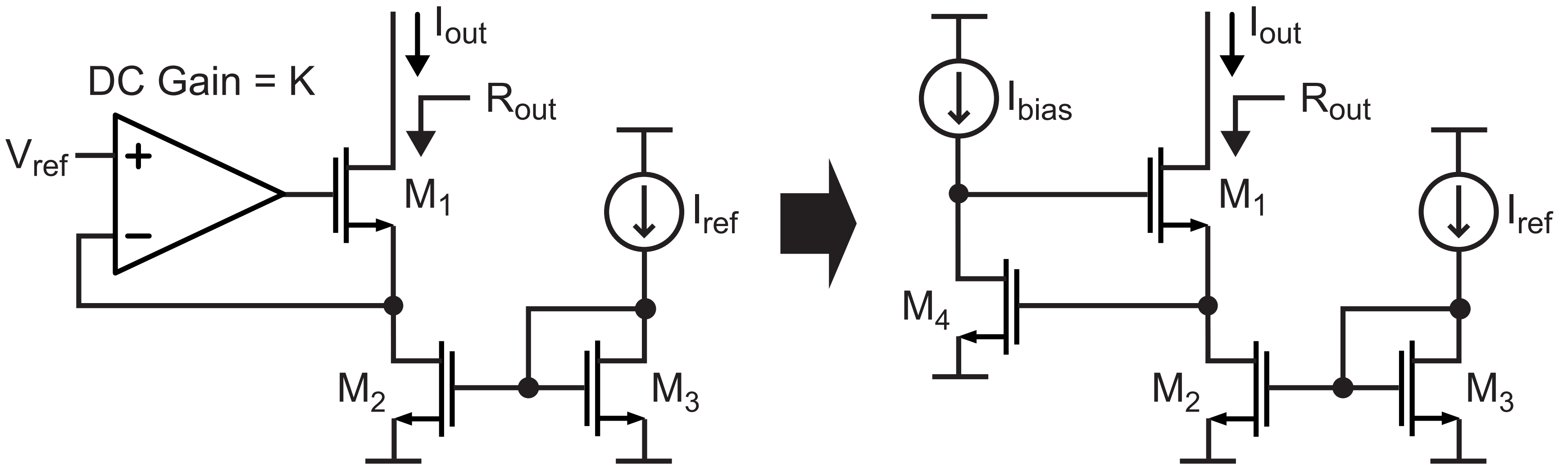


- **We can achieve increased output impedance of a current source with an amplifier**
  - **The amplifier essentially increases g_{m1} by factor K**

$$R_{out} = (K g_{m1} r_{o1}) R_{ref}$$

- **Key issue: what is a convenient implementation of the above circuit?**

A Simple Gain Boosting Amplifier



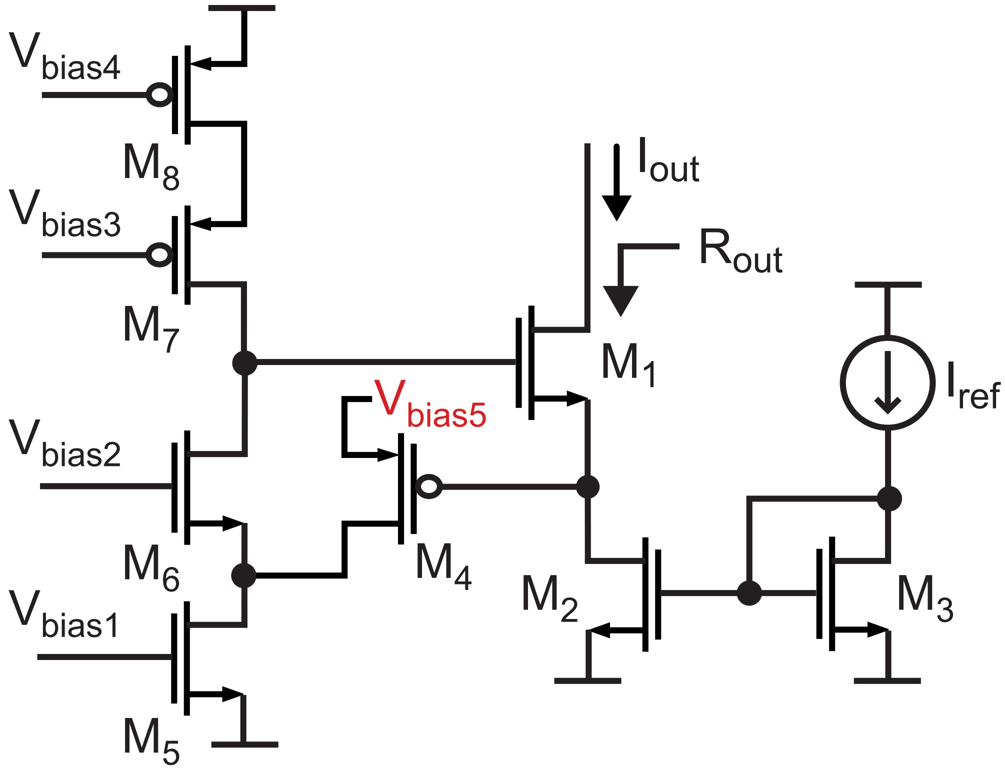
- **Common source amplifier utilized**

$$K = g_{m4} r_{o4},\ R_{ref} = r_{o2}$$

$$\Rightarrow\ R_{out} = (g_{m4} r_{o4})(g_{m1} r_{o1})\, r_{o2} \approx (g_m r_o)^2 r_{o2}$$

- **Issue: current source requires significant headroom due to the fact that $V_{ds2} = V_{gs4}$**

Folded Cascode Gain Boosting Amplifier



- **Folded cascode yields**

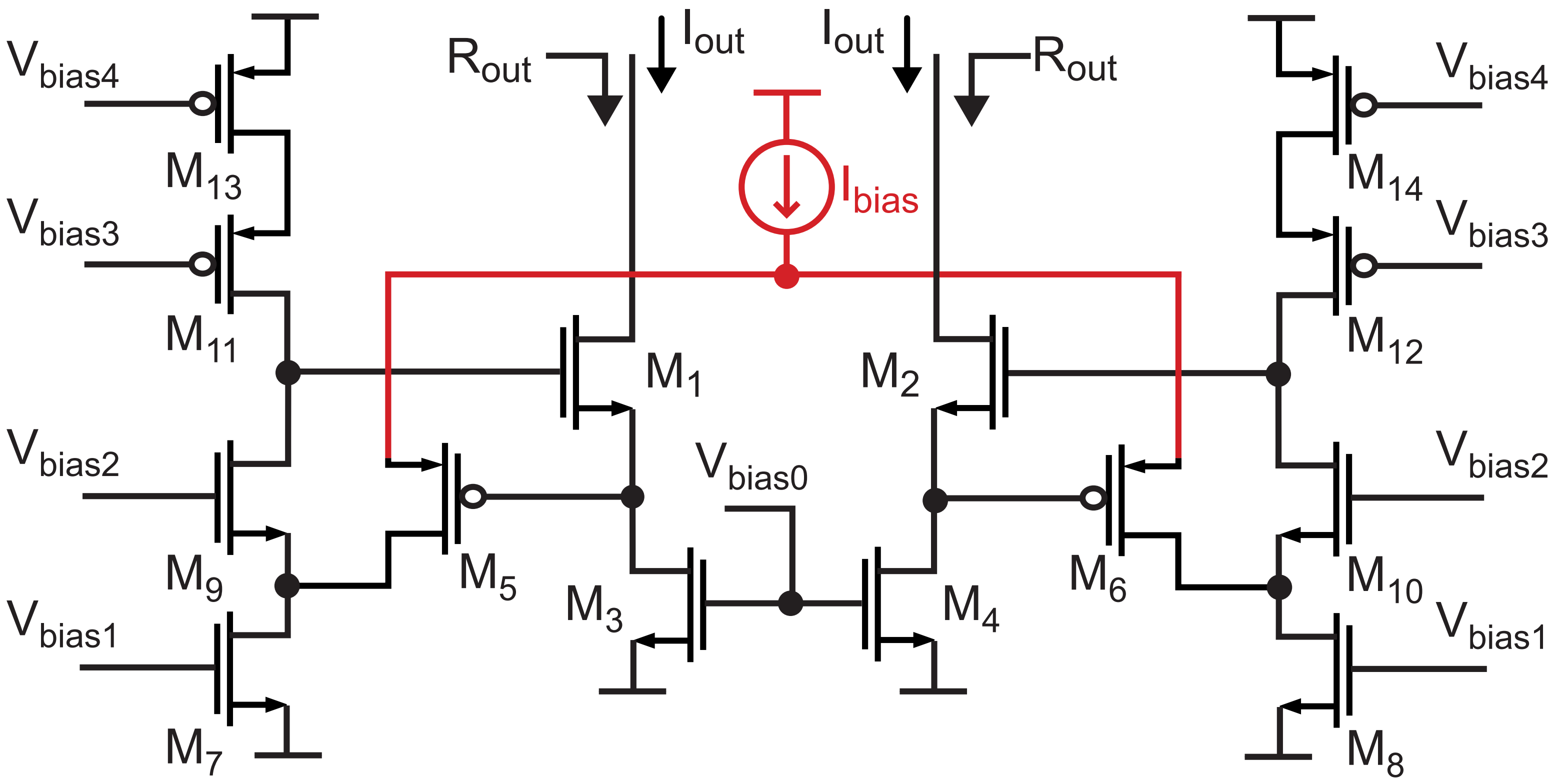
$$K = g_{m4}(((g_{m6}r_{o6})r_{o5})||((g_{m7}r_{o7})r_{o8}))$$

$$\Rightarrow \quad R_{out} \approx (g_m r_o)^3 r_{o2}$$

  - **Improved headroom and higher gain!**

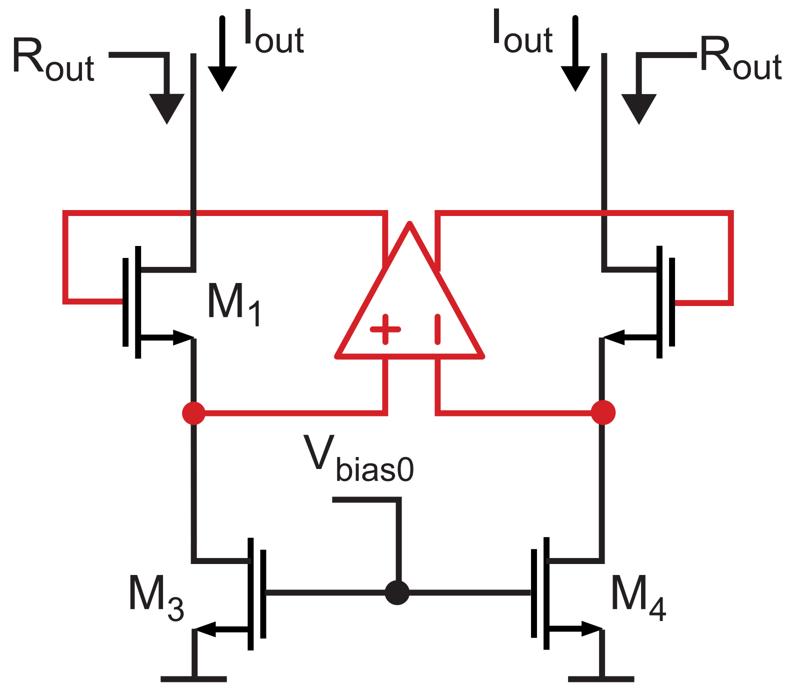
Is there a convenient way to set V_{bias5}?

Differential Version of Gain Boosting Amplifier



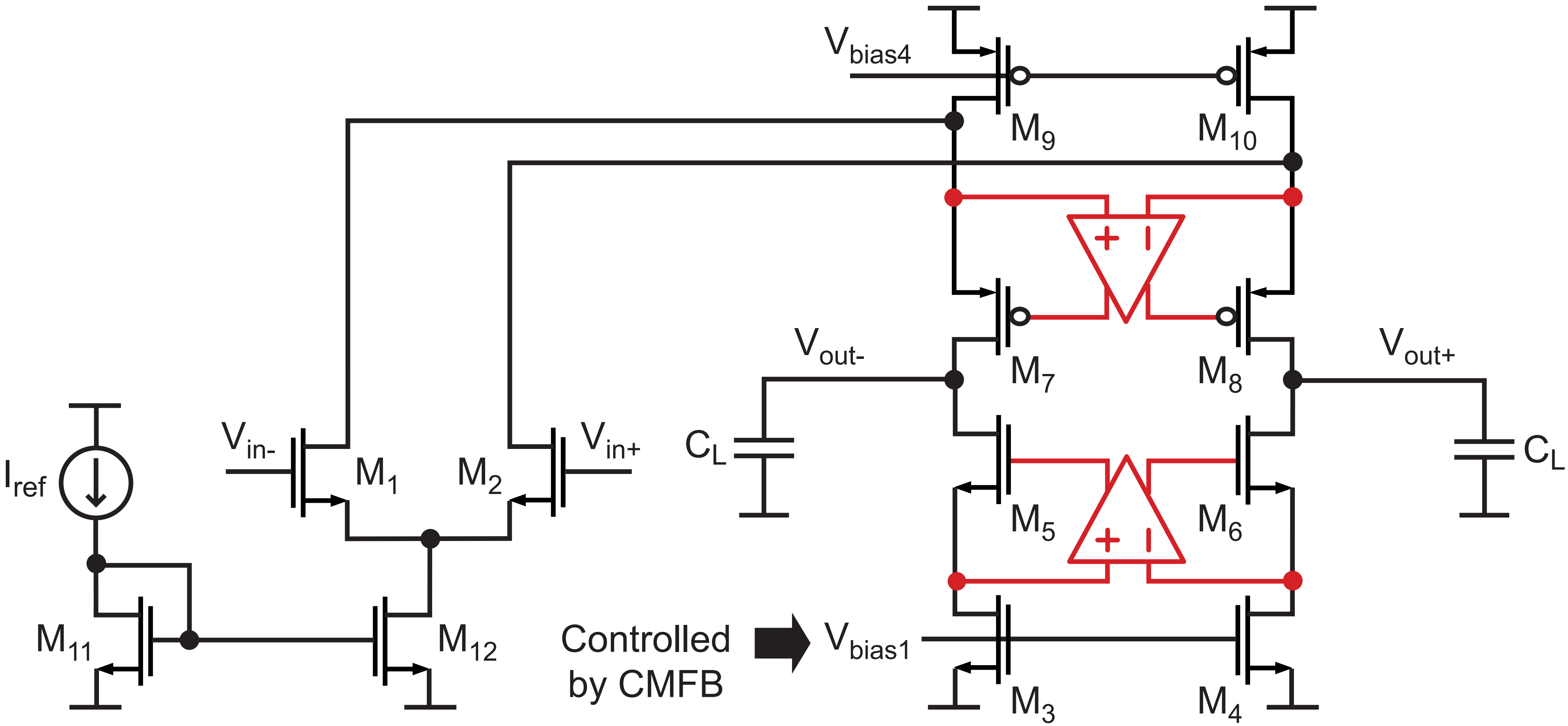
- **Leverage fully differential nature of current sources within the opamp**
  - **PMOS gain devices are now part of a differential pair**
  - **Need CMFB to set common-mode gate voltages of M_1 and M_2**

Symbolic View of Folded Cascode Gain Boosting Amp



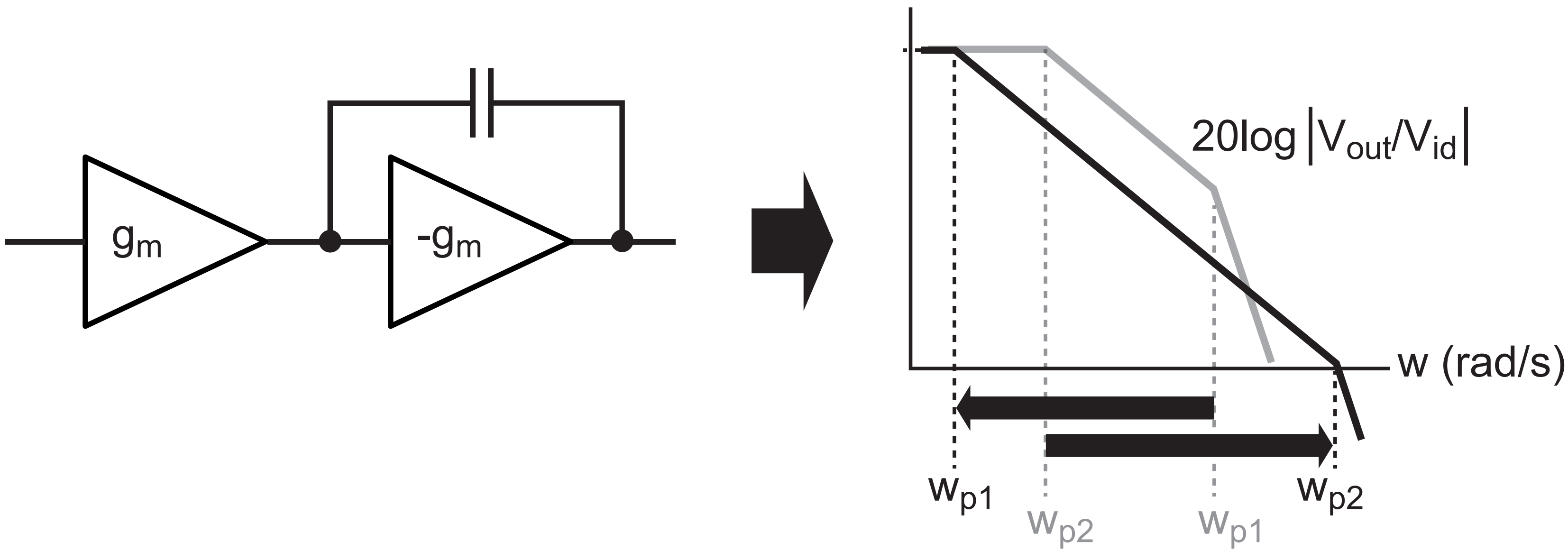
- **We can apply this to the overall folded cascode opamp**

Folded Cascode with Gain Boosting



- **Gain boosting provides substantial increase of DC gain while maintaining good input and output swing**
  - **Gain is on the order of $(g_m r_o)^4$**
- **Issue – very complex!**

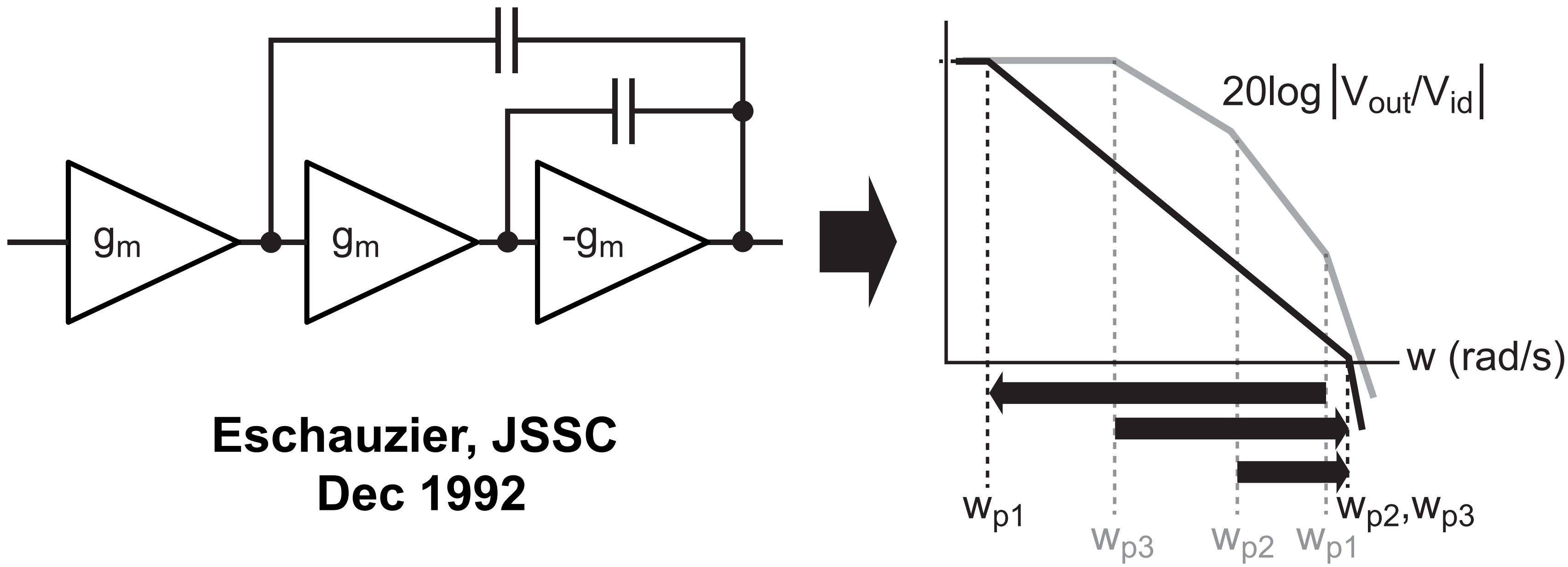
Recall Pole Splitting for Two Stage Compensation



- **Moves the dominant pole of the second stage to higher frequencies such that it becomes a parasitic pole**
- **Places the first stage pole as the dominant pole**
  - **Leverages the gain of the second stage to achieve capacitor multiplication using the Miller effect**

Can we extend the pole splitting technique to more than 2 gain stages?

Nested Miller Compensation

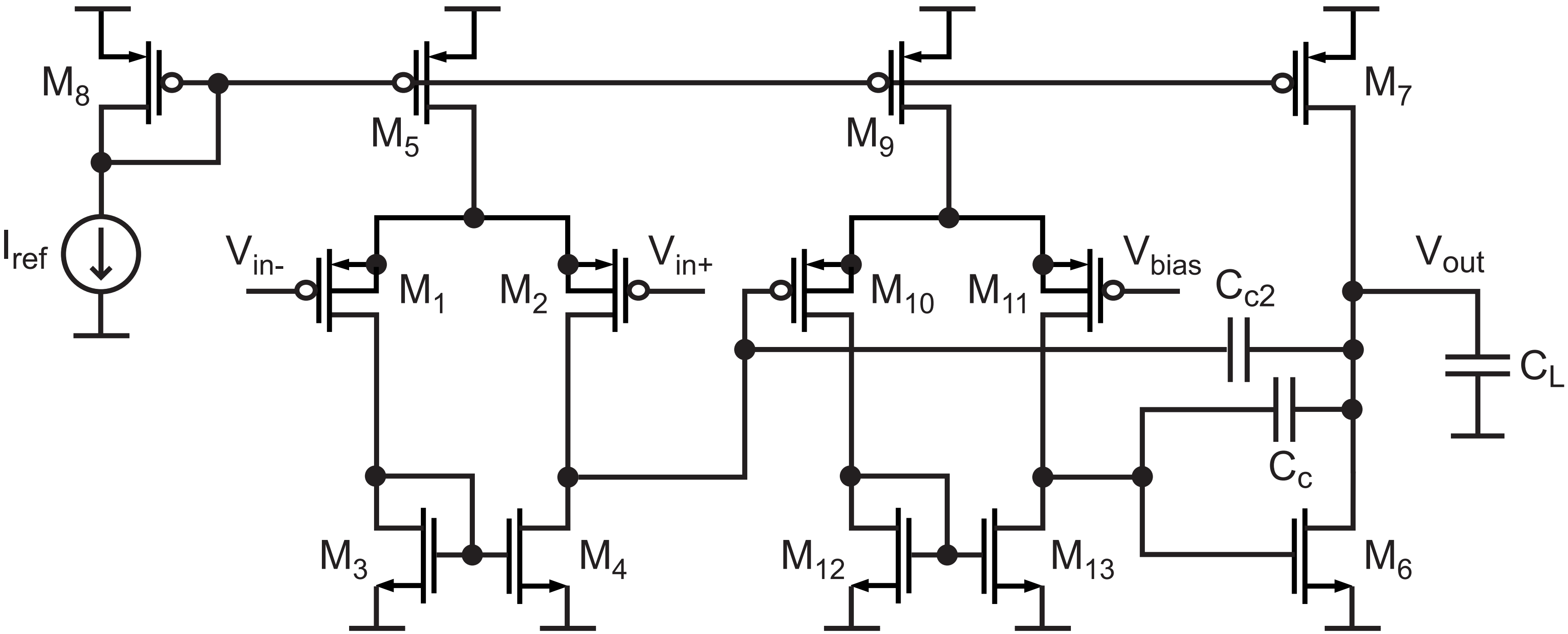


Eschauzier, JSSC
Dec 1992

- **Advantage: increased DC gain with high input and output swing**
- **Issue: more parasitic poles to deal with**
  - **Leads to lower unity gain bandwidth for reasonable phase margin**

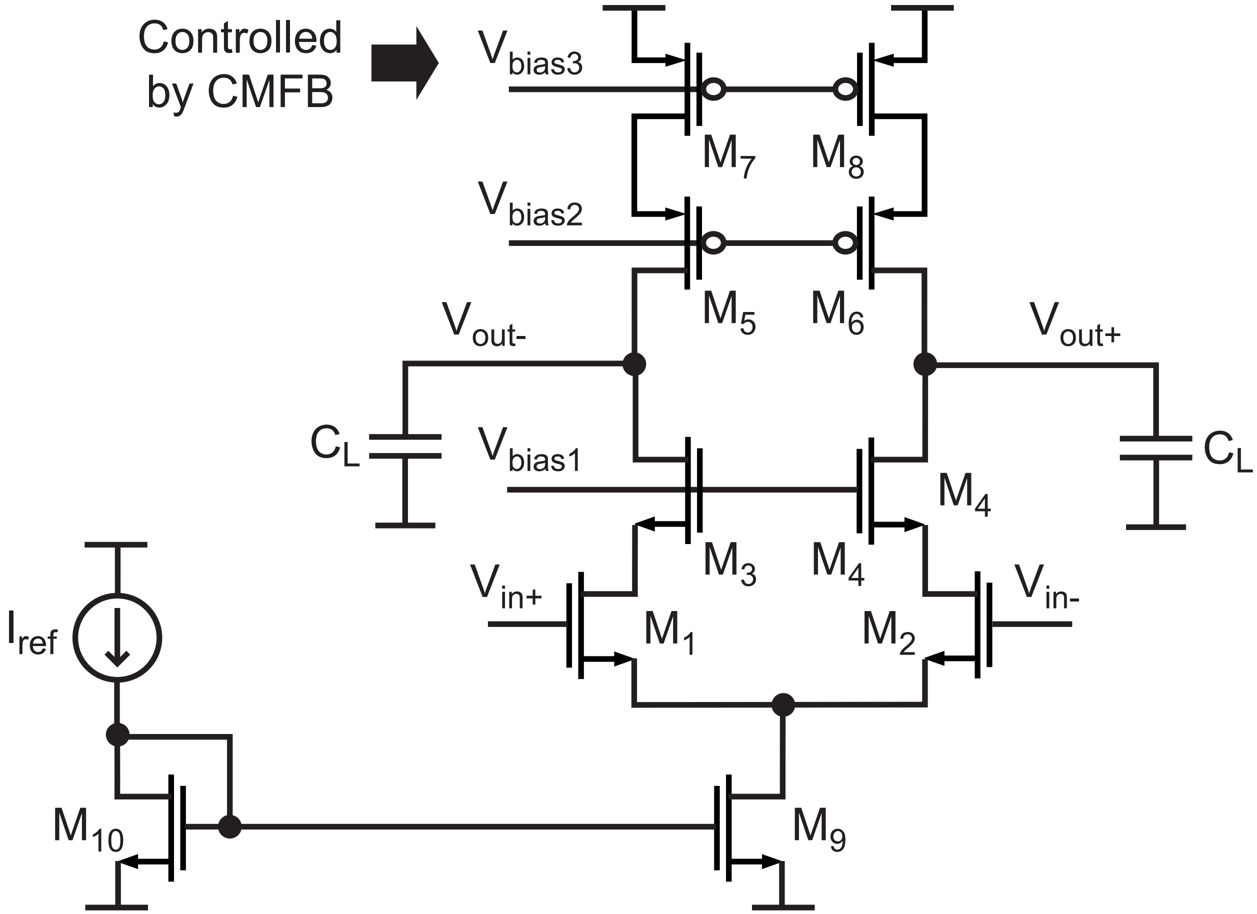
Proving to be a useful technique in advanced CMOS processes which offer fast speed (high g_m/C) but low intrinsic gain (low $g_m r_o$)

Nested Miller Example



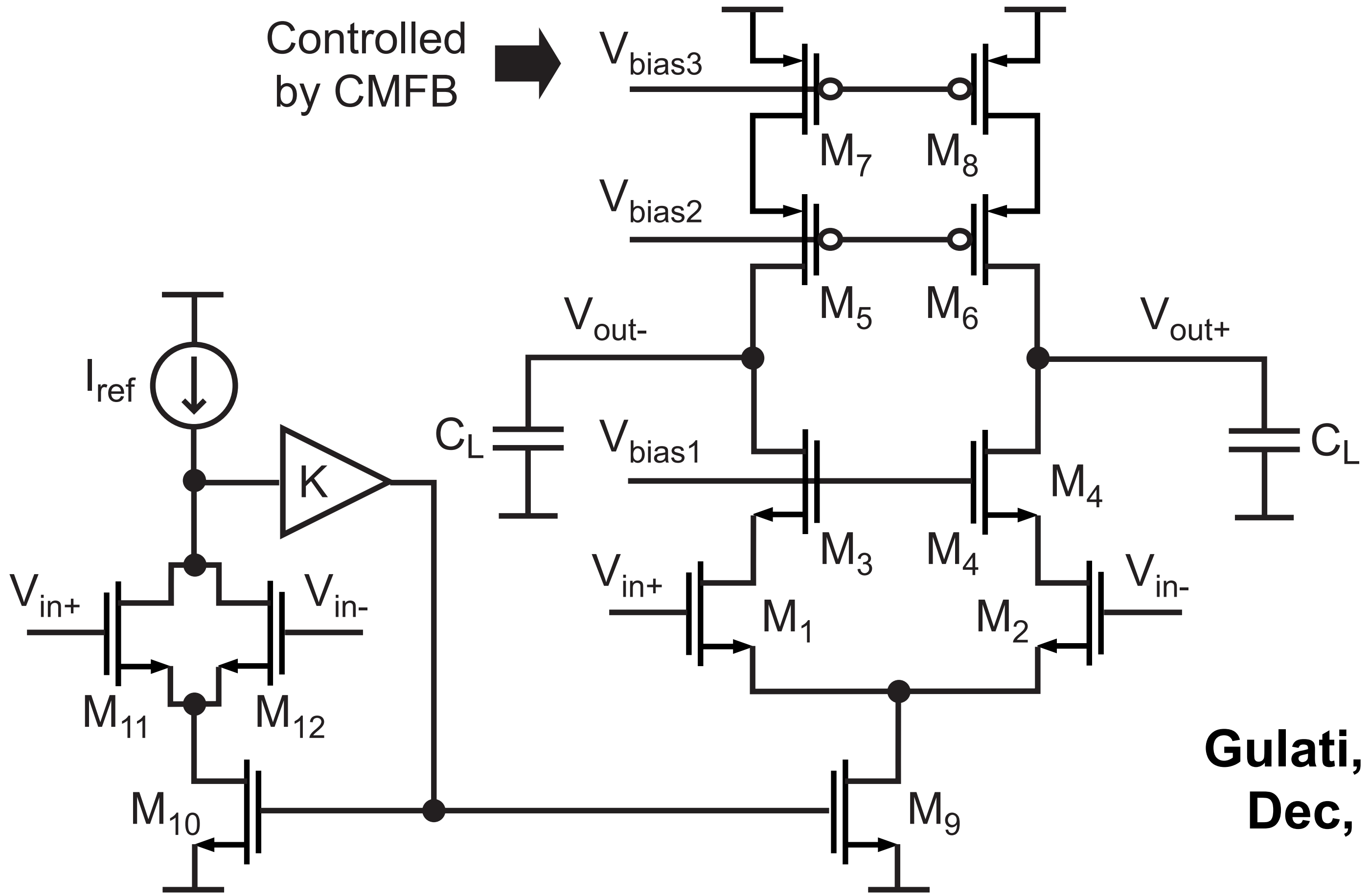
- Intermediate gain stages must be non-inverting in order to achieve stable feedback
- Compensation resistors should also be included to eliminate the impact of RHP zeros
  - Not shown for simplicity

Recall the Telescopic Opamp



- **Key issue is input swing**
  - **Can we improve this?**

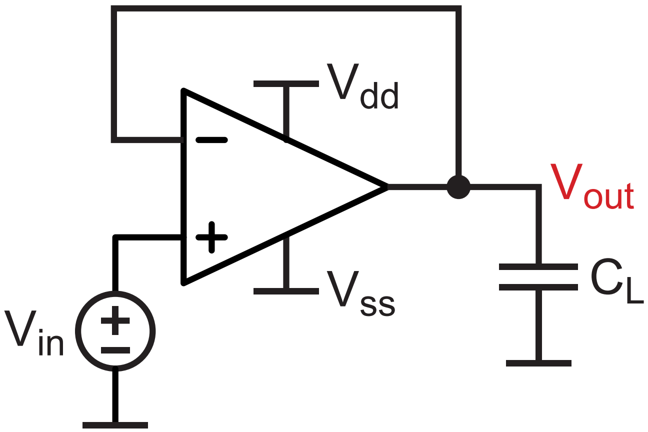
Replica Bias Technique

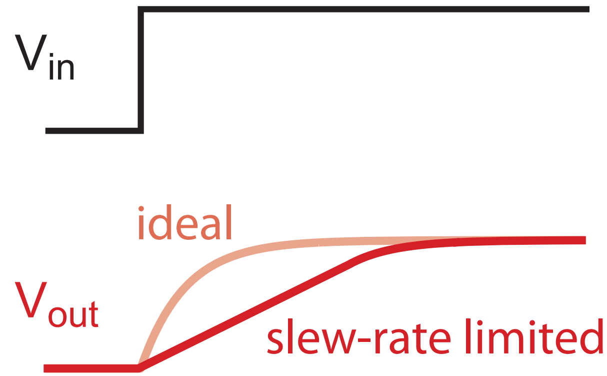


Gulati, JSSC Dec, 1998

- **Allows current source to maintain its output current even for low V_{ds} using dynamic bias of V_{gs}**
  - **Allows extended input common-mode range**

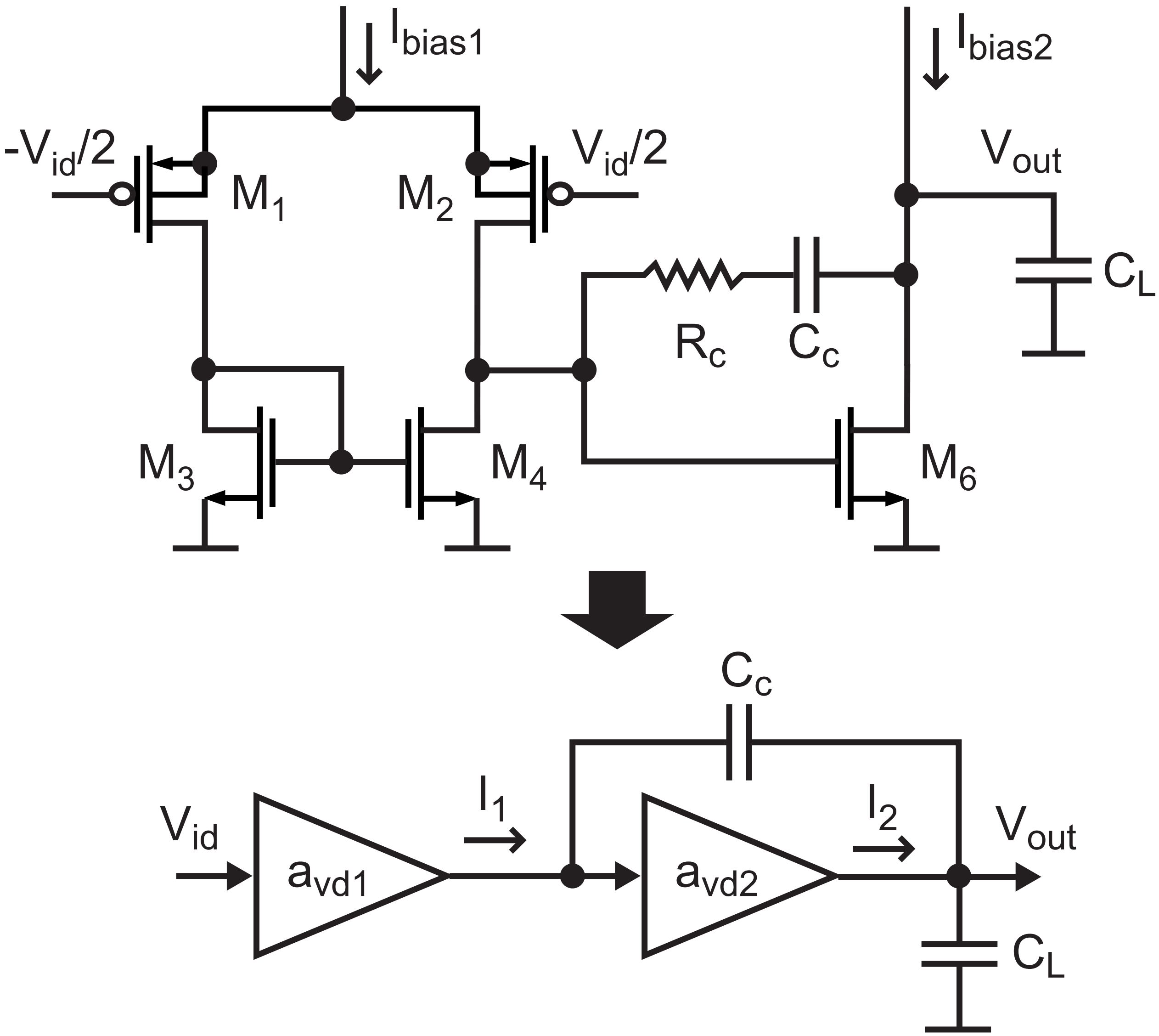
Recall: Slew Rate Issues for Opamps





- **Output currents of practical opamps have max limits**
  - **Impacts maximum rate of charging or discharging load capacitance, C_L**
  - **For large step response, this leads to the output lagging behind the ideal response based on linear modeling**
    - We refer to this condition as being slew-rate limited
- **Where slew-rate is of concern, the output stage of the opamp can be designed to help mitigate this issue**
  - **Will lead to extra complexity and perhaps other issues**

Key Observations for Slew Rate Calculations



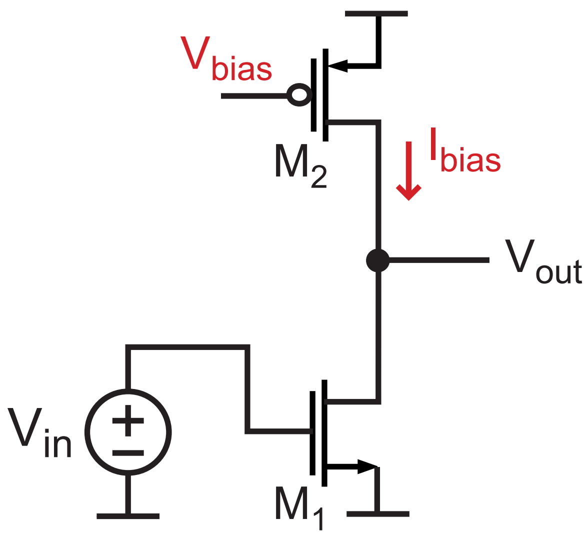
Current Limits

- **First stage**
  - **Max $I_1 = I_{bias1}$**
  - **Min $I_1 = -I_{bias1}$**
- **Second stage**
  - **Max $I_2 = I_{bias2}$**
  - **Min I_2 = Large**

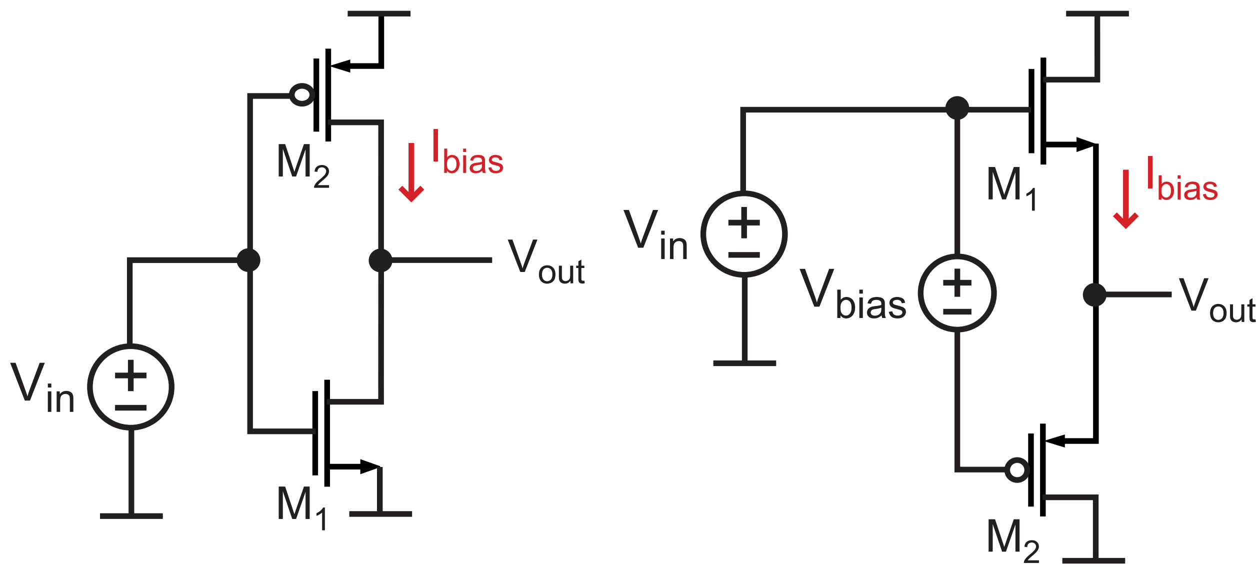
How can we improve opamp slew rate?

Class A and AB Amplifiers/Buffers

Class A Amplifier

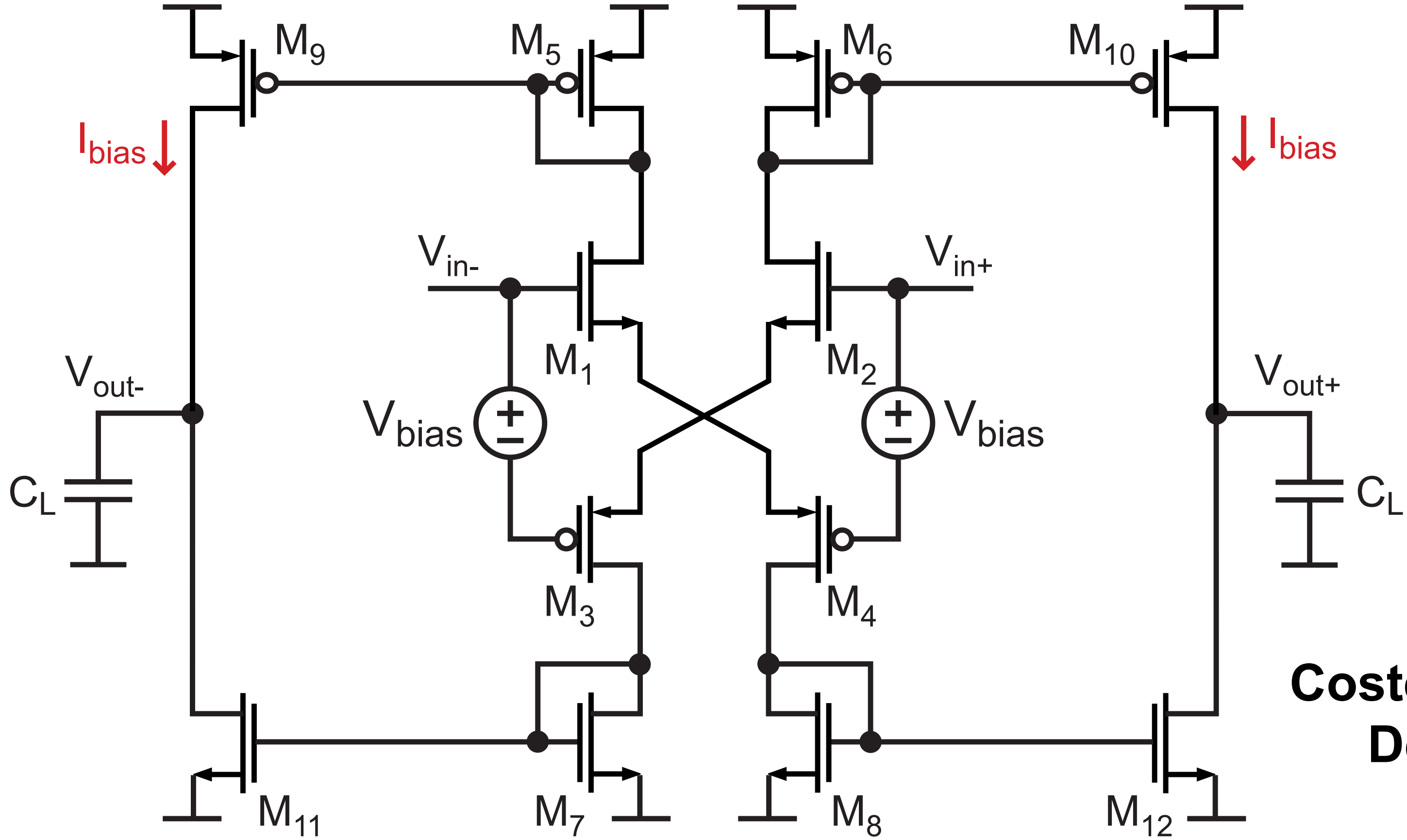


Class AB Amplifier/Buffer



- **Class A**
  - **Maximum slew rate in one direction is set by the nominal bias current**
- **Class AB**
  - **Maximum slew rate is not set by the nominal bias current**
    - Goal: low nominal bias current

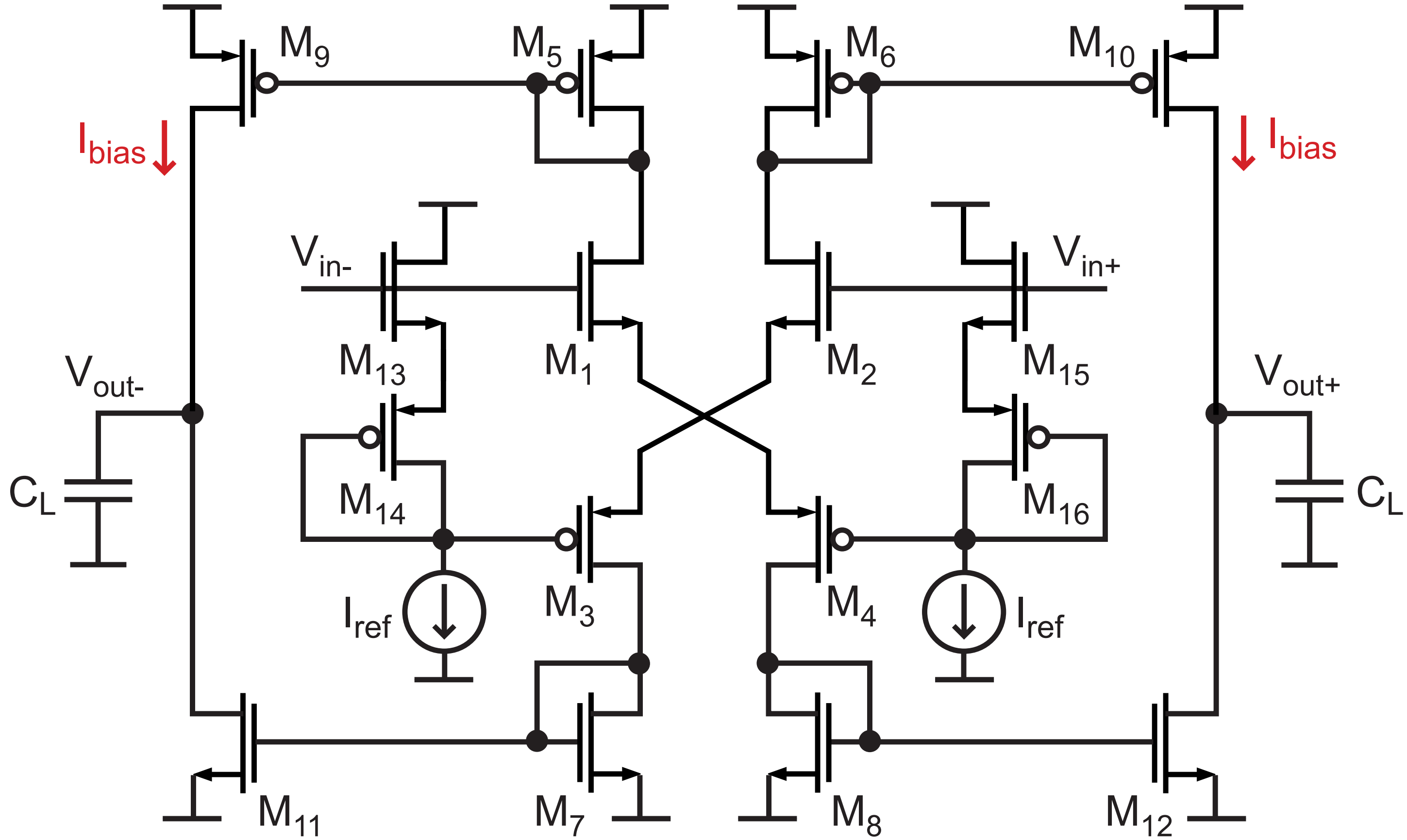
Class AB Opamp



Costello, JSSC Dec 1985

- **Low bias current can be achieved for $V_{in+} = V_{in-}$**
  - **Must properly set V_{bias}**
- **Much higher current when $V_{in+} \neq V_{in-}$**
- **DC gain can be increased through cascoding of output stage**

Biasing Network for Class AB Opamp



- **Bias current set by**
  - **Ratio of device sizes of M_1-M_4 versus M_{13}-M_{16}**
  - **I_{ref} current**

Summary

- Opamps invite a wide variety of techniques to address different application requirements
  - Cleverness can substantially improve performance and robustness
  - Changing of CMOS processes over time leads to new techniques which were previously unnecessary or unpractical
- Four techniques discussed today
  - Gain boosting
  - Nested Miller
  - Replica bias
  - Class AB stages