Analysis and Design of Analog Integrated Circuits
Lecture 18

Key Opamp Specifications

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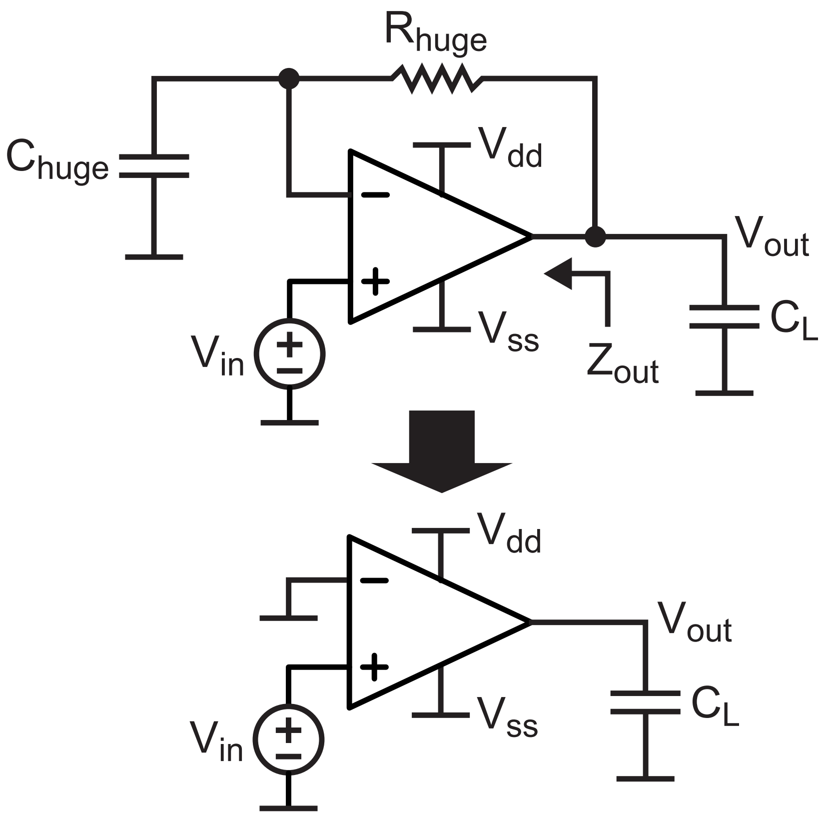
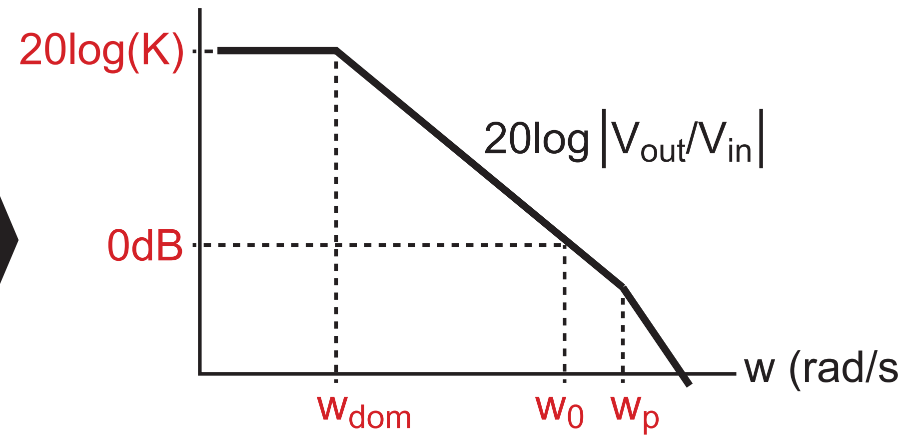
Recall: Key Specifications of Opamps (Open Loop)



<u>For Open Loop Characterization</u>

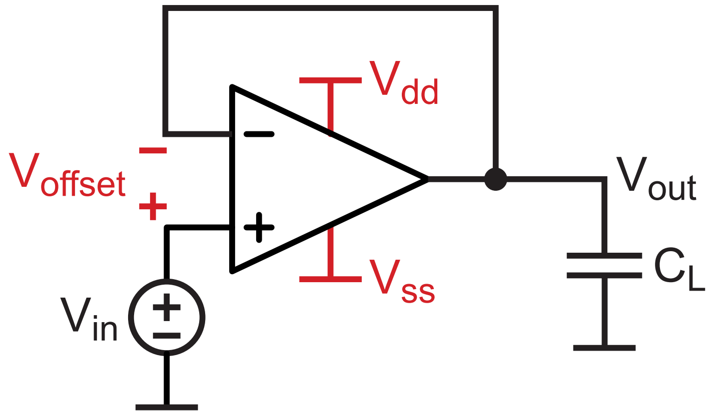
Set R_{huge} >> $|Z_{out}|$

and $1/(R_{huge}C_{huge}) \ll w_{dom}$



- **DC small signal gain: *K***
- **Unity gain frequency: w_0**
- **Dominant pole frequency: w_{dom}**
- **Parasitic pole frequencies: w_p (and higher order poles)**
- **Output swing (max output range for DC gain > K_{min})**

Recall: Key Specifications of Opamps (Closed Loop)



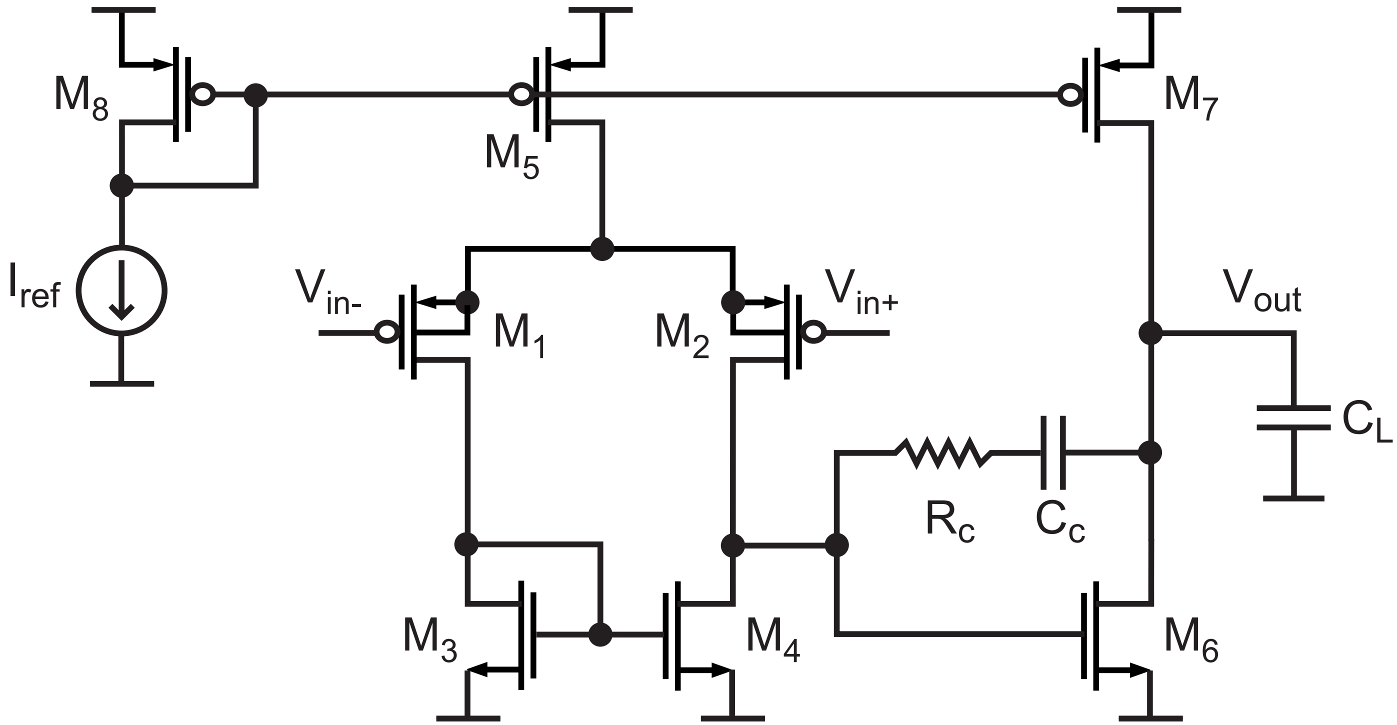
- **Offset voltage**
- **Settling time (closed loop bandwidth)**
- **Input common mode range**
- **Equivalent Input-Referred Noise**
- **Common-Mode Rejection Ratio (*CMRR*)**

$$CMRR = \left(\frac{\delta V_{offset}}{\delta V_{in}}\right)^{-1}$$

- **Power Supply Rejection Ratio (*PSRR*)**

$$PSRR^{+} = \left(\frac{\delta V_{offset}}{\delta V_{dd}}\right)^{-1} \qquad PSRR^{-} = \left(\frac{\delta V_{offset}}{\delta V_{ss}}\right)^{-1}$$

Basic Two Stage CMOS Op Amp

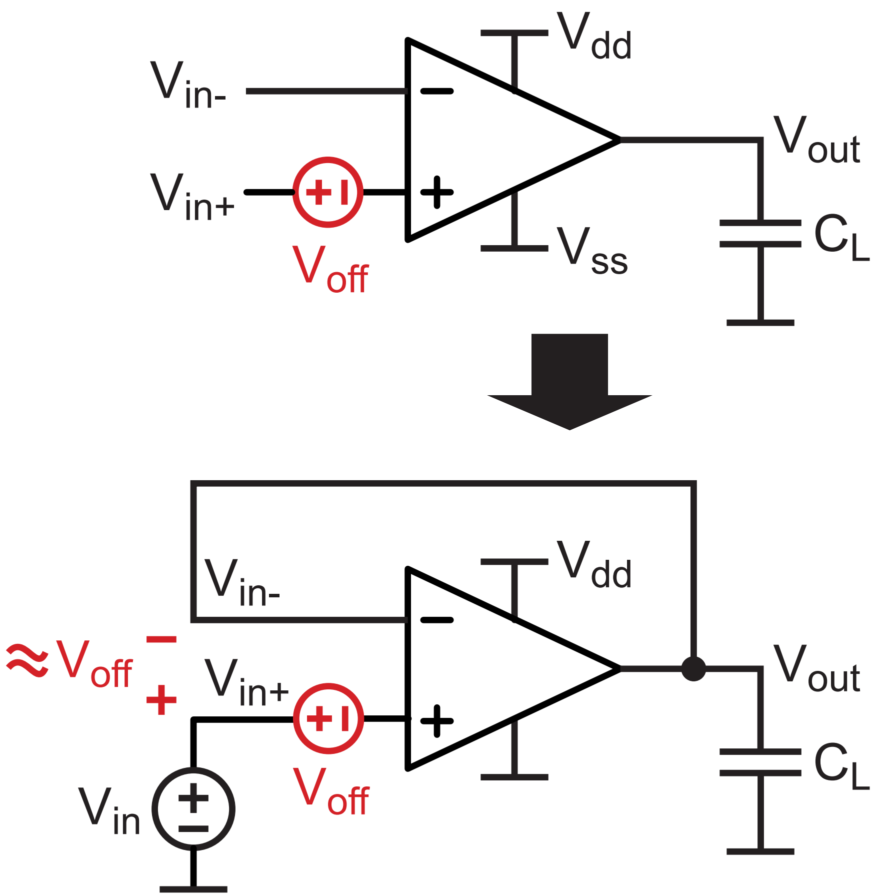


- **This is a common "workhorse" opamp for medium performance applications**
- **Provides a nice starting point to discuss various CMOS opamp design issues**
- **Starting assumptions: $W_1/L_1 = W_2/L_2$, $W_3/L_3 = W_4/L_4$**

Key Specifications Discussed In This Lecture

- Systematic offset voltage
- CMRR
- $PSRR^+$ and $PSRR^-$
- Input-referred voltage noise
- Slew rate

A Closer Look at Offset Voltage



$$V_{out} = H(s)\left(V_{in+} - V_{in-} - V_{off}\right)$$

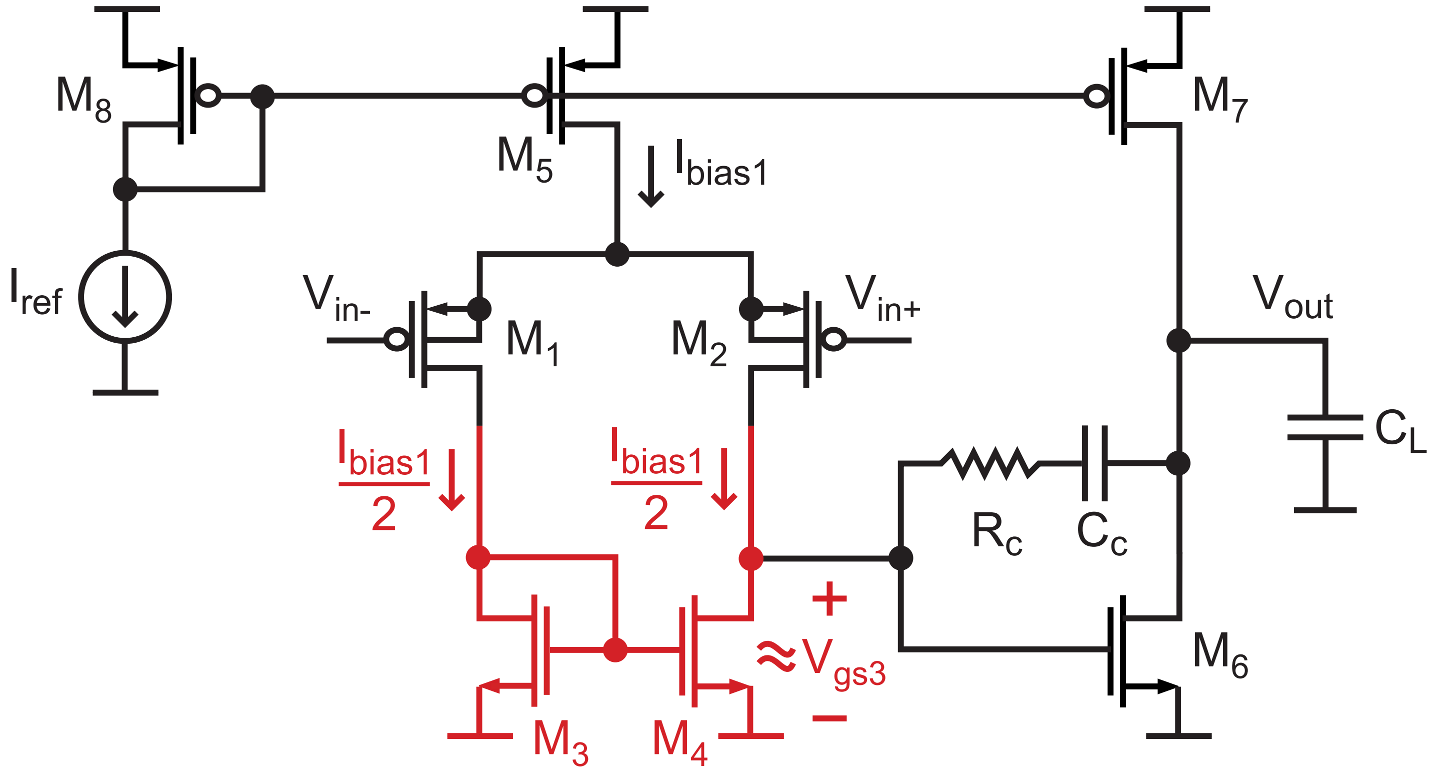
- **Assume:**
  - **Input to opamp is a DC signal**
  - **Amplifier is not saturated**
  - **DC gain of amplifier is large**

$$V_{out} = K\left(V_{in+} - V_{in-} - V_{off}\right)$$

$$\Rightarrow V_{in+} - V_{in-} = V_{off} + V_{out}/K \approx V_{off}$$

Two sources of offset: systematic and random

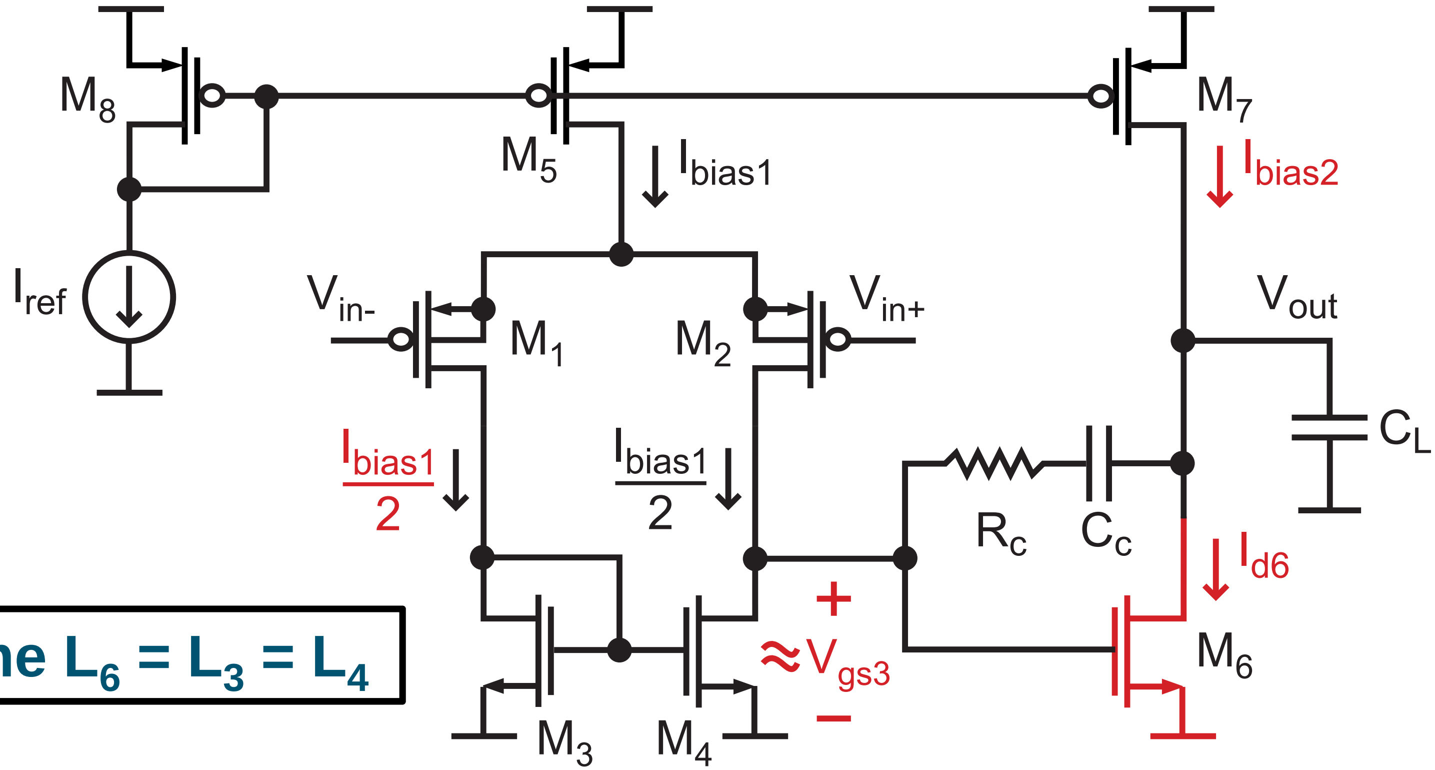
Systematic Offset: First Stage Analysis



- **For zero systematic offset we want V_{out} to be at roughly mid-rail assuming $V_{in+} = V_{in-}$**
  - **$V_{in+} = V_{in-}$ leads to equal currents in M_3/M_4**
  - **Equal currents and equal V_{gs} for M_3/M_4 leads to:**

$$V_{ds4} = V_{ds3} = V_{gs3}$$

Key Constraints To Achieve Zero Systematic Offset



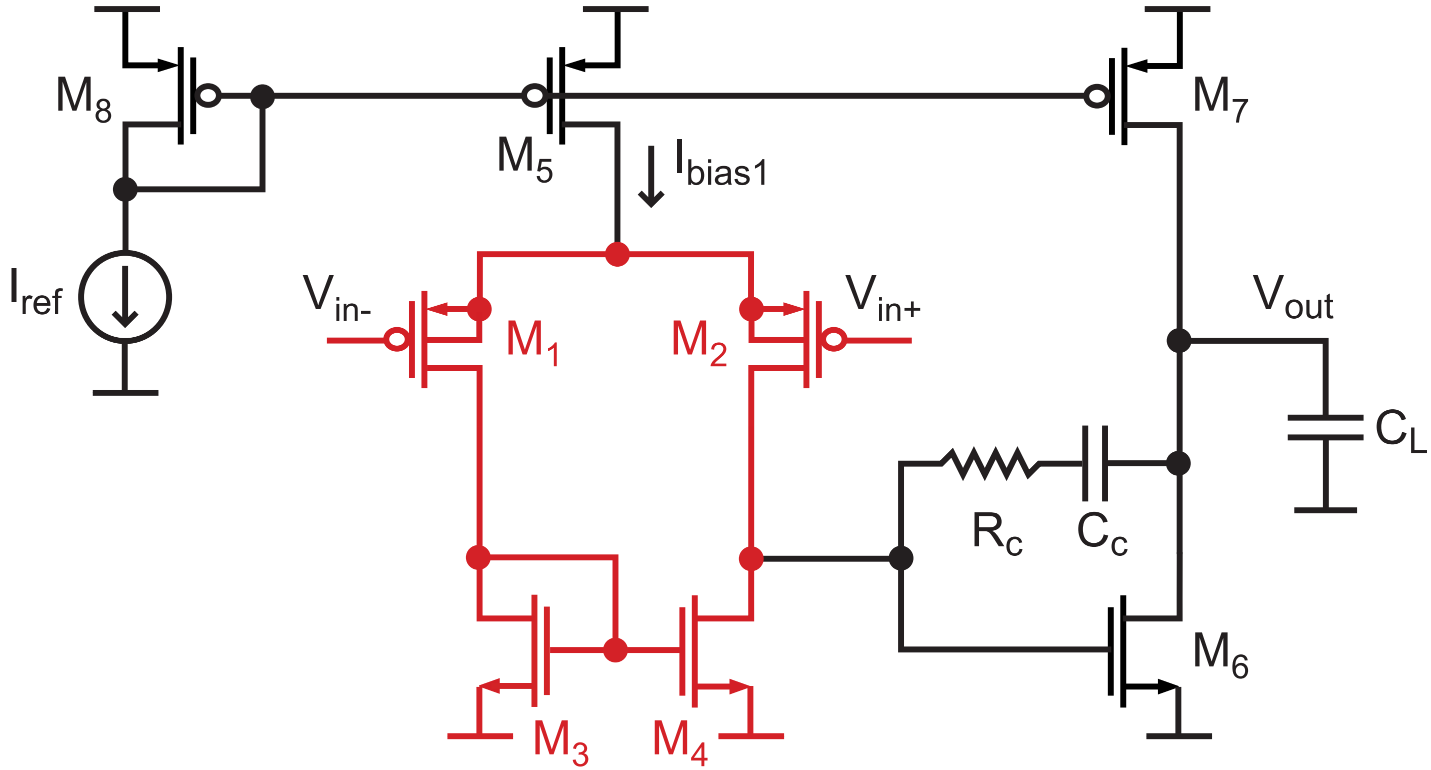
assume $L_6 = L_3 = L_4$

- **For mid-rail V_{out}, we need $I_{d6} = I_{bias2}$**

$$\Rightarrow \quad I_{d6} = \frac{1}{2}\mu_n C_{ox}\frac{W_6}{L_6}\left(V_{gs3} - V_{TH}\right)^2 = I_{bias2}$$

Also: $$\frac{1}{2}\mu_n C_{ox}\frac{W_3}{L_3}\left(V_{gs3} - V_{TH}\right)^2 = \frac{I_{bias1}}{2} \Rightarrow \boxed{\frac{W_6}{2W_3} = \frac{I_{bias2}}{I_{bias1}} = \frac{W_7}{W_5}}$$

Key Common-Mode Rejection (CMRR) Observations



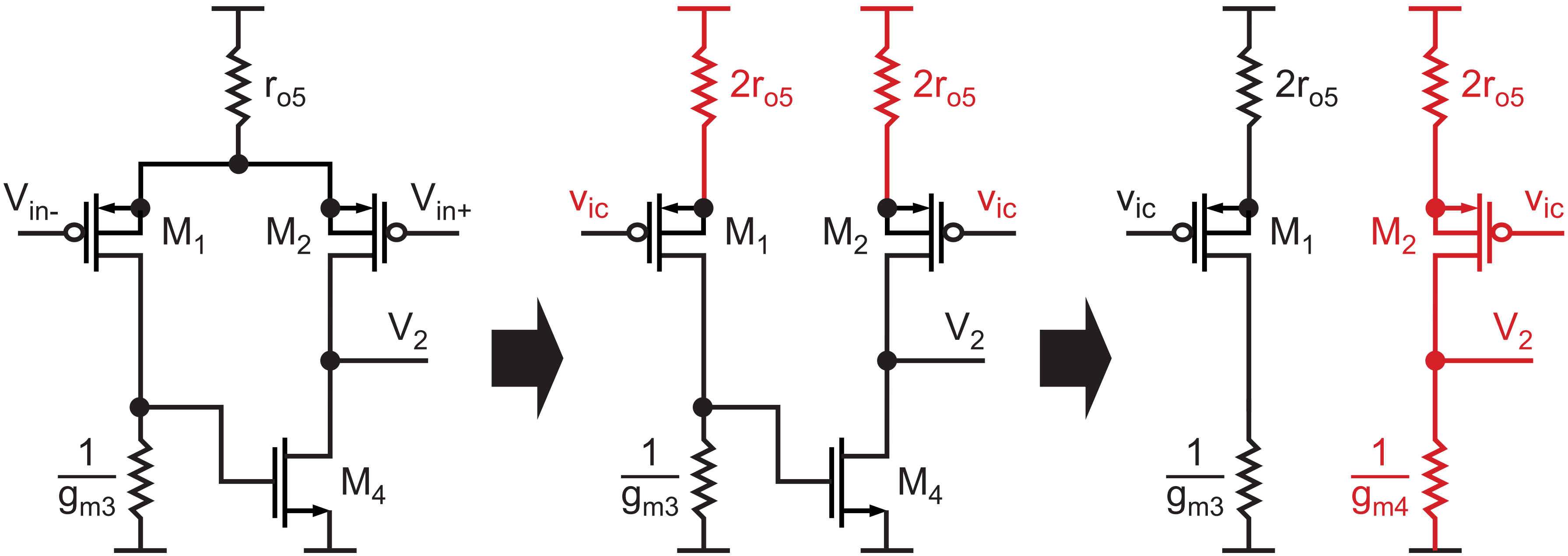
- **CMRR defined as a_{vd}/a_{vc}, where**

$$a_{vd} = a_{vd1}a_{vd2} \qquad a_{vc} = a_{vc1}a_{vd2}$$

- **Inspection of the above reveals that CMRR is determined by the first stage**

$$CMRR = \frac{a_{vd1}a_{vd2}}{a_{vc1}a_{vd2}} = \frac{a_{vd1}}{a_{vc1}} = CMRR_1$$

Common Mode Gain and Resulting CMRR



- **Differential gain was derived in Lecture 17**

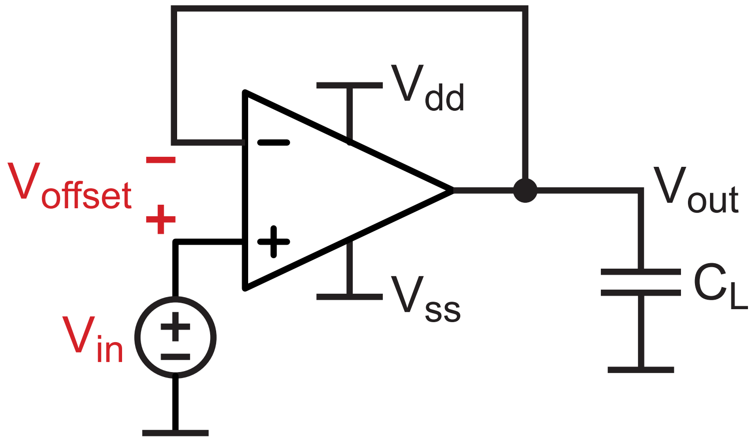
$$a_{vd1} = g_{m1}\left(r_{o2}||r_{o4}\right)$$

- **Common-mode gain is calculated from the above as**

$$a_{vc1} = \frac{1/g_{m4}}{1/g_{m2} + 2r_{o5}} \approx \frac{1}{2g_{m4}r_{o5}}$$

$$\Rightarrow \quad CMRR = \frac{a_{vd1}}{a_{vc1}} = \boxed{2g_{m1}(r_{o2}||r_{o4})g_{m4}r_{o5}}$$

Characterizing CMRR with Changes in Offset Voltage



- **Consider V_{in} as a common-mode signal which has an *open loop* impact on V_{out} as**

$$\Delta V_{out} = a_{vc} \Delta V_{in}$$

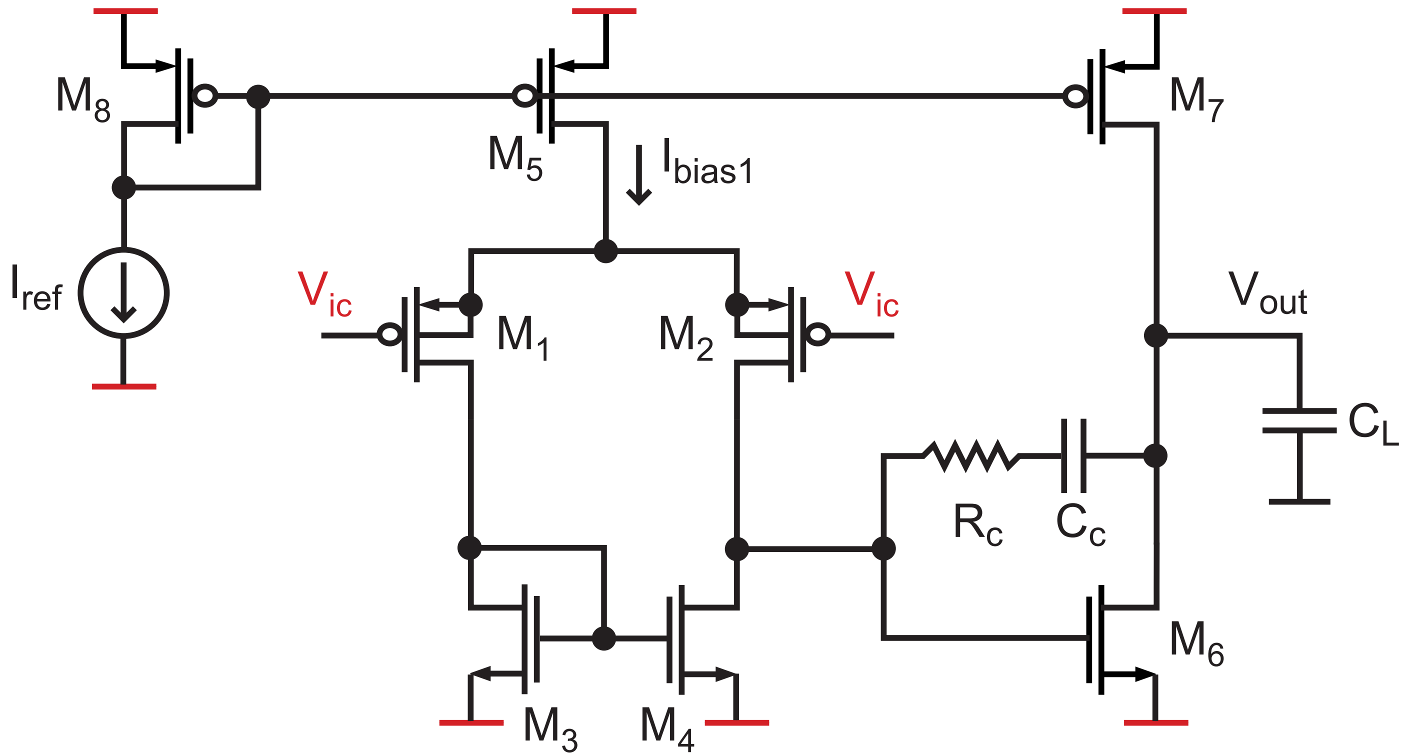
- **However, the *closed loop* configuration above tries to keep $V_{in+} = V_{in-}$ subject to finite differential gain a_{vd}**

$$V_{out} = a_{vd}(V_{in} - V_{out}) = a_{vd} V_{offset}$$

$$\Rightarrow \; \Delta V_{offset} = \frac{1}{a_{vd}} \Delta V_{out} = \frac{a_{vc}}{a_{vd}} \Delta V_{in}$$

$$\Rightarrow \; \frac{\Delta V_{offset}}{\Delta V_{in}} = \frac{a_{vc}}{a_{vd}} = (CMRR)^{-1}$$

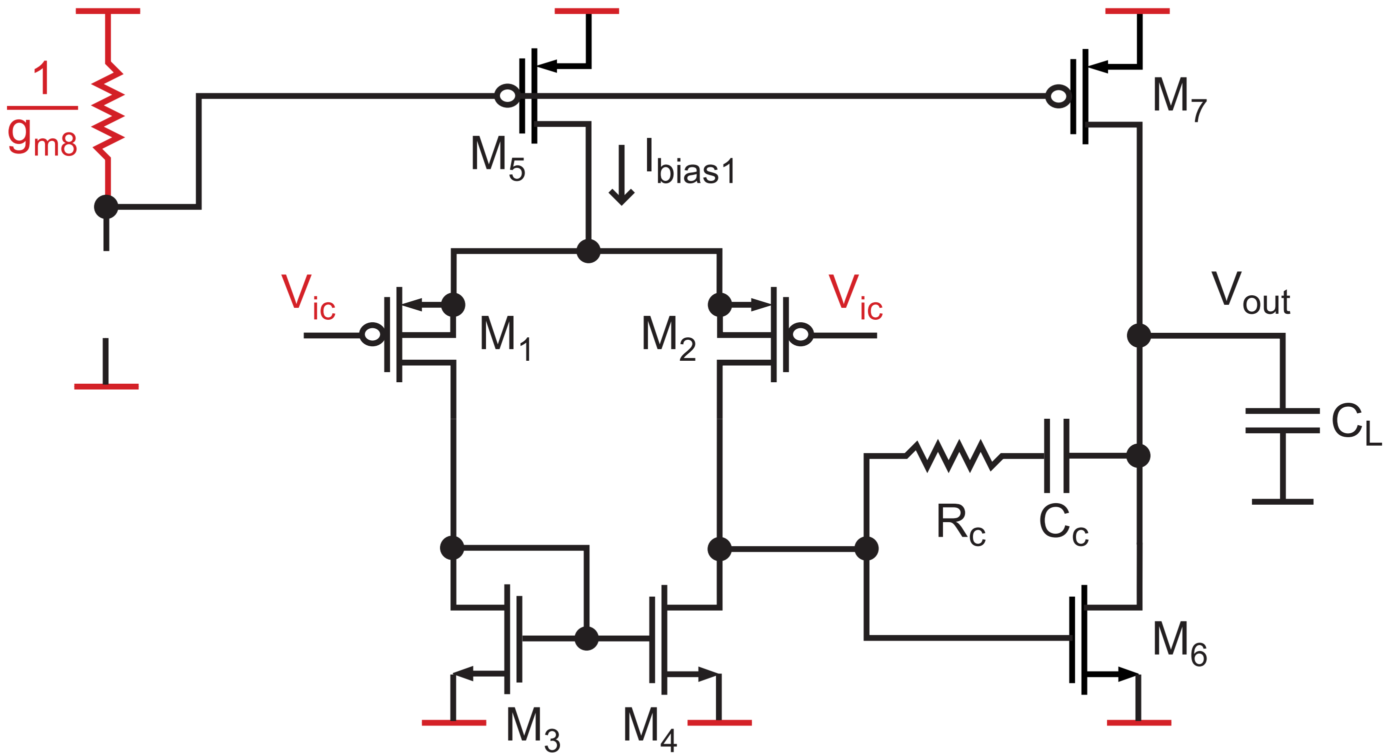
Power Supply Rejection Ratio (PSRR)



- **We now consider the impact of positive and negative supply variation on the output of the amplifier**
  - **Key assumption: $V_{in+} = V_{in-} = V_{ic}$**
- **Definitions:**

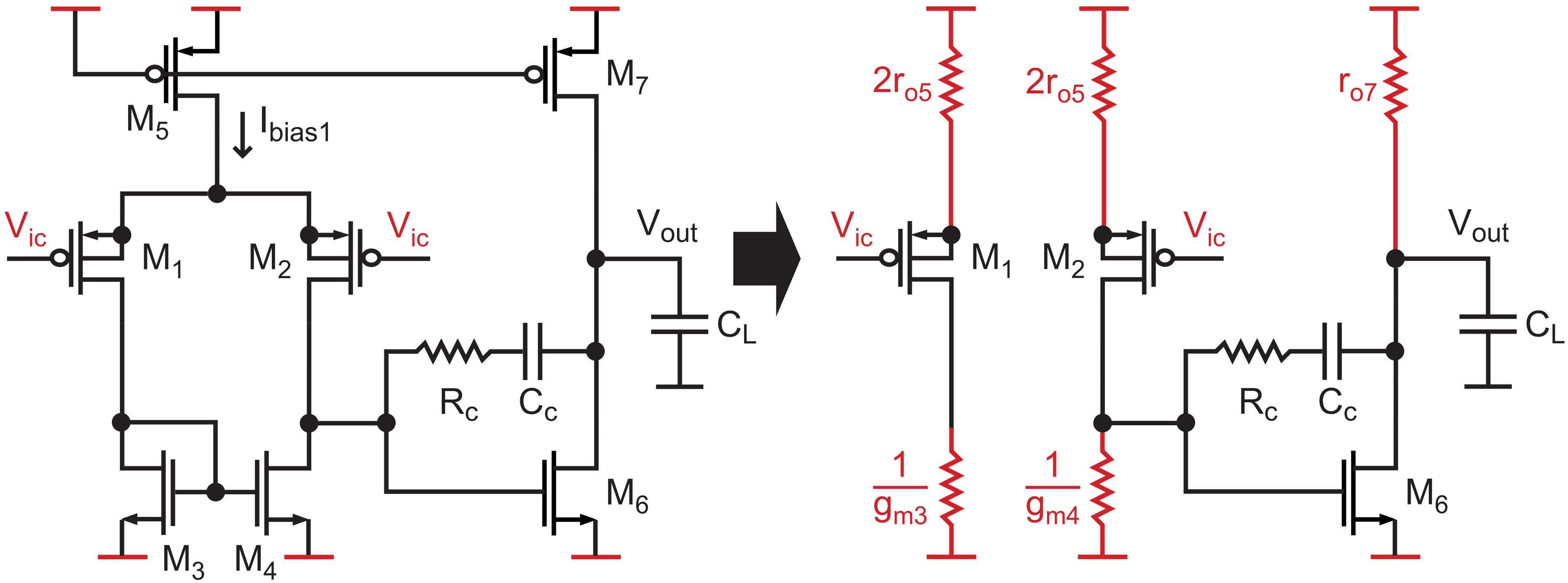
$$PSRR^{+} = \frac{a_{vd}}{a^{+}} \qquad PSRR^{-} = \frac{a_{vd}}{a^{-}}$$

Simplification of Current Mirror



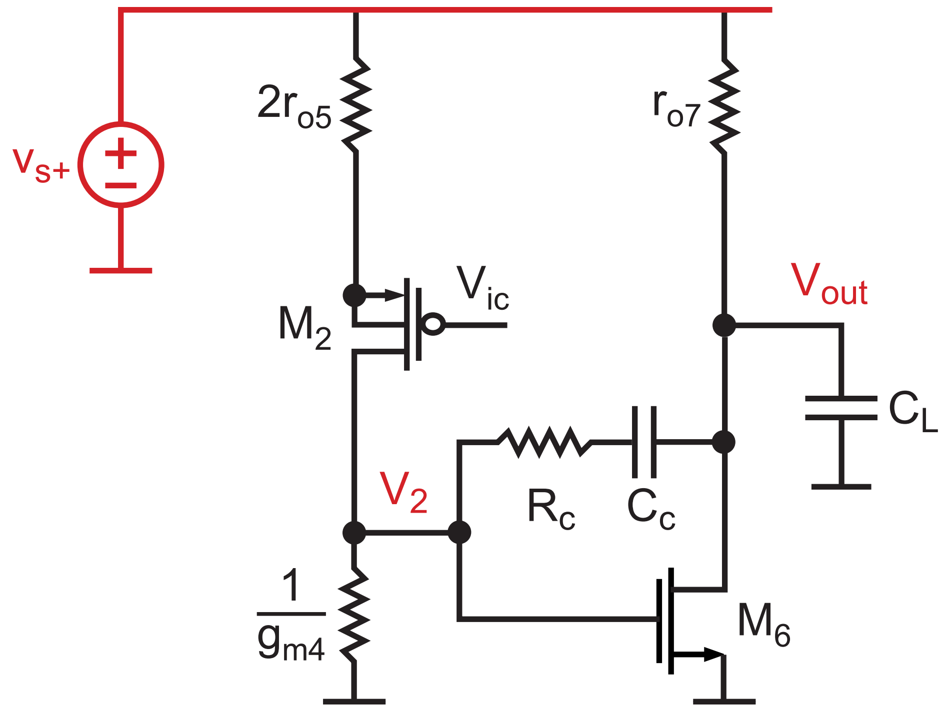
- **Replace current reference and diode connected device M_8 with their small signal models**
  - **We see that positive and negative supply variations have no impact on V_{gs} of M_5 and M_7**
    - We can ignore M_8 and current reference in our PSRR analysis

Further Simplifications for PSRR Calculations



- Observe that positive and negative supply variations have equal impact on both sides of the differential pair
  - We can use common-mode analysis for the first stage

Calculation of PSRR$^+$ At Low Frequencies



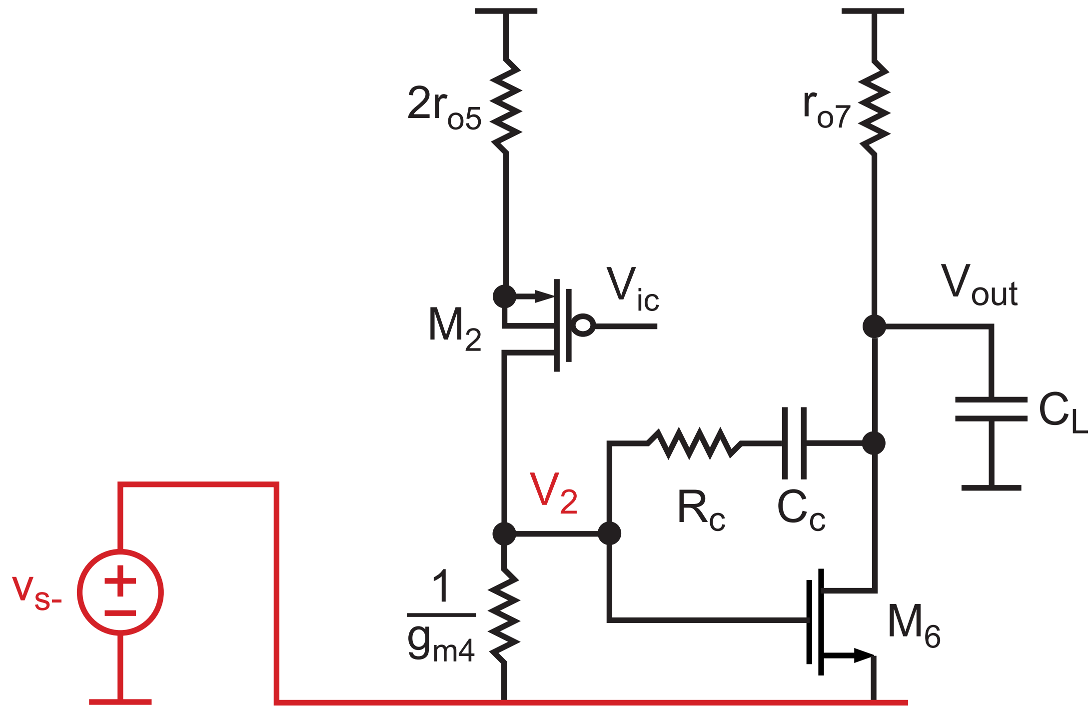
- **Calculation of impact of V_{s+} on V_{out}**

$$V_{out} = \frac{r_{o6}}{r_{o6} + r_{o7}} V_{s+} + g_{m6}(r_{o6}||r_{o7}) \left(\frac{1}{2g_{m4}r_{o5}}\right) V_{s+}$$

$$\Rightarrow \quad a_+ = \frac{V_{out}}{V_{s+}} \approx 1$$

$$\Rightarrow \quad PSRR^+ = \frac{a_{vd}}{a_{v+}} \approx a_{vd} = \boxed{g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})}$$

Calculation of PSRR⁻ At Low Frequencies



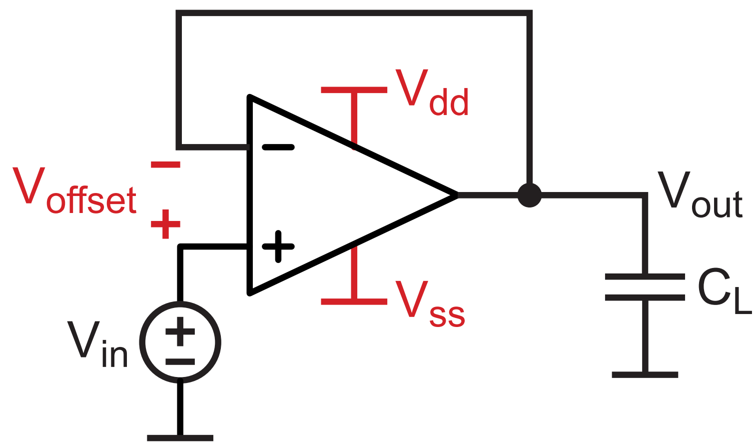
- **Calculation of impact of V_{s-} on V_{out}**

$$V_{out} \approx \frac{r_{o7}}{r_{o6}+r_{o7}} V_{s-} + g_{m6}(r_{o6}||r_{o7}) \left(\frac{1}{g_{m4}(g_{m2}r_{o2})2r_{o5}} \right) V_{s-}$$

$$\Rightarrow \quad a_- = \frac{V_{out}}{V_{s-}} \approx 1$$

$$\Rightarrow \quad PSRR^- = \frac{a_{vd}}{a_{v-}} \approx a_{vd} = \boxed{g_{m1}(r_{o2}||r_{o4})g_{m6}(r_{o6}||r_{o7})}$$

Characterizing PSRR with Changes in Offset Voltage



- **Consider V_{dd} as a common-mode signal which has an *open loop* impact on V_{out} as**

$$\Delta V_{out} = a_+ \Delta V_{dd}$$

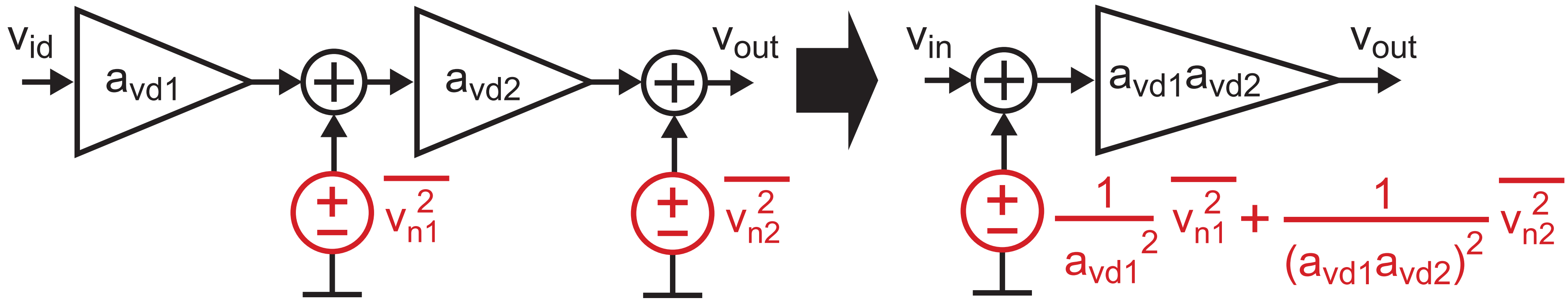
- **However, the *closed loop* configuration above tries to keep $V_{in+} = V_{in-}$ subject to finite differential gain a_{vd}**

$$V_{out} = a_{vd}(V_{in} - V_{out}) = a_{vd} V_{offset}$$

$$\Rightarrow \Delta V_{offset} = \frac{1}{a_{vd}} \Delta V_{out} = \frac{a_+}{a_{vd}} \Delta V_{dd}$$

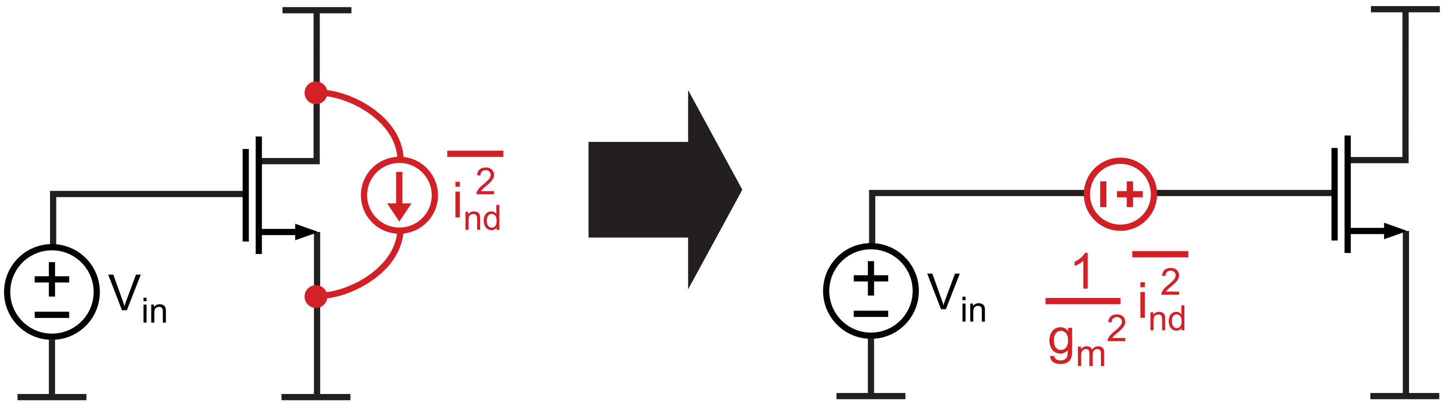
$$\Rightarrow \frac{\Delta V_{offset}}{\Delta V_{dd}} = \frac{a_+}{a_{vd}} = \left(PSRR^+\right)^{-1}$$ **(Similar for $PSRR^-$)**

Noise Analysis for a Two Stage Opamp



- **Each opamp stage will contribute noise**
  - **Typically the spectral density of the noise will be of the same order at each stage**
- **Input referral of the noise reveals that the second stage noise will have much less impact than the first stage noise**
  - **Input-referred noise calculations of an opamp need only focus on the first stage**

Input-Referral of MOS Device Noise



- **Transistor drain current noise:**

$$\overline{i_{nd}^2} = 4kT\frac{\gamma}{\alpha}g_m\Delta f + \frac{K_f}{f}\frac{g_m^2}{WLC_{ox}^2}\Delta f$$

Thermal noise **1/f noise**

Note:

$$g_{ds0} = \frac{g_m}{\alpha}$$

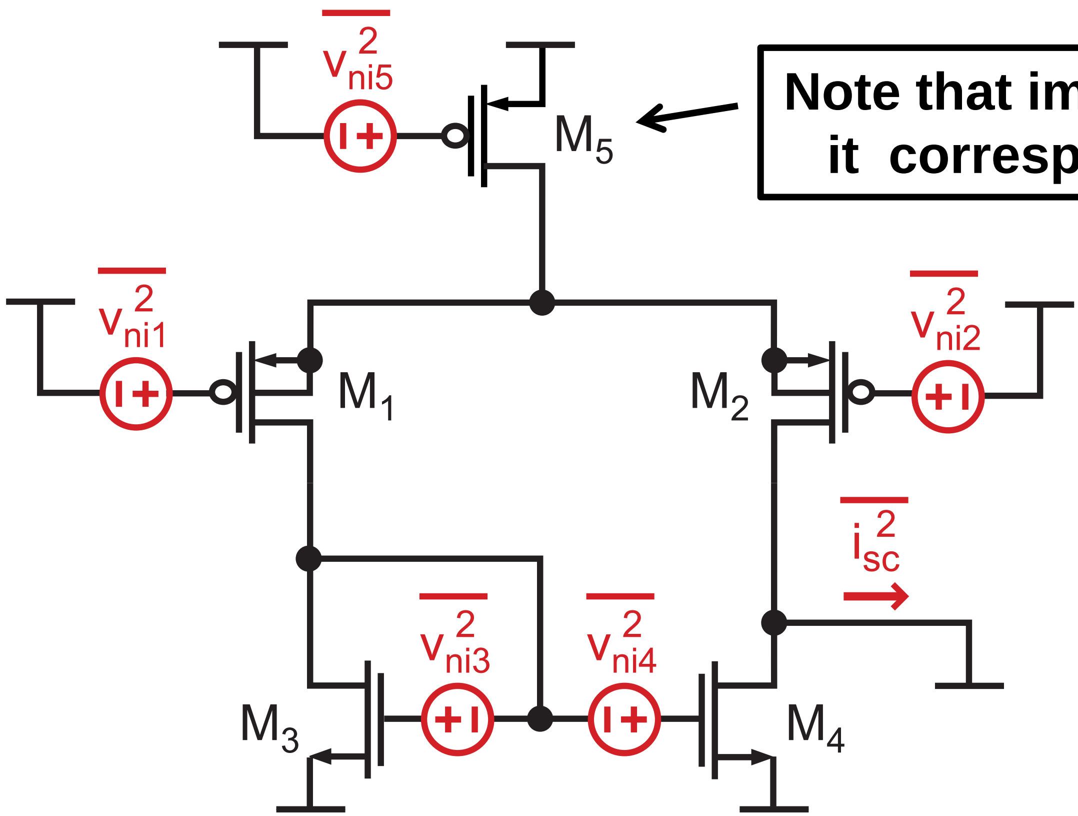
- **Input-referred voltage noise:**

$$\overline{v_{ni}^2} = 4kT\frac{\gamma}{\alpha}\frac{1}{g_m}\Delta f + \frac{K_f}{f}\frac{1}{WLC_{ox}^2}\Delta f$$

Thermal noise **1/f noise**

Impact of thermal versus 1/f noise depends on g_m

Analysis of Op Amp Output Noise (First Stage)



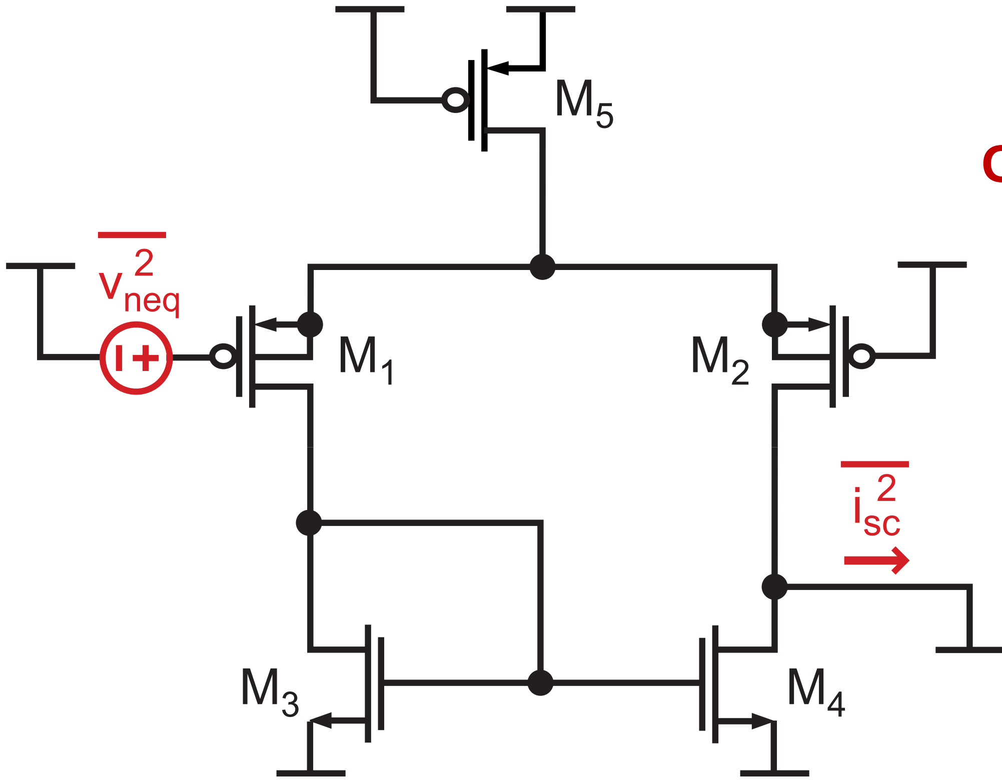
Note that impact of M_5 noise is minor since it corresponds to common-mode noise

Assume:
$g_{m1} = g_{m2}$
$g_{m3} = g_{m4}$

$$\overline{i_{sc}^2} = g_{m1}^2\left(\overline{v_{ni1}^2} + \overline{v_{ni2}^2}\right) + g_{m3}^2\left(\overline{v_{ni3}^2} + \overline{v_{ni4}^2}\right)$$

$$\Rightarrow \overline{i_{sc}^2} = 2g_{m1}^2\overline{v_{ni1}^2} + 2g_{m3}^2\overline{v_{ni3}^2}$$

Determining Input-Referred Noise



Output noise due to equivalent input-referred noise:

$$\overline{i_{sc}^2} = g_{m1}^2 \overline{v_{neq}^2}$$

Assume:
$g_{m1} = g_{m2}$
$g_{m3} = g_{m4}$

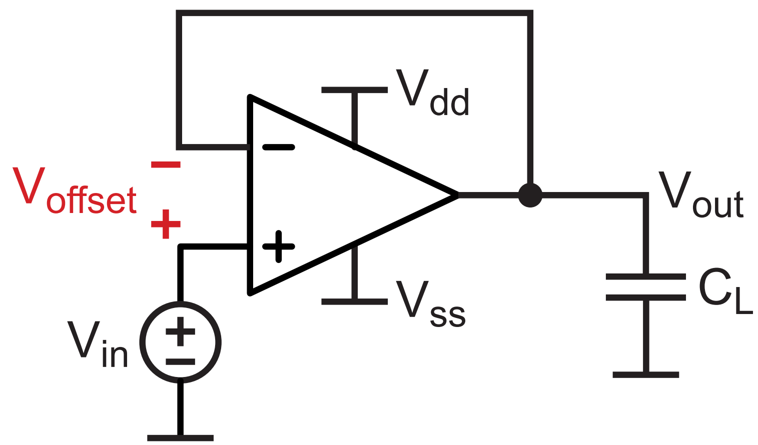
- Output noise due to individual devices (Slide 20):

$$\overline{i_{sc}^2} = 2g_{m1}^2 \overline{v_{ni1}^2} + 2g_{m3}^2 \overline{v_{ni3}^2} = g_{m1}^2 \overline{v_{neq}^2}$$

$$\overline{v_{neq}^2} = 2\overline{v_{ni1}^2} + 2\left(\frac{g_{m3}}{g_{m1}}\right)^2 \overline{v_{ni3}^2}$$

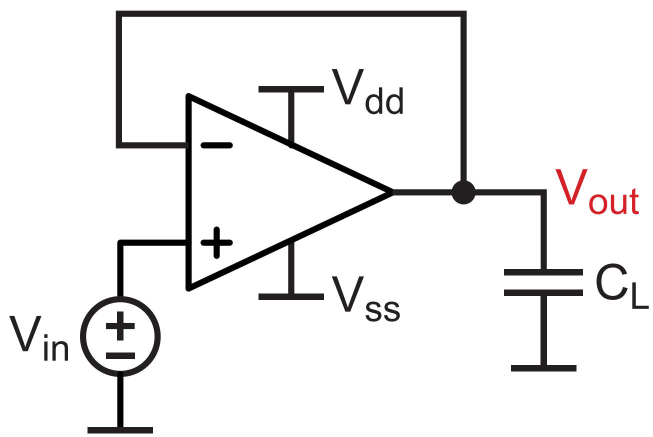
Want $g_{m1} > g_{m3}$ for low noise

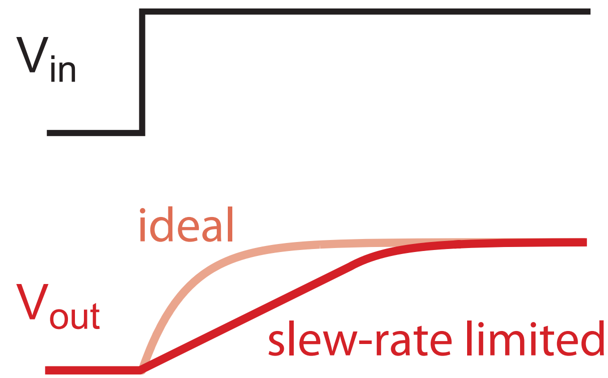
Characterizing Input-Referred Noise



- **Placing the amplifier within unity gain feedback configuration causes the overall output noise of the amplifier to become referred to the input**
  - **We can now examine the low frequency content of the input-referred noise by simply probing the noise of V_{out}**

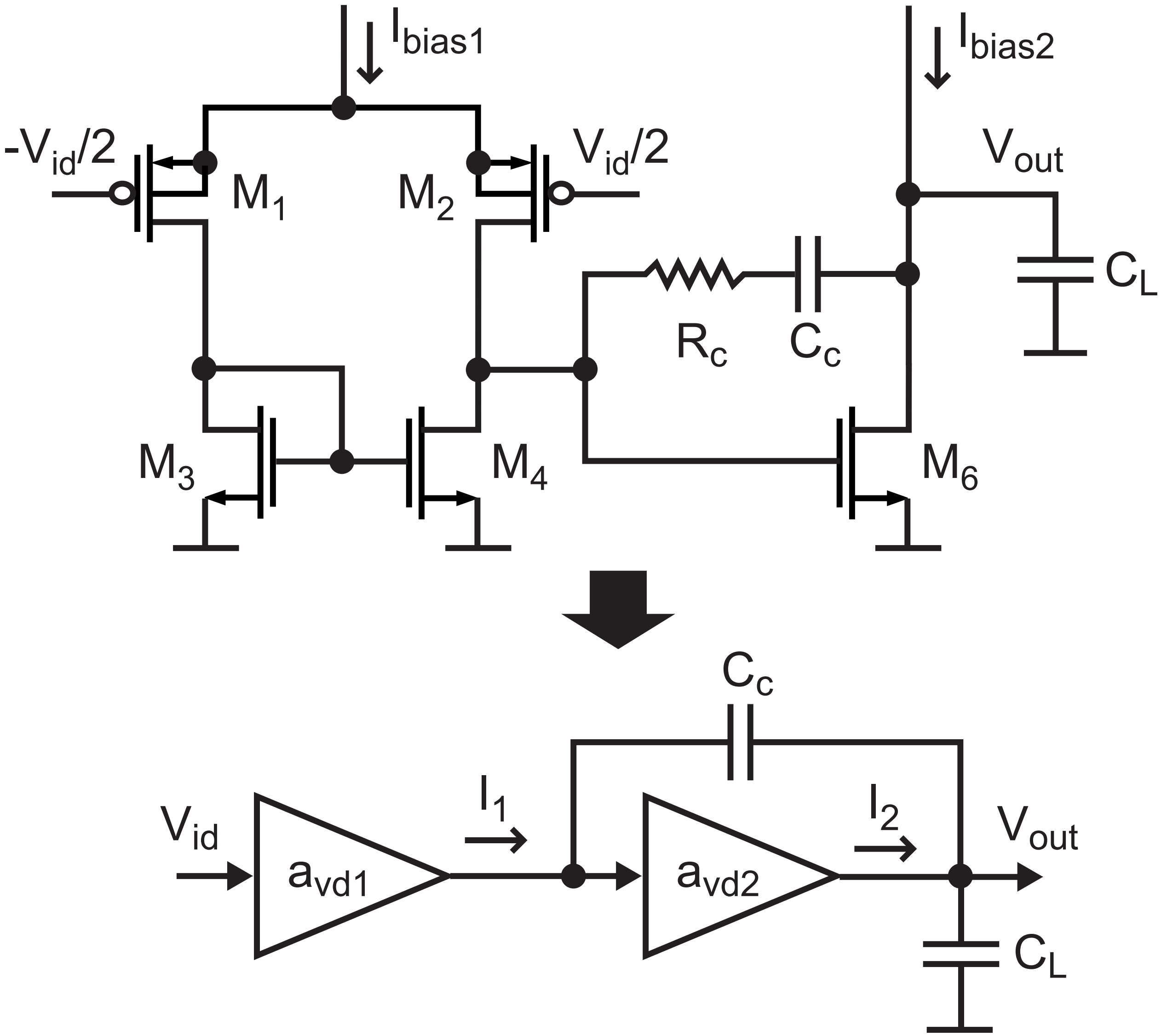
Recall: Slew Rate Issues for Opamps





- **Output currents of practical opamps have max limits**
  - **Impacts maximum rate of charging or discharging load capacitance, C_L**
  - **For large step response, this leads to the output lagging behind the ideal response based on linear modeling**
    - We refer to this condition as being slew-rate limited
- **Where slew-rate is of concern, the output stage of the opamp can be designed to help mitigate this issue**
  - **Will lead to extra complexity and perhaps other issues**

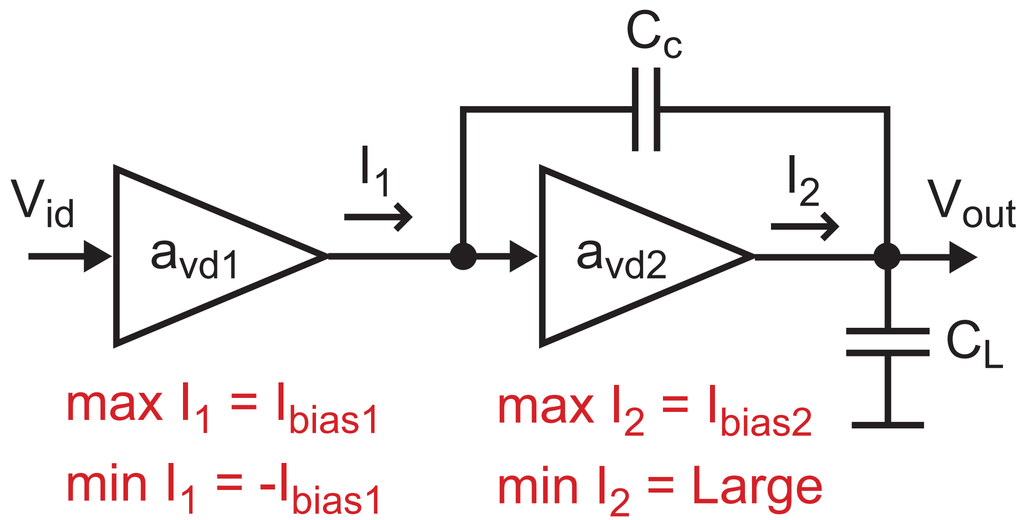
Key Observations for Slew Rate Calculations



Current Limits

- First stage
  - Max $I_1 = I_{bias1}$
  - Min $I_1 = -I_{bias1}$
- Second stage
  - Max $I_2 = I_{bias2}$
  - Min I_2 = Large

Slew Rate Analysis (First Stage Limits)

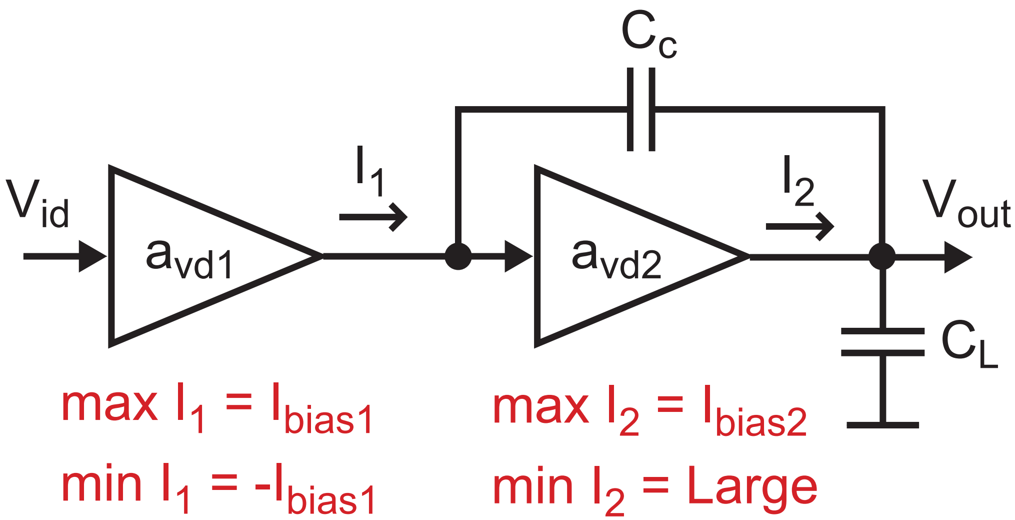


- **Slew rate refers to maximum voltage slope at output**
  - **Impact of current limits in first stage:**

$$V_{out} = -\frac{1}{C_c}\int I_1 dt \;\Rightarrow\; \left.\frac{dV_{out}}{dt}\right|_{max} = -\left.\frac{I_1}{C_c}\right|_{max} = \frac{I_{bias1}}{C_c}$$

$$\left.\frac{dV_{out}}{dt}\right|_{min} = -\left.\frac{I_1}{C_c}\right|_{min} = -\frac{I_{bias1}}{C_c}$$

Slew Rate Analysis (Second Stage Limits)



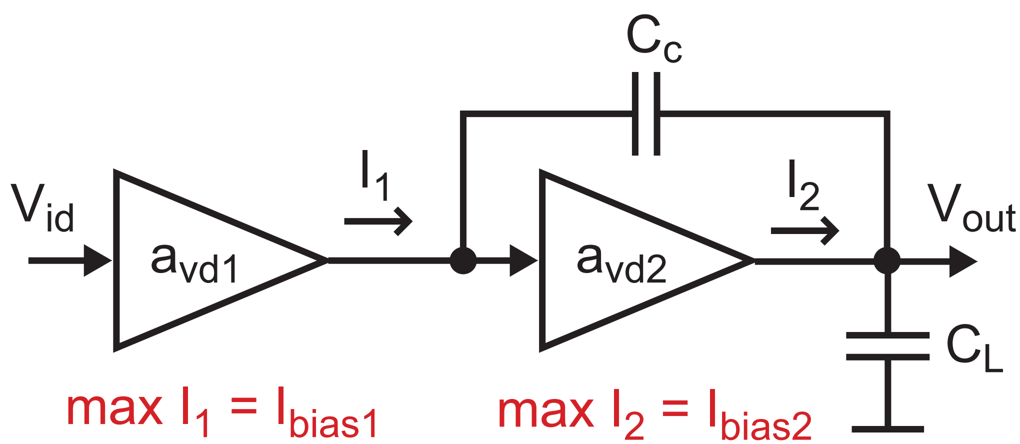
- **Impact of current limits in second stage**
  - **Maximum slope at the output:**

$$\left.\frac{dV_{out}}{dt}\right|_{max} = \frac{I_{bias2}}{C_c + C_L}$$

  - **Minimum slope at the output:**

$$\left.\frac{dV_{out}}{dt}\right|_{min} = \text{Large}$$

Slew Rate Analysis (Overall)



max $I_1 = I_{bias1}$ max $I_2 = I_{bias2}$

min $I_1 = -I_{bias1}$ min I_2 = Large

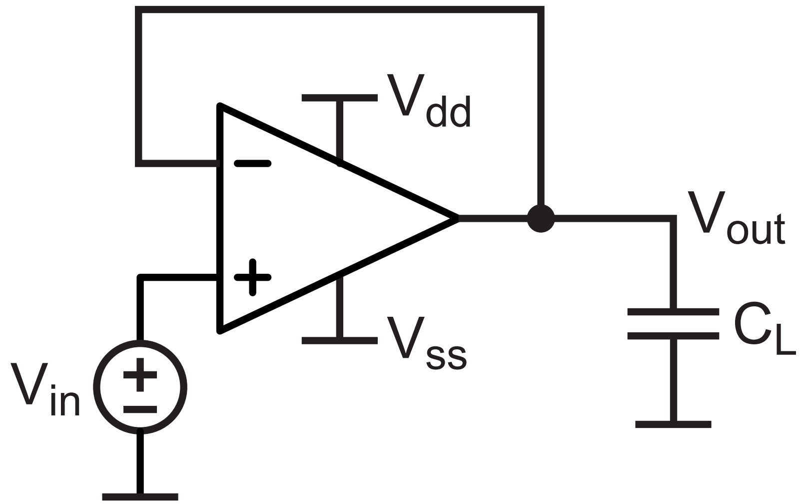
- **Maximum slope at the output:**

$$\left.\frac{dV_{out}}{dt}\right|_{max} = \min\left(\frac{I_{bias1}}{C_c}, \frac{I_{bias2}}{C_c + C_L}\right)$$

- **Minimum slope at the output:**

$$\left.\frac{dV_{out}}{dt}\right|_{min} = \frac{-I_{bias1}}{C_c}$$

Impact of Slew Rate



- **Consider the closed loop, unity gain configuration above with a sine wave input**

$$V_{in} = A\sin(wt)$$

- **Note: the max slope of the input depends on *A* and w**

$$\frac{dV_{in}}{dt} = Aw\cos(wt) \quad \Rightarrow \quad \left.\frac{dV_{out}}{dt}\right|_{max} = Aw$$

Slew rate limits the maximum frequency that the amplifier can track

Summary

- **Opamp design must take into consideration many different specifcations**
- **Today we covered**
  - **Systematic offset voltage**
  - **CMRR**
  - **$PSRR^+$ and $PSRR^-$**
  - **Input-referred voltage noise**
  - **Slew rate**